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Power Quality Improvement of BLDC Drive using D-STATCOM

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Abstract

Distribution static compensator (DSTATCOM) is a shunt compensation device that is generally used to solve power quality problems in distribution systems. In this project a new algorithm to generate reference voltage for a distribution static compensator (DSTATCOM) operating in voltage-control mode. The proposed scheme ensures that unity power factor (UPF) is achieved at the load terminal during nominal operation, which is not possible in the traditional method. Also, the compensator injects lower currents and, therefore, reduces losses in the feeder and voltage-source inverter. In this paper, implementing Power quality circuit with voltage source converter in the BLDC Motor drive is developed. The control of BLDC drive used is Field Oriented Control using pulse with Modulation. The power quality circuit proposed here improves the power factor and reduces harmonic distortion. Simulation work is performed using MATLAB / SIMULINK environment.

Index Terms—***Current Control Mode, Power Quality (PQ), Voltage-Control Mode, Voltage-Source Inverter.***

I. INTRODUCTION

Power Quality (PQ) is the key to successful delivery of quality product and operation of an industry. The increased application of electronic loads and electronic controllers which are sensitive to the quality of power makes serious economic consequences and of revenues loss each year. Poor PQ can cause malfunctioning of equipment performance, harmonics, voltage imbalance, sag and flicker problems, standing waves and resonance – are some of the issues that adversely affect production and its quality leading to huge loss in terms of product, energy and damage to equipment. Thus, it becomes imperative to be aware of quality of power grid and the deviation of the quality parameters from the norms /standard such as IEEE-519 standard [1] to avoid breakdown or equipment damage.

In present day distribution systems (DS), major power consumption has been in reactive loads. The typical loads may be computer loads, lighting ballasts, small rating adjustable speeds drives (ASD) in air conditioners, fans, refrigerators, pumps and other domestic and commercial appliances are generally behaved as nonlinear loads. These loads draw lagging power-factor currents and therefore give rise to reactive power burden in the DS. Moreover, situation worsens in the presence of unbalanced and non-linear loads, affect the quality of source currents to a large extent. It affects the voltage at point of common coupling (PCC) where the facility is connected. This has adverse effects on the sensitive equipments connected to PCC and may damage the equipment appliances. Excessive reactive power demand increases feeder losses and reduces active power flow capability of the DS, whereas unbalancing affects the operation of transformers and generators [2-3].

The BLDC Motor used to make low power rating application devices such as Refrigerator, Washing Machine, House-hold appliances, Medical Equipment, Wide speed range of servo drives and industrial robots. BLDC drives are used for its high efficiency, fast

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dynamic response and small size etc. For the operation of BLDC Drive first need to convert AC supply power to DC power using rectifier circuit and then DC power to variable magnitude and variable frequency AC power to feed BLDC. BLDC operates on two mode vector control and direct torque control. Here we are using vector control BLDC.

II. PROPOSED CONTROL SCHEME

Circuit diagram of a DSTATCOM-compensated distribution system is shown in Fig.1. It uses a three-phase, four-wire, two-level, neutral-point-clamped VSI. This structure allows independent control to each leg of the VSI [7]. Fig.2 shows the single-phase equivalent representation of Fig.1. Variable is a switching function, and can be either or depending upon switching state. Filter inductance and resistance are and, respectively. Shunt capacitor eliminates high-switching frequency components. First, discrete modeling of the system is presented to obtain a discrete voltage control law, and it is shown that the PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. Then, a procedure to design VSI parameters is presented. A proportional-integral (PI) controller is used to regulate the dc capacitor voltage at a reference value. Based on instantaneous symmetrical component theory and complex Fourier transform, a reference voltage magnitude generation scheme is proposed that provides the advantages of CCM at nominal load. The overall controller block diagram is shown in Fig. 3 These steps are explained as follows.

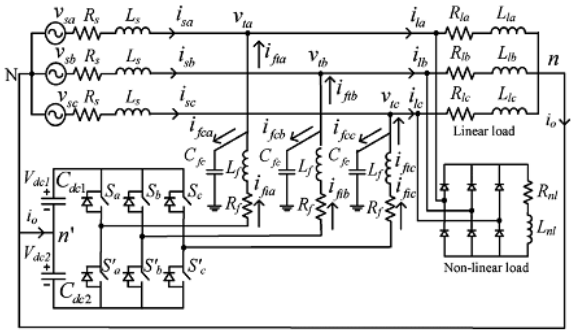

Fig.1.Circuit diagram of the DSTATCOM-compensated distribution system.

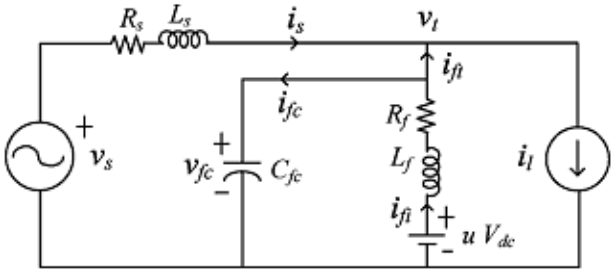

Fig.2 Single-phase equivalent circuit of DSTATCOM.

A. System Modeling and Generation of the Voltage-Control Law

The state-space equations for the circuit shown in Fig. 2 are given by

$$\dot{x} = Ax + Bz \quad (1)$$

$$A=\begin{bmatrix} 0 & \frac{1}{Cf_c} & 0 \\ -\frac{1}{L_f} & 0 & 0 \\ -\frac{1}{L_s} & 0 & -\frac{R_S}{L_s} \end{bmatrix}$$

$$B=\begin{bmatrix} 0 & -\frac{1}{Cf_c} & 0 \\ \frac{V_{dc}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{L_s} \end{bmatrix}$$

$$x=[v_{fc} \quad i_{fi} \quad i_s]^t,\ z=[u \quad i_{ft} \quad v_s]^t$$

The general time-domain solution of (1) to compute the state vector x (t) with known initial value x (t_0), is given as follows:

$$X(t) = X(e^{A(t-t_0)})\, x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)} B\, z(\tau)\, d\tau \quad (2)$$

The equivalent discrete solution of the continuous state is obtained by replacing t_0= k$T_d$and t= (k+1)T_d as follows:

$$X(k+1) = e^{AT_d} x(k) + \int_{kT_d}^{T_d} e^{A(T_d+kt_d-\tau)} B\, z(\tau)\, d\tau \quad (3)$$

In (3), k and T_d represent the K_{th} sample and sampling period, respectively. During the consecutive sampling period, the value of z (τ) is held constant, and can be taken as z (k) .After simplification and changing the integration variable, (3) is written as [12]

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$$X(k+1) = e^{AT_d}x(k) + \int_0^{T_d} e^{A\lambda}B\lambda B\, z(K) \quad (4)$$

Equ.4.is re written as follows

$$x(k+1) = G\,x(K) + H\,z(k)$$

Where G and H are sampled matrices, with a sampling time of T_d. For small sampling time, matrices and are calculated as follows:

$$G=\begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix}$$

$$=e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2} \quad (6)$$

$$H=\begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda}Bd\lambda$$

$$=\int_0^{T_d}(I + A\lambda)B\lambda \quad (7)$$

From (6) and (7) $G_{11}= 1 - T_d^2/2L_Fc_{fc}$, $G_{12}= T_d/ c_{fc}- T_d^2R_f/2L_Fc_{fc}$,$G_{13} = 0$, $H_{11} = T_d^2v_{dc}/2L_Fc_{fc}$,$H_{12}= -T_d/c_{fc}$, $H_{13} = 0$.

Hence, the capacitor voltage using (8) is given as

$$v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{f1} + H_{11}\,u(k) + H_{12}\,i_{f1}\,(k). \quad (8)$$

As seen from (8), the terminal voltage can be maintained at a reference value depending upon the VSI parametersv_{dc}, c_{fc},L_F,R_F, and sampling timeT_d. Therefore, VSI parameters must be chosen carefully. Let v_t^* be the reference load terminal voltage. A cost function J is chosen as follows [8]:

$$J = [v_{fc}(k+1) - v_t^*(k+1)^2 \quad (9)$$

The cost function is differentiated with respect to u (k) and its minimum is obtained at

$$V_{fc}(K+1)=V_t^*(K+1) \quad (10)$$

The deadbeat voltage-control law, from (8) and (10), is given as

$$u_t^*(k) = \frac{v_t^*(k+1) - G_{11}v_{fc}(k) - G_{12}i_{f1}(k) - H_{12}\,i_{ft}(k)}{H_{11}} \quad (11)$$

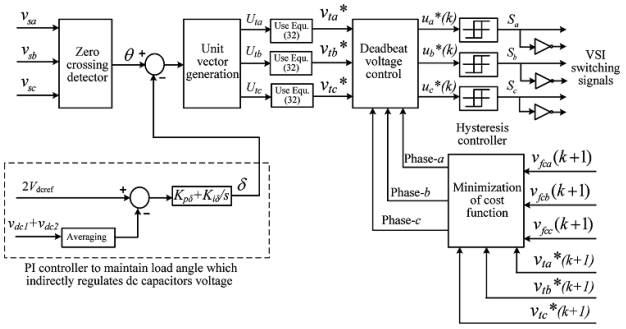

Fig.3 Overall block diagram of the controller to control DSTATCOM in a distribution system.

In (11), $v_t^*(k+1)$ is the future reference voltage which is unknown. One-step-ahead prediction of this voltage is done using a second-order Lagrange extrapolation formula as follows:

$$v_t^*(k+1) = 3\,v_t^*(k) - 3\,v_t^*(k-1) + v_t^*(k-2). \quad (12)$$

The term $v_t^*(k+1)$ is valid for a wide frequency range and when substituted in (11), yields to a one-step-ahead deadbeat voltage-control law. Finally $u_t^*(k)$, is converted into the ON/OFF switching command to the corresponding VSI switches using a deadbeat hysteresis controller.

B. Design of VSI Parameters

DSTATCOM regulates terminal voltage satisfactorily, depending upon the properly chosen VSI parameters. The design procedure of these parameters is presented as follows.

Voltage Across DC Bus (v_{dc}): The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

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DC Capacitance (C_{dc}): Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients. Let the total load rating be S kVA. In the worst case, the load power may vary from minimum to maximum that is, from 0 to S kVA. The compensator needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in the deviation of capacitor voltage from its reference value. The voltage continues to decrease until the capacitor voltage controller comes into action. Consider that the voltage controller takes a ρ cycle that is ρT, seconds to act, where T the system is time period. Hence, maximum energy exchange by the compensator during transient will be. This energy will be ρ S T equal to the change in the capacitor stored energy. Therefore

$$\frac{1}{2}C_{\mathrm{dc}}\left(V_{\mathrm{dcref}}^2 - V_{\mathrm{dc}}^2\right) = p\,S\,T \tag{13}$$

Where and are the reference dc bus voltage and maximum-allowed voltage during transients, respectively. Hence

$$C_{\mathrm{dc}} = \frac{2\,p\,S\,T}{V_{\mathrm{dcref}}^2 - V_{\mathrm{dc}}^2}. \tag{14}$$

Here, S=10 kVA, $V_{dcref=}$650 V, ρ=1, and or, $V_{dcref=}0.8V_{dcref}$ OR $1.2V_{dcref}$. Using (14), capacitor values are found to be 2630 and 2152μF. The capacitor value 2600 μF is chosen to achieve satisfactory performance during all operating conditions.

Filter InductanceL_f : Filter inductance L_f should provide reasonably high switching frequency(f_{max}) and a sufficient rate of change of current such that VSI currents follow desired currents. The following equation represents inductor dynamics:

$$L_f\frac{di_{fi}}{dt} = -v_{fc} - R_f i_{fi} + V_{\mathrm{dc}}. \tag{15}$$

The inductance L_f is designed to provide good tracking performance at a maximum switching frequency(f_{max}) which is achieved at the zero of the source voltage in the hysteresis controller. Neglecting R_f, L_f is given by

$$L_f = \frac{2\,V_m}{(2\,h_c)\,(2\,f_{\max})} = \frac{0.5\,V_m}{h_c\,f_{\max}} \tag{16}$$

Where $2h_c$ is the ripple in the current. With f_{max} = 10 kHz and h_c = 0.75 A (5% of rated current), the value L_f of using (16) is foundtobe21.8mH, and 22Mh is used in realizing the filter.

Shunt Capacitor (C_{fc}): The shunt capacitor should not resonate with feeder inductance at the fundamental frequency (ω_0). Capacitance, at which resonance will occur, is given as

$$C_{fcr} = \frac{1}{\omega_o^2\,L_s}. \tag{17}$$

For proper operation, C_{fc} must be chosen very small compared to C_{fcr} . Here, a value of 5μF is chosen which provides an impedance of 637 ohm atω_0. This does not allow the capacitor to draw significant fundamental reactive current.

III. CONTROLLER FOR DC BUS CAPACITOR VOLTAGE

Average real power balance at the PCC will be

$$P_{\mathrm{pcc}} = P_{lavg} + P_{\mathrm{loss}} \tag{18}$$

Where P_{pcc}, P_{1avg}, and P_{loss} are the average PCC power, load power, and losses in the VSI, respectively. The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle. Hence δ must be maintained P_{pcc} constant to keep constant. The voltage of the dc bus of DSTATCOM can be maintained at its reference value by taking inverter losses P_{loss} from the source. If the capacitor voltage is regulated to a constant reference valueP_{loss}, is a constant value. Consequently, δ is also a constant value. Thus, it is evident that dc-link voltage can be regulated by generating a suitable value δ of .This δ includes the effect of losses in the VSI and, therefore, it takes care of P_{loss} the term in its action. To calculate load angle δ, the averaged dc-link voltage ($V_{dc1} + V_{dc2}$) is compared with a reference voltage, and error is passed

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through a PI controller. The output of the PI controller, which is load angle δ, is given as follows:

$$\delta = K_{p\delta}\, e_{vdc} + K_{i\delta} \int e_{vdc}\, dt \qquad (19)$$

Where $e_{vdc} = 2V_{dcref-(V_{dc1}+V_{dc2})}$ is the voltage error. Terms $K_{p\delta}$ and $K_{i\delta}$ are proportional and integral gains, respectively. δ must lie between 0 to 90^0 for the power flow from the source to PCC. Hence, controller gains must be chosen carefully.

IV. BLDC MOTOR

BLDC engine comprises of the perpetual magnet rotor and an injury stator. The brushless engines are controlled utilizing a three stage inverter. The engine obliges a rotor position sensor for beginning and for giving legitimate compensation arrangement to turn on the force gadgets in the inverter extension. In light of the rotor position, the force gadgets are commutated consecutively every 60 degrees. The electronic compensation takes out the issues connected with the brush and the commutator plan, in particular starting and destroying of the commutator brush course of action, along these lines, making a BLDC engine more rough contrasted with a dc engine. Fig.4 demonstrates the stator of the BLDC engine and fig.5 shows rotor magnet plans.

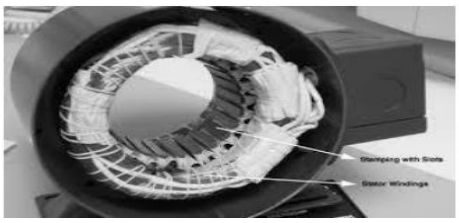

Fig.4. BLDC motor stator construction

Fig.5. BLDC motor Rotor construction.

The brush less dc engine comprise of four fundamental parts Power converter, changeless magnet brushless DC Motor (BLDCM), sensors and control calculation. The force converter changes power from the source to the BLDCM which thus changes over electrical vitality to mechanical vitality. One of the remarkable highlights of the brush less dc engine is the rotor position sensors, in view of the rotor position and order signals which may be a torque charge, voltage summon, rate order etc; the control calculation s focus the entryway sign to every semiconductor in the force electronic converter.

The structure of the control calculations decides the sort of the brush less dc engine of which there are two principle classes voltage source based drives and current source based drives. Both voltage source and current source based commute utilized for perpetual magnet brushless DC machine. The back emf waveform of the engine is demonstrated in the fig. 6. Be that as it may, machine with a non sinusoidal back emf brings about diminishment in the inverter size and lessens misfortunes for the same influence level.

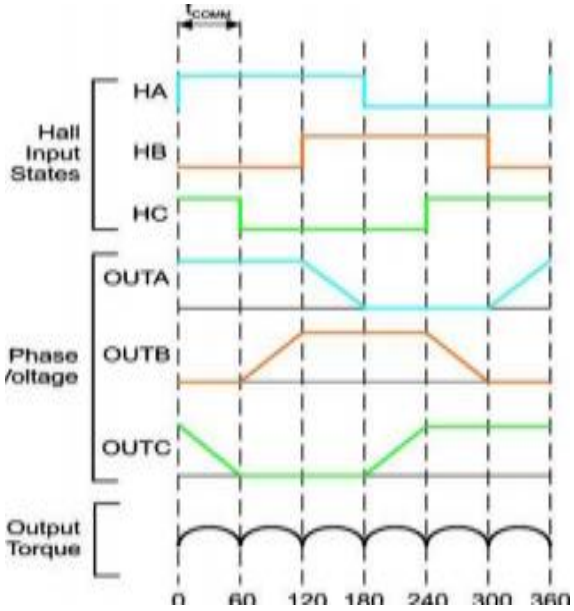

Fig.6. Hall signals & Stator voltages.

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V.MATLAB/SIMULINK RESULTS

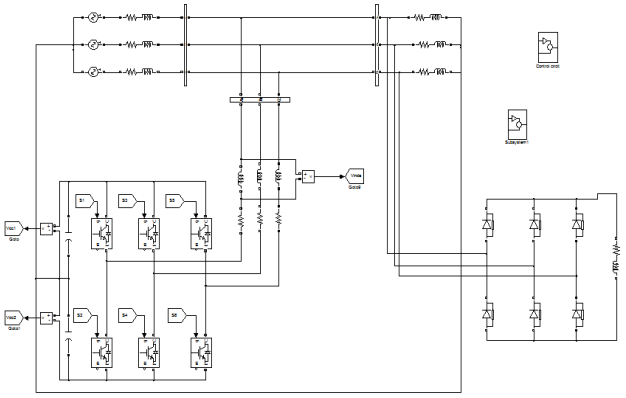

Fig.7.Simulation results for Conventional/Proposed system.

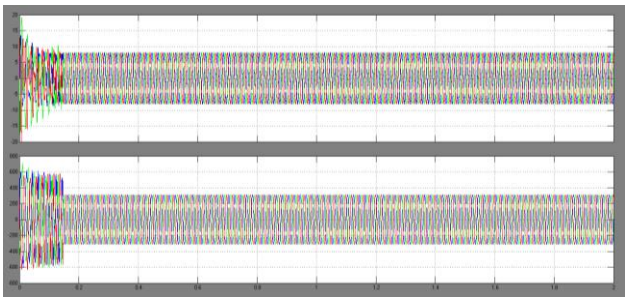

Fig.8.Source voltage and current.

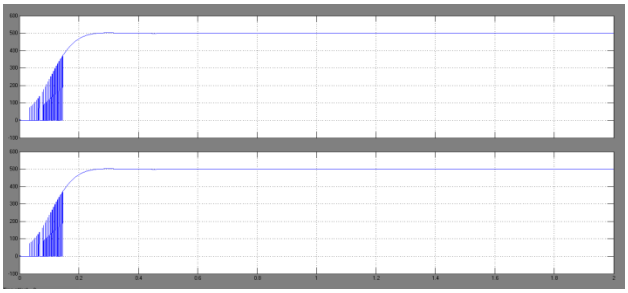

Fig.9.dc link voltage.

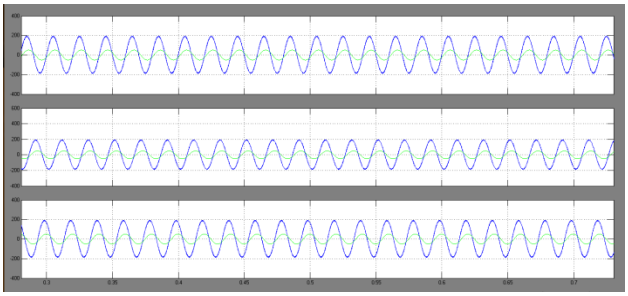

Fig.10. Terminal voltages and source currents using the traditional method. (a) Phase-A. (b) Phase-B. (c) Phase-C.

Initially, the traditional method is considered. Fig.10. shows the regulated terminal voltages and corresponding source currents in phases a, b, and c, respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents.

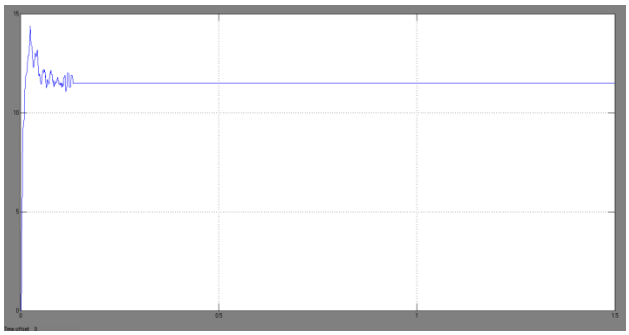

Fig.11. Phase- source RMS currents.

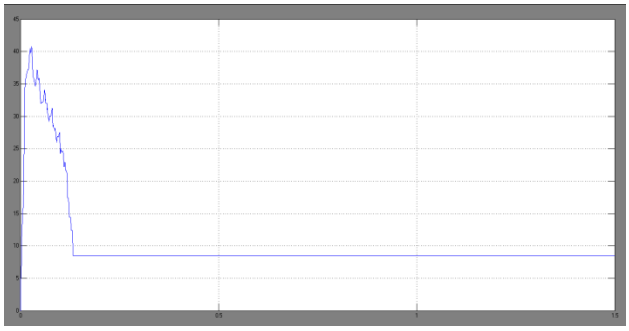

Fig.12. Phase- compensator RMS currents.

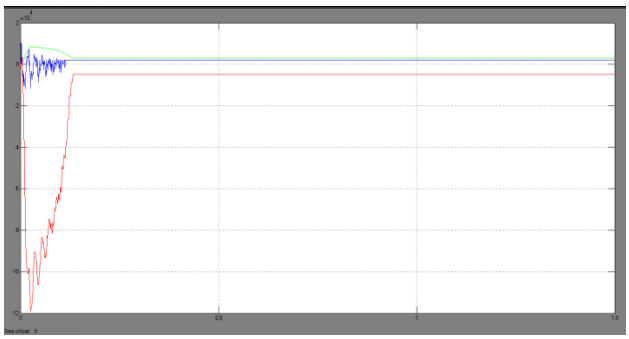

Fig.13. Load reactive power (Q-Load), compensator reactive power (Q-VSI), and reactive power at PCC (Q-PCC).

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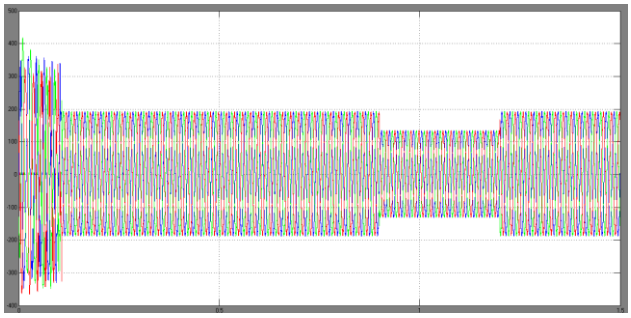

Fig.14. Simulation results for Source Voltage During Sag.

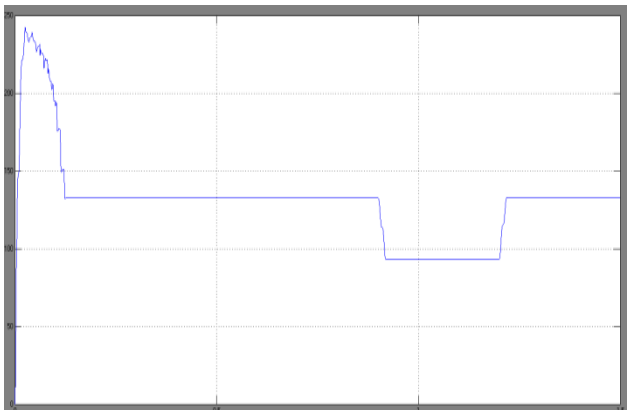

Fig.15. simulation result for RMS value of source voltage during sag

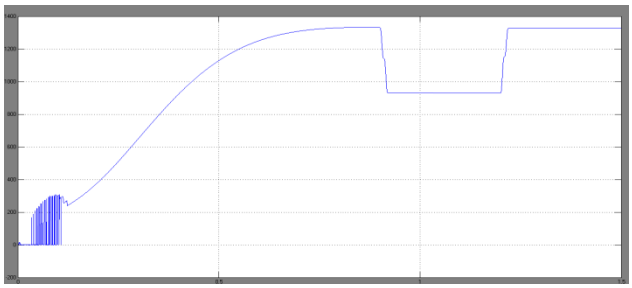

Fig.16.Simulation results for dc link voltage.

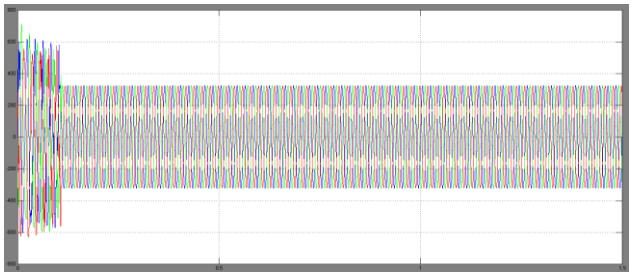

Fig.17. Simulation results for load voltage after compensation

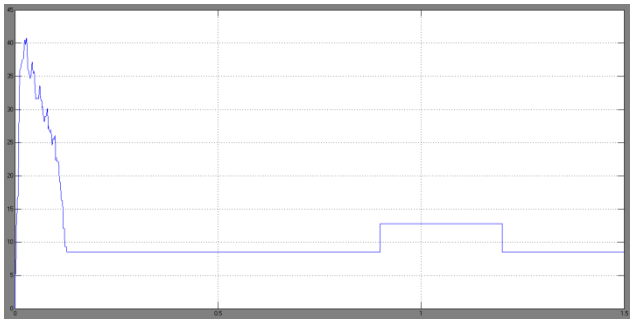

Fig.18. simulation results for compensation current of D-statcom.

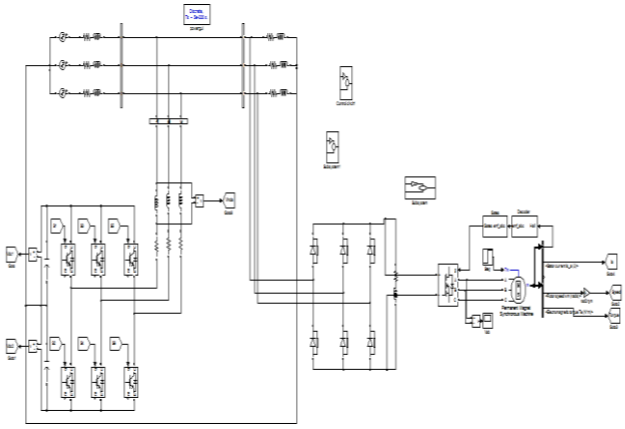

Fig.19. Simulink circuit for conventional D-statcom with BLDC drive.

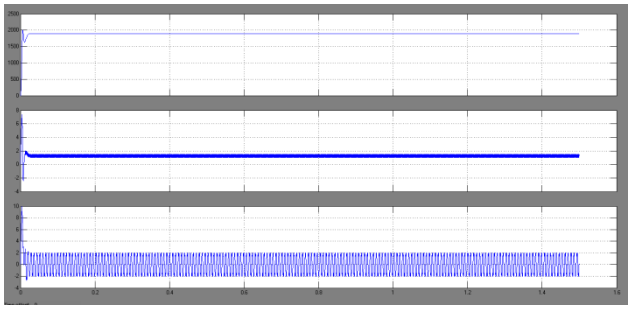

Fig.20.speed, torque and armature current of BLDC drive.

V.CONCLUSION

In this paper, a control algorithm has been proposed for the generation of reference load voltage for a voltage-controlled DSTATCOM. The performance of the proposed scheme is compared with the traditional voltage-controlled DSTATCOM. The proposed method provides the following advantages:

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1) At nominal load, the compensator injects reactive and harmonic components of load currents, resulting in UPF;
2) Nearly UPF is maintained for a load change;
3) Fast voltage regulation has been achieved during voltage disturbances.

The SVM inverter increases the output voltage and lowers the output harmonic distortions compared with the conventional sinusoidal PWM inverter. The field oriented control using space vector modulation allows easy implementation of the BLDC drive with fewer harmonic. The advantages of the proposed drive are confirmed by the simulation results.

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