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# Implementation of Counter Using Low Power Overlap Based Pulsed Flip Flop

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*Abstract*

***The state machine elements are major power consuming component in VLSI system. The power reduction of these element leads to reduction of global power consumption of VLSI system. In this paper, we propose implementation of Counter using Low power Overlap based Pulsed Flip Flop and observed the power reduction compared with conventional flip flop designs. The proposed counter shows power reduction of 46.6%, 20.6% and 57.8% when compared to counters implemented with Semi-dynamic Flip Flop, Power Pc Flip Flop and Static flip-flop respectively. The performance comparison done in Mentor Graphics 10.2v with 0.5um technology.***

## I. INTRODUCTION

Technology and speed are always moving forward, from low scale integration to large scale integration. So, the system requires large number of components. In order to reduce the no of components we are using flip-flops. In this paper, we propose Low power Overlap based Pulsed Flip Flop.

Here our intension is to implement counter using Toggle flip-flops, because implementation of counter with these flip-flops will not require any additional hardware. The Data flip-flops having extensive developments from literature [1] to [4], as toggle flip flop can be obtained from data flip-flop with additional XOR gate, the proposed flip-flop with embedded logic is chosen. Also D flip-flop with Qbar terminal feed backed to Din can be used to implement counter but this implementation suffers with charge sharing problem.

## II. FLIP FLOP ARCHITECTURES

The master-slave designs, such as the transmission gate based master-slave flip-flop, PowerPC 603 master-slave latch dissipate comparatively lower power and have a low clock-to-output (CLK-Q) delay. PowerPC 603 is one ofthe most efficient classic static structures. It has the advantages of having a low-power keeper structure and a low latency direct path. The large D-Q delay resultingfrom the positive setup time is one of the disadvantages of this design. Also, the large data and CLK node capacitances make the design inferior in performance. The implementation of Power Pc flip-flop is shown in figure 2.1.

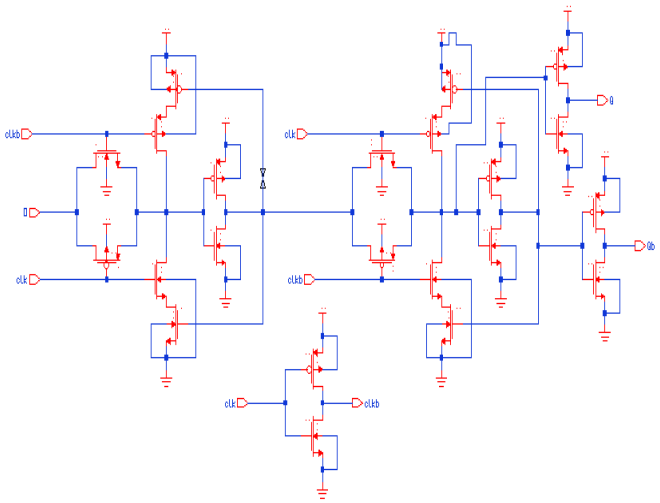

Fig 2.1: Power Pc Flip Flop

The second category of the flip-flop design, the dynamic flip-flops includes the modern high performance flip-flops. There are purely dynamic designs as well as pseudo-dynamic structures. The latter, which has an internal pre-charge structure and a static output, deserves special attention because of their distinctive performance

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improvements. They are called the semi-dynamic or hybrid structures, because they consist of a dynamic frontend and a static output. SDFF fall under this category. They benefit from the CLK overlap to perform the latching operation. SDFF is the fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large pre-charge capacitance. Semi dynamic flip-flop (SDFF) is considered as classic high performance flip-flop, combines the merits of static and dynamic structures in hybrid architecture. In SDFF, only one transistor driven by the data input greatly helps to reduce pipeline overhead. The major sources of power dissipation in the conventional semi-dynamic designs are the redundant data transitions and large pre-charge capacitance. Many attempts have been made to reduce the redundant data transitions in the flip-flops. The major advantage of the SDFF is the capability to incorporate complex logic functions efficiently. The efficiency in terms of speed and area comes from the fact that an *N*-input function can be realized in a positive edge triggered structure using a pull-down network (PDN) consisting of *N* transistors. This embedded structure offers a very fast and small implementation. Although SDFF is capable of offering efficiency in terms of speed and area, it is not a good solution as far as power consumption is concerned. SDFF has a fast non inverting output and a slow inverting output. The implementation of Semi Dynamic flip-flop is shown in figure 2.2.

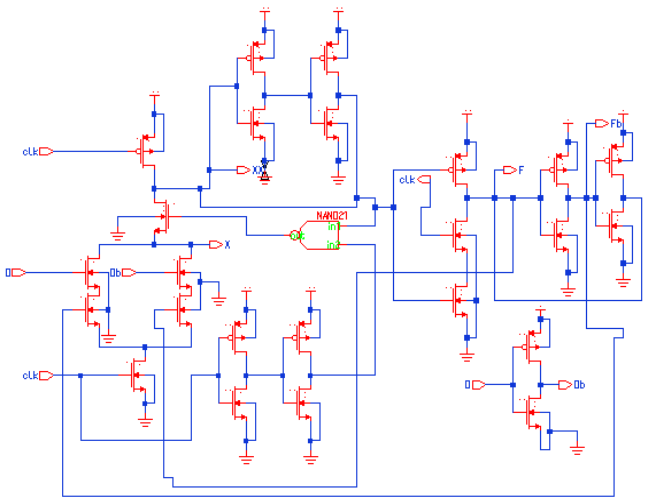


Fig2.2: Semi Dynamic Flip Flop

As clock clock-bar overlapping is major problem in conventional Dynamic flip-flops, Aflip-flop architecture that can operated with single clock is proposed, called True Single Phase Clock flip-flop (TSPC). The circuit consists of alternating stages called n-blocks and p-blocks and each block is being driven by the same clock signal. This latch was constructed by merging two parts consisting of CMOS Domino and CMOS NORA logic. There are several benefits with this flip-flop such as elimination of skew due to different clock phases and significant saving in chip area. The implementation of True single phase flip-flop is shown in figure 2.3.

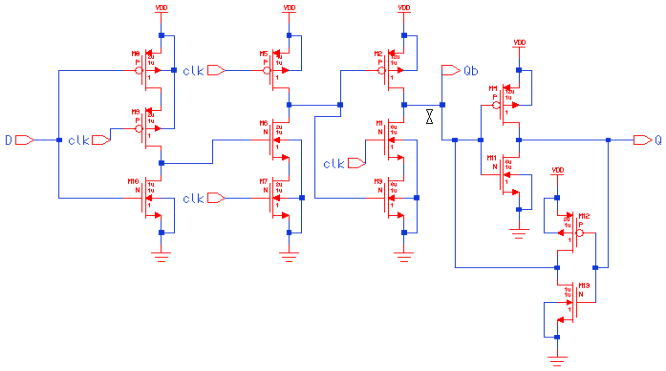


Fig 2.3: True Single Phase Clock Flip Flop

## III. PROPOSED ARCHITECTURE

The proposed flip-flop is a data flip-flop with an embedded pull down network of XOR gate attached to it, to obtain a toggle flip flop operation. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the pre-charge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. The proposed Overlap based Pulsed Flip Flop implementation is shown in figure 3.1.

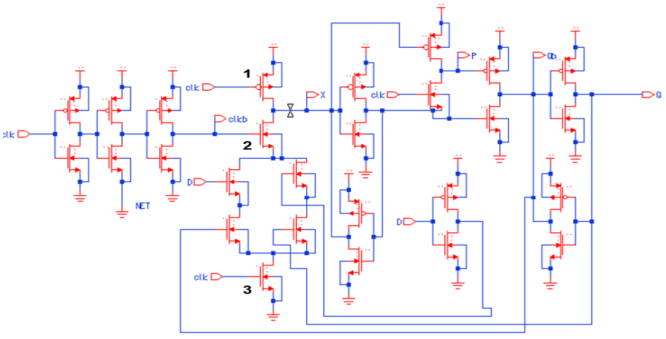


Fig 3.1: Proposed Toggle Flip Flop

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The operation of flip-flop relays on the overlapping of clock and clock bar signals. To enhance the overlapping period in the circuit three inverters are connected instead one inverter. Here the transistors 1&3 implements dynamic logic in which pair of PMOS and NMOS are used to avoid the direct short between power rails i.e, Vdd and ground.

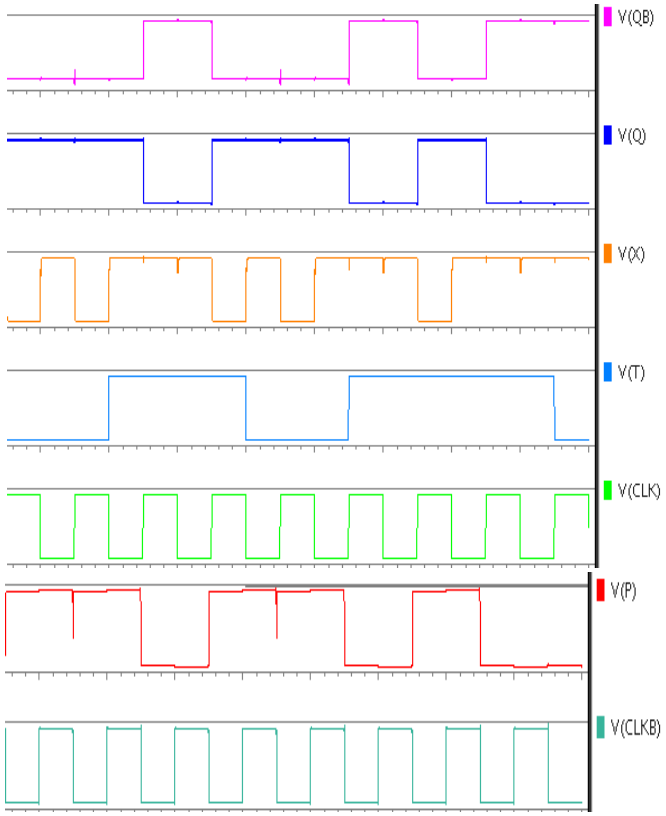


Fig 3.2: Proposed Flip Flop output waveforms

The transistors 2&3 implements overlapping logic to latch the input D value at the rising edge of clock. The transistors present between 1&2 and implementing pull down network of the XOR gate, applied with D, Dbar, Q, Qbar converts the data flip-flop into toggle flip-flop. The circuit analysis is as follows. When clock is equal to zero then transistor1 will be ON and hence pre-charge occurs to the node X to logic high. The transistor2 will be in OFF state so no logic may be evaluated. When clock is equal to 1 transistor1 forced to OFF condition to allow logic evolution but transistor2 is in OFF state to avoid logic evolution.Therefore the circuit may not take any input in clock low and high periods. In these conditions the leakage current decides the power dissipation. If we consider transition from high to low initially clock is in high state so transistors 1&2 are in OFF state and 3 in ON state, no logic evaluation takes place, whenever the clock transition occurs immediately the transistor1 ON and transistor3 OFF to initiate pre-charge period and transistor2 is in OFF state during over lap period due to clock to clock bar delay, to avoidlogic evaluation. Considering rising edge of clock or low to high transition, Initially clock is at logic low level hence the circuit is in pre-charge condition, whenever transition occurs,immediately transistors 1&2 change their state but the transistor2 remains in its previous state for short duration of time due to inverter delay in that period the transistors 2&3 are in ON condition to allow the XOR logic to be evaluated and effect the voltage at the node X. During evaluation period the value present at X may be remained at logic high or discharged to zero depending on input D and previous input or present output Q. In the waveforms shown the voltage waveforms X to be at logic high value whenever the clock input is at logic low and the X value alters only at some instances of clock low to high transition the value present at X made to retained by bi-stable element employed by two back to back connected inverters. The hold value of X latched to output state through inverter operated by the clock input. During or after evaluation period the clock will be at logic high to allow X or Xbar signal to output latch.If we observe the voltage waveform at node P the voltage level of P updated at rising edge of clock and it holds the same value up to the next rising edge as it becomes floating node during clock low period. Here to implement toggle flip flop Q,Qbar outputs are feed backed to input X or pull down so that the output toggles if at all input is given a logic high value for every clock cycle . If the waveforms are observed,during first rising edge of clock the input is applied at T (D in the circuit) is at logic low and output Q is at logic high and the XNOR of these two is logic low evaluated to node X.Since value at X is logic low the node P is changed to logic high to maintain Q&Qbar at same previous values. In case of second rising edge input T and feed back Q both are at logic high to produce logic high value at X which causes node P to

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discharge to logic low hence the output Q and Qbar toggled.

## IV. COUNTER IMPLEMENTATION

The conventional counter is a digital electronic device which measures the frequency of an input signal. It may also have been designed to perform related basic measurements including the period of the input signal, ratio of the frequency of two input signals, time interval between two events and totalizing a specific group of events. Figure 4.1 shows the implementation of four bit asynchronous counter.

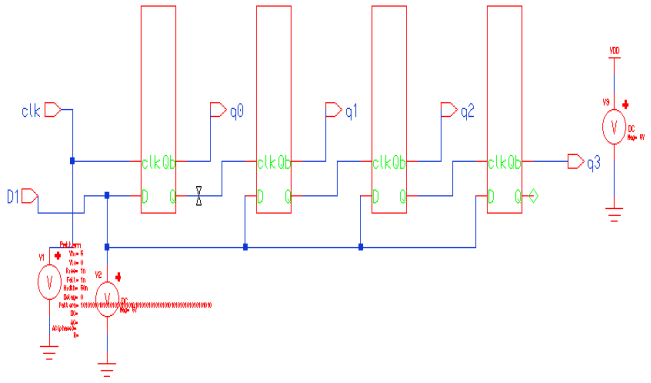


Fig 4.1: Four bit counter implementation

There is a great variety of counter based on its construction.

- Clock: Synchronous or Asynchronous
- Clock Trigger: Positive edged or Negative edged
- Counts: Binary, Decade
- Count Direction: Up, Down, or Up/Down
- Flip-flops: JK or T or D

Counters are classified according to the way they are clocked. In asynchronous counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by output of the preceding flip-flop. In synchronous counters, the clock input is connected to all of the flip-flop so that they are clocked simultaneously.Synchronous and asynchronous circuits have their own advantages and disadvantages. In a synchronous circuit, all the bits in the count change synchronously with the assertion of the clock. In an asynchronous circuit, all the bits in the count do not all change at the same time.

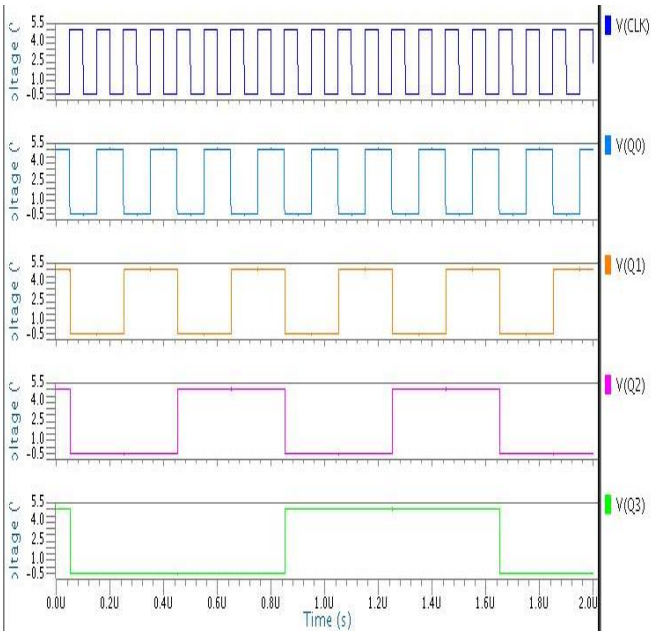


Fig 4.2: Implemented 4 bit Counter Waveforms

In synchronous circuit clock signal drives more number of transistors, results in more switching power consumption. But the requirement here is, low power delay product.Figure 4.2 shows the output waveforms of implemented four bit binary counter showing count from 0 to 15.

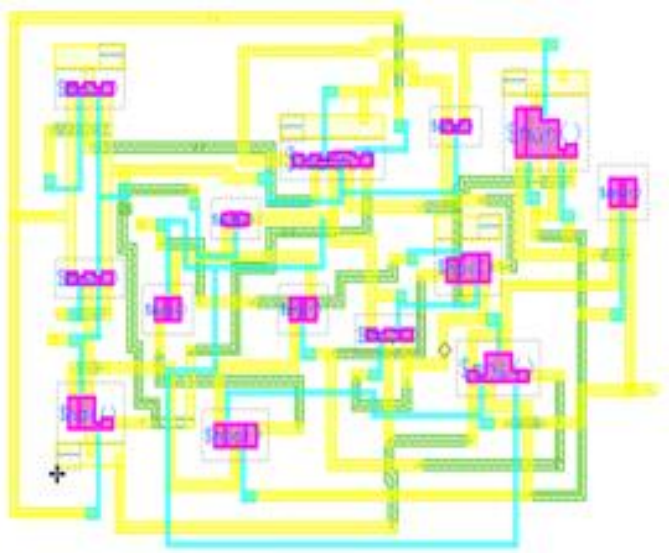

Fig 4.3: Layout of Proposed Flip Flop

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Table 5.1: Performance Comparison of Flip Flops

| Flip Flop | No.of Transistors | clk Driving Transistors | Data Driving Transistors | Power(P Watts) | Output rise time(P sec) | clock to Q Delay(P sec) | EDP(10^-24) |
|---|---|---|---|---|---|---|---|
| ptff | 27 | 5 | 3 | 272.012 | 156.31 | -749.8256 | 42518.19572 |
| sdff | 28 | 3 | 3 | 297.1007 | 490.92 | -603.4115 | 145852.6756 |
| power pc | 24 | 10 | 0 | 322.6059 | 192.29 | -373.2826 | 62033.88851 |
| Static tff | 38 | 6 | 4 | 353.1131 | 1428.3 | -355.75 | 504351.4407 |
| tspc | 13 | 4 | 2 | 163.2669 | 163.53 | -352.9259 | 26699.03616 |

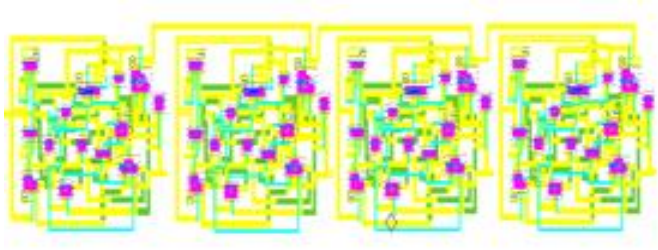

Fig 4.4: Layout of implemented Four bit Count.

Most often, Layout of the VLSI circuits Drawn manually to get most possible compact circuit layout. Figure 4.3 and Figure 4.4 shows the Hand Drawn layouts of proposed flip-flop and implemented counter respectively.

## V. PERFORMANCE ANALYSYS

Design metrics Area, Delay and Power decides the performance of a flip-flop. The readings obtained from tool are tabulated in TABLE 5.1 and TABLE 5.2

Table 5.2: Performance Comparison of Counters

| Flip Flop | Power | Output rise time(P sec) | | | |
|---|---|---|---|---|---|
| | | Q0 | Q1 | Q2 | Q3 |
| ptff | 1.0200N | 548.7 | 513.29 | 510.93 | 480.35 |
| sdff | 1.9109N | 374.64 | 376.39 | 376.66 | 300.65 |
| power pc | 1.2830N | 156.85 | 156.16 | 154.7 | 155.52 |
| Static tff | 1.6104N | 1420.7 | 1435.1 | 1447.5 | 1498.2 |
| tspc | 5.2009M | 289.29 | 246.48 | 257.76 | 144.03 |

The CMOS static flip-flop occupies more area when compared to other flip-flops, Requiring 38 transistors. Though the advancement in VLSI reached the saturation level to decrease the transistor size up to 13nm so we no need to bother about transistors but the increase in number of transistors makes the routing network more complex. Alongside, number of transistors driven by clock and data inputs are of more interest. The more data driving transistors provide pipeline overhead. More number of clock driving transistors responsible for switching power consumption. Figure 5.1 shows the Comparison of Flip-flop Architectures where static flip-flop suffers with requirement of more number of transistors and more data driving transistors. Power Pc suffers with more number of clock driving transistors. The proposed flip-flop architecture is optimum in all respects.

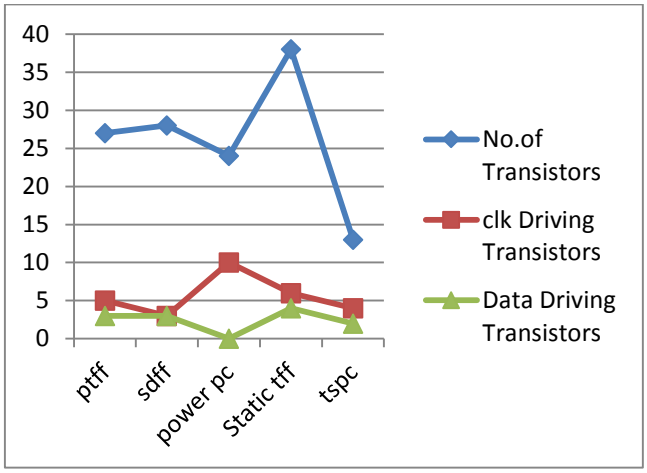


Fig 5.1: Comparison of Flip-flop Architectures

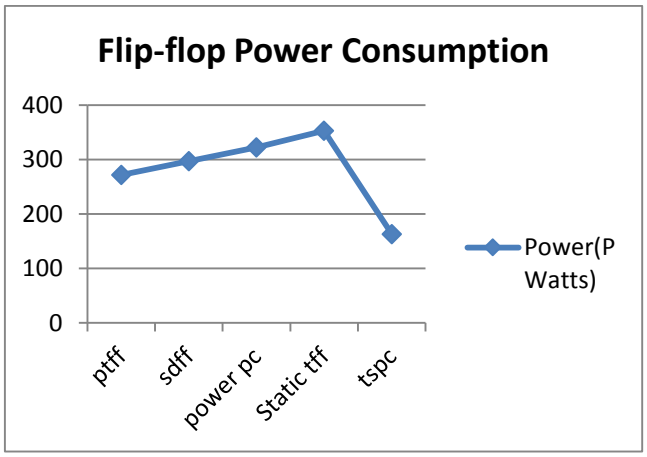


Fig 5.2: Comparison of power consumed by flip-flops in Peco Watt.

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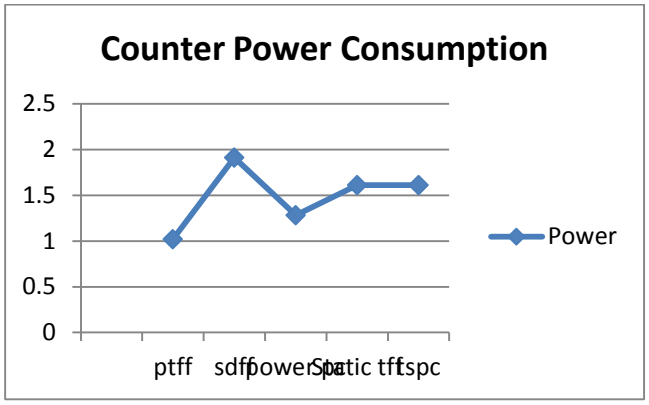


Fig 5.3: Comparison of power consumed counters in Nano Watt.

In the implemented flip flops, toggle flip-flop operation for the proposed PTFF and SDFF is obtained with embedded logic i.e., D flip-flop with XOR pull down network. For The power pc and TSPC flip-flops obtained by feed backing inverted output to the input. In case of PTFF feed backed output is XORed with input. The Static flip-flop is a conventional CMOS technology implementation of toggle flip flop. As shown in Figure 5.2,Comparatively the proposed flip-flop consumes less power which is 29.8% less than conventional static flip-flop. In the same way counter implemented with proposed flip-flop consumes less power which is 57.8%less than conventional static flip-flop as shown in Figure 5.3. The TSPC flip-flop seems to be consuming very less power individually but in the counter implementation it consumes significant amount of power. The clock to Q delay taken gives the propagation delay of flip-flop, also rise times of the outputs mentioned to know the effect of flip-flop on the driving circuit as the transition time determines the switching power consumption in VLSI circuits.

## VI. CONCLUSION

A Four bit Counter implemented using Low power Overlap based Pulsed Flip Flop and Compared it withCounters implemented using well known flip flop architectures and found that proposed design consumes less power and outputs less Delay. The % decrease in energy delay Product when compared to Semi Dynamic Flip Flop is 46.6%, Power Pc flip-flop is 20.4% and Static flip-flop is 36.6%Also layout is drawn for the proposed architecture.

## References

[1] KalarikkalAbsel, Lijo Manuel and R. K. Kavitha, Low Power Dual Dynamic Node Pulsed Hybrid Flip Flop Featuring Efficient Embedded Logic, IEEE Transactions on Very Large Scale Integration Systems, vol. 21,2013.

[2] Vladimir Stojanovic and Vojin G. Oklobdzija, Comparative Analysis of Master–Slave Latches and Flip-Flops, IEEE Journal Of Solid-State Circuits, Vol. 34, No. 4, April 1999.

[3] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2003.

[4] Fabian Klass, Semi-Dynamic and Dynamic Flip-FLops with Embedded Logic, Symposium on VLSl Circuits Digest of Technical Papers,1998.

[5] Fundamentals of the Electronic Counters, Hewlett-Packard Company Copyright © 1997.

[6] YongshengGao, Lecture notes, Floyd, Digital Fundamental.

[7] Siva Narendra, Vivek De, ShekharBorkar,Full-Chip Sub threshold Leakage Power Prediction and Reduction Techniques for Sub-0.18-um CMOS, IEEE Journal Of Solid-State Circuits, Vol. 39, No. 2, February 2004.

[8] Hassan Mostafa, M. Anis, M. Elmasry, Comparative Analysis of Timing Yield Improvement under Process Variations of Flip-Flops Circuits, IEEE Computer Society Annual Symposium on VLSI, 2009.

[9] MounirZid, Carlo Pistritto, RachedTourki, Alberto Scandurra, A New N-Fold Flip-Flop With Output Enable, International Journal of Embedded Systems and Applications (IJESA) Vol.3, No.2, June 2013.

[10] SoheilZiabakhsh, MeysamZoghi, Design of a Low-Power High-Speed T-Flip-Flop Using the Gate-Diffusion Input Technique, 17th Telecommunications forum TELFOR 2009.

[11] C. H. (Kees) van Berkel, Mark B. Josephs, and Steven M. Nowick, Scanning the Technology:

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Applications of Asynchronous Circuits, Version September 9, 1998: Proceedings Of TheIeee, Vol. Xx, No. Y, December 1998.

[12] J. Yuan and C. Svensson, New single-clock CMOS latches and flipflops with improved speed and power savings,IEEE J. Solid-State Circuits, vol. 32, no. 1, pp. 62–69, Jan. 1997.

[13] A. Hirata, K. Nakanishi, M. Nozoe, and A. Miyoshi, The cross chargecontrol flip-flop: A low-power and high-speed flip-flop suitable for mobile application SoCs, in Proc. Symp. VLSI Circuits Dig. Tech.Papers, Jun. 2005, pp. 306–307.

[14] G. Gerosa, S. Gary, C. Dietz, P. Dac, K. Hoover, J. Alvarez, H. Sanchez, P. Ippolito, N. Tai, S. Litch, J. Eno, J. Golab, N. Vanderschaaf, and J. Kahle, A 2.2 W, 80 MHz superscalar RISC microprocessor, IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1440–1452, Dec. 1994.

[15] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, Conditional-capture flip-flop forstatistical power reduction,IEEE J. Solid-State Circuits, vol. 36, no. 8,pp. 1263–1271, Aug. 2001.

[16] N.Nedovic and V. G. Oklobdzija, Hybrid latch flip-flop with improvedpower efficiency, in Proc. Symp. Integr. Circuits Syst. Design, 2000, pp.211–215.

[17] P. Zhao, T. K. Darwish, and M. A. Bayoumi, High-performanceand low-power conditional discharge flip-flop,IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May2004.

[18] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y.Oowaki, Conditional data mapping flip-flops for low-power and highperformancesystems,IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[19] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani,Low-power single- and double-edge-triggered flip-flops for high-speedapplications,Proc. Inst. Elect. Eng. Circuits Devices Syst., vol. 152,no. 2, pp. 118–122, Apr. 2005.

[20] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, Ultra lowpowerclocking scheme using energy recovery and clock gating,IEEETrans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44,Jan. 2009.