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Fault Tolerent Encoder and Decoder Design with Parallel Operation

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ABSTRACT:

Error detection and correction or error control are techniques that enable reliable delivery of digital data over unreliable communication channels (or storage medium. Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Error correction is the detection of errors and reconstruction of the original, error-free data. A novel and efficient VLSI architecture is proposed and implemented for the fault secure memory. The VLSI architecture has been authored in Verilog code for fault secure encoder and decoder for memory and its synthesis was done with Xilinx XST.

I.INTRODUCTION:

Field Programmable Gate Arrays (FPGA) is well known devices concerning reconfigurable hardware. FPGAs consist of an array of programmable logic blocks surrounded by a programmable routing fabric that allows blocks to be programmably interconnected. The array is surrounded by programmable input/output blocks that connect the chip to the outside world.

Every FPGA relies on an underlying programming technology that is used to control the programmable switches that give FPGAs their programmability. SRAM-based FPGA devices are steadily becoming the most suitable platform for implementing modern embedded applications due to their high re-configurability, low cost and availability. Static memory cells are the basis for SRAM programming technology which are distributed throughout the FPGA to provide configurability.

The re-programmability feature of SRAM leads to high logic density in terms of SRAM memory cells. Due to high logic density in terms of SRAM memory cells, SRAM based FPGA's are sensitive to radiation and require protection to work in harsh environments. Due to the increasing integration density FPGA chips are getting more prone to faulty behavior caused by cosmic or artificial radiation. Such faults are modeled as Single Event Upsets (SEU s) or Transient faults.

II.RELATED WORK:

The protection of digital filters has been wide studied. as an example, fault-tolerant implementations supported the employment of residue range systems or arithmetic codes are proposed[7], [8]. The employment of reduced exactness replication or word-level protection has been conjointly studied[9], [10].

Another choice to perform error correction is to use 2 totally different filter implementations in parallel [11]. All those techniques specialize in the protection of one filter. The protection of parallel filters has solely been recently thought-about. In [12], associate initial technique to shield 2 parallel filters was planned. This theme was generalized in[13],

wherever the employment of a theme supported ECCs was given. During this work, every filter was treated as a trifle on associate code, and extra filters area unit additional to act as verification bits. this suggests that, for single error correction, {the range|theamount|the quantity} of redundant filters required is that the same because the number of bits required in an exceedingly ancient single error correction overacting code[14]. as an example, for four parallel filters, 3 redundant filters area unit needed, whereas for eight filters, four redundant filters area unit required. This theme so considerably reduces the implementation price compared therewith of TMR.

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III.IMPLEMENTATION

3.1 FAULT-TOLERENT MEMORY SYSTEM OVERVIEW

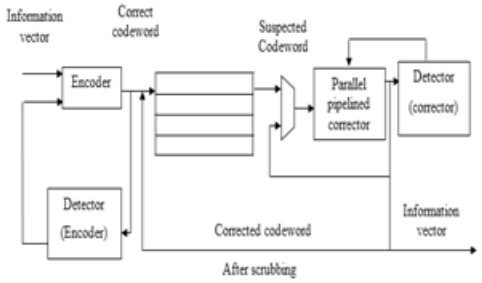

FIG 1.block diagram

3.2. Encoder:

An -bit codeword, that encodes a -bit info vector is generated by multiplying the -bit info vector with a bit generator matrix.

Fig2: Generator matrix for the (15, 7, 5) EG-LDPC in systematic format.

Fig.2 shows the systematic generator matrix to get (15, 7, 5) EG-LDPC code. The encoded vector consists of bits followed by parity bits, wherever every bit is just an real of vector and a column of from . Fig. three shows the encoder circuit to cipher the parity bits of the (15, 7, 5) EG-LDPC.

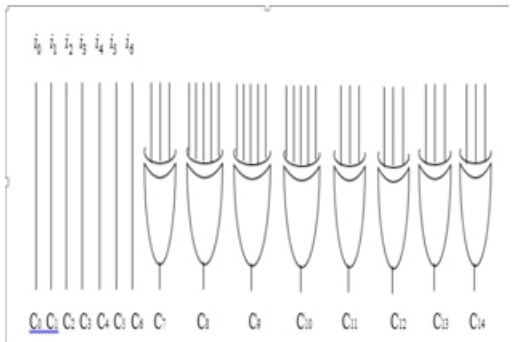

FIG 3: Structure of an encoder circuit for the (15, 7, 5) EG-LDPC code

3.3 Corrector:

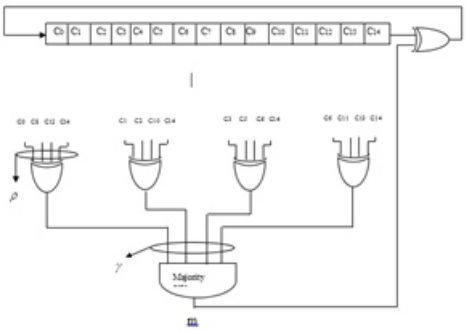

Fig 4 corrector implementation

This technique consists of 2 parts:

1) Generating a particular set of linear sums of the received vector bits and

2) Finding the bulk worth of the computed linear sums.

The majority worth indicates the correctness of the code-bit beneath consideration; if the bulk worth is one, the bit is inverted, otherwise it's unbroken unchanged. The speculation behind the one cycle majority corrector and also the proof that EG-LDPC codes have this property area unit accessible in [1]. Here we have a tendency to summary the structure of such correctors for EG-LDPC codes.

IV.RESULTS

Encoder

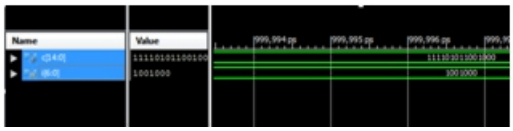

Fig 4: encoder resultant

As the input is 1001000 the encoder resultants the 11101011001000.

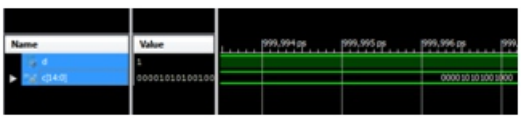

Fig 5 : detector

Syndrome detector detects the resultant as zero when no error and one when error exists

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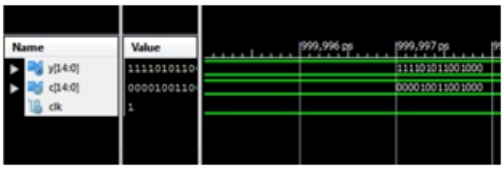

Fig 6 corrector

Corrects the bits in the input vector given. Using parallel corrector.

CONCLUSION:

Xilinx implementations of fault secure encoder and decoder for memory applications. Using this architecture tolerates transient faults bothin the storage unit and in the supporting logic (i.e., encoder, decoder (corrector),and detector circuitries).The main advantage of the proposed architecture is using this detect-and-repeat technique we can correct potential transient errors in the encoder or corrector output and provide fault-tolerant memory system with fault-tolerant supporting circuitry.

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