ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Novel Pipelined Vedic Multiplier Constituted With Reversible Logic

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ABSTRACT

Multiplication is an important element in different applications like DSP, DIP, communication and etc. Vedic Mathematics is prominent approach by that many mathematical challenges came across in present conditions.In our design rather than traditional methods different methods will be introduced 1) In our propose method Vedic multiplier based on UrdhwaTiryakbyamSutra , which can be faster multiplication in present all designs 2) for the designing of the proposed algorithms we uses the reversible logic. This can reduce the junction temperature and also the power compared with the irreversible logic.

INTRODUCTION

From the past decay the different advance multiplication method like Booth's and modified Booth's algorithm and are proposed. Even though in present DSP and other application the fast multiplication is not suitably advised. There are three steps in multiplication like partial product generation, redundant addition and final addition. Not only area wise but operation wise also redundant addition place important role in multiplication.

To achieve the performance improvement with refer to speed of the method mentioned above, [5] and [6] explored a novel method of multiplier design by ancient Vedic Mathematics. This Vedic mathematics is give gift of Indian sages with this many mathematical calculation can be done orally. This Vedic mathematics majorly depends on 16-sutras and their upa sutras. By using these we can performance the different calculations like Arithmetic, Geometry, Algebra, Geometry, Analytical, Trigonometry, etc. this makes the researches are turned towards theVedicmathematic for fast operating application like Control Engineering, Signal Processing

This paper organizes as follows. In Section I deal with the introduction, followed by the session II that deals with introduction to reversible logic, Session III Vedic multiplicationmethod, session IV deals about proposed method, session V deals with Results and analysis of our architecture with the proposed technique and Section VI concludes the paper.

REVERSIBLE LOGIC

Generally,thesemultipliers can be designed using the irreversible gates like XOR, NAND and NOR etc. When this multipliersdesign with these gates generally the pervious bits will be erased and it stores the present values when each time input changes that causes the heat dissipation at the junction, in long run this causes the damage of system and may provide the wrong values

Reversibility Conditions

For the design of reversible gate it should satisfy the important conditions they are stated below

Condition 1

One to One correspondence between input and outputs, also known as "Bijective Conditions".

Condition 2

Each output function must be equal to 1 for its half of the inputs, known as "Balance Conditions".

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Condition 3

By inversing output, we must be able to reproduce mapped input called as "Dual" or "Inverse Conditions".

Reversible Logic Gates: Advantage

If the design is constructed using the reversible gates these are the features and advantages can be obtained and that are stated in table II. Not only above stated power calculations it also reduces the switching power of the transistor and intermediate power loss and moreover important the glitches are can be avoided efficiently.

For the designing the any circuit by using the reversible logic we need to considered the parameters that are described below.

1. Reversible logic gates do not allow fan-outs.
2. Reversible logic circuits should have minimum quantumcost.
3. The design can be optimized so as to produce minimum number of garbage outputs.
4. The reversible logic circuits must use minimum number ofconstant inputs.
5. The reversible logic circuits must use a minimum logicdepth or gate levels.

TABLE-1
Reversible logic advantages

Types of power loss	Reversible logic gate advantage
P_S Loss	Almost zero switching power dissipation can be obtained using the reversible gates in design
P_{SC} Loss	Short circuit power loss can be minimized by using the reversible logic gates even for adiabatic circuits
P_L Loss	Even tank capacitor leakage power also can be reduced for adiabatic reversible logic
P_{STATIC} Loss	Reversible MOS that inherently promises asymptotically-zero power consumption will minimizes the static power
Power Consumption Reduction	Reversible logic properties shows no bit loss during computation, unique output to input port mapping etc characteristics reduces the power consumption

Different design researches are going on the reduction of the below stated optimized parameters. For the improved and advanced design by using the reversible design considering of the many aspects that related to the basic needs of the reversible logic and that should also meet the requirements of the quantum technology

VEDIC MULTIPLICATION

Vedic sutras are derived from the traditional Indian Vedas. basic Vedic sutras is of 16 different types in that only two are used for the multiplication and more over the simple and best method of performing multiplication is urdhwatiryakbhyam sutra this name can be derived by the Vedic saints because the algorithm involves vertical and crosswise. The major aspect of designing multiplier with this sutra is, only with simple circuit also we can design the fast and efficient multiplier that are AND plane, FA and HA and the operation and the addition also independent to each other and more over pipeline operation also archived. The operation time also reduced.

Let us consider two 8 bit numbers X7-X0 and Y7-Y0, where 0 to 7 represent bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P0 to P15 represent each bit of the final computed product.

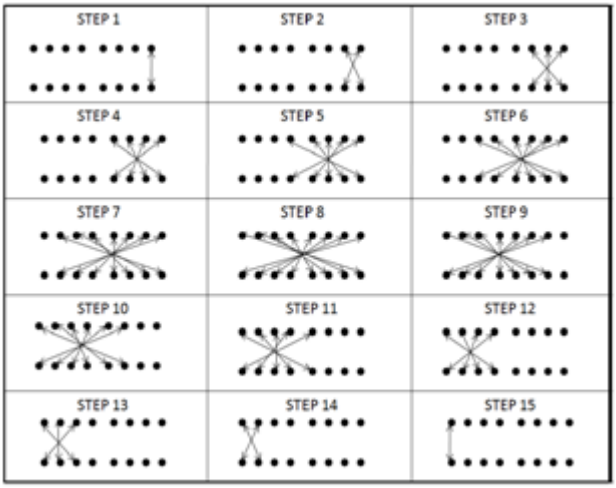

Fig1: step by step method of multiplying two 8 bit numbers using the UrdhwaTiryakbyamSutra.

It can be seen from equation (1) to (15), that P0 to P15 are calculated by adding partial products, which are

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calculated previously using the logical AND operation. The individual bits obtained from equations (1) to (15), in turn when concatenated produce the final product of multiplication which is depicted in (16).The carry bits generated during the calculation of the individual bits of the final product are represented from C1 to C30.

The carry bits generated in (14) and (15) are ignored since they are superfluous

P0 =A0 * B0 (1)

C1P1 = (A1 * B0) + (A0 * B1) (2)

C3C2P2 = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 (3)

C5C4P3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) +C2 (4)

C7C6P4 = (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) + (A0 * B4) + C3 + C4 (5)

C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) +(A1 * B4) + (A0 * B5) +C5 + C6 (6)

C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) +C7 + C8 (7)

C16C15C14P7 = (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) + (A2 * B5) + (A1 * B6) + (A0 * B7) +C9 + C11 (8)

C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 + C12 + C14 (9)

C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) + C13 +C15 +C17 (10)

C25C24C23P10 = (A7 * B3) +(A6 * B4) + (A5 * B5) + (A4 * B6) +(A3 * B7) + C16 + C18 + C20 (11)

C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 + C21 + C23 (12)

C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 +C26 (13)

C30P13= (A7 * B6) + (A6 * B7) + C25 + C27 + C28 (14)

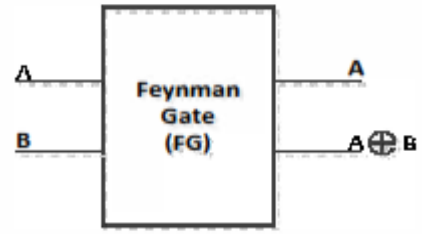
P14 = (A7 * B7) + C29 + C30 (15)

P15= (A7 * B7) (16)

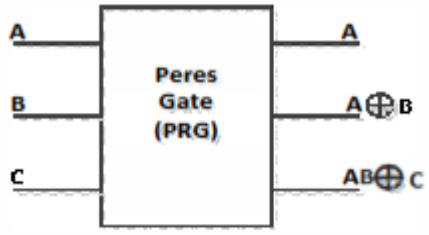
PROPOSED MULTIPLICATION

Rather than the traditional method we uses the pipelined addition can be used for the improvement in the delay. Hence the critical path delay can be reduced The staple reversible logic gates attained duringthe design is listed below:

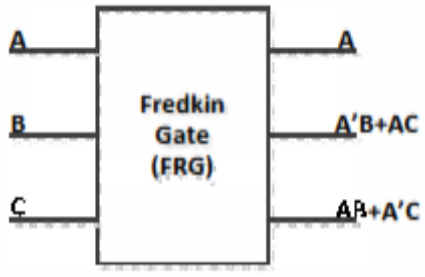
1. Feynman Gate [5]:



2. Peres Gate [17]:



3. Fredkin Gate [16]:



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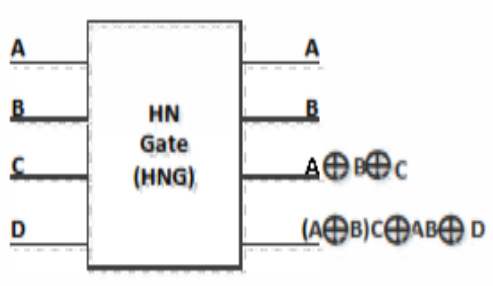
4. HNG Gate[7]:



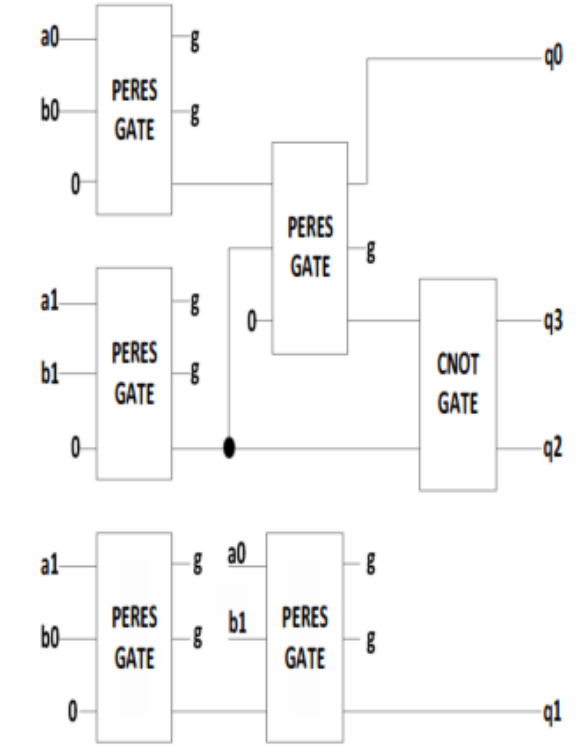


Fig2: reversible implementation of 2x2 UR Multiplier

Pipelining technique employed for the addition of the internal products generated by the reversible gate based on UrdhwaTiryakbyam.

- P0 = x0.y0.
- P1 = x1.y0 +x0.y1.
- P2 = x2.y0+x1.y1+x0.y2+P1 [1].
- P3 = x3.y0+x2.y1+x1.y2+x0.y3+P2 [2:1].
- P4 = x3.y1+x2.y2+x1.y3+P3 [2:1].
- P5 = x3.y2+x2.y3+P4 [2:1].
- P6 = x3.y3+P5 [2:1].
- P7 = p6 [2:1]

RESULTS AND ANALYSIS

The design of the reversible 2x2, 4x4, 8x8, 16x16 and 32x32 multipliers designed using VERILOG HDL and logically verified using and MODELSIM.In our proposed method UrdhvaTiryakbhayam Vedic Multiplier designed using reversible logic gates. Principally we designed 2x2 UT multiplier and then 2x2 UT multiplier block is cascaded to acquire 4x4 multiplier. The ripple carry adders which were expected for adding the partial products were retraced using HNG gates.Thesimulation results are as shown in below fig.

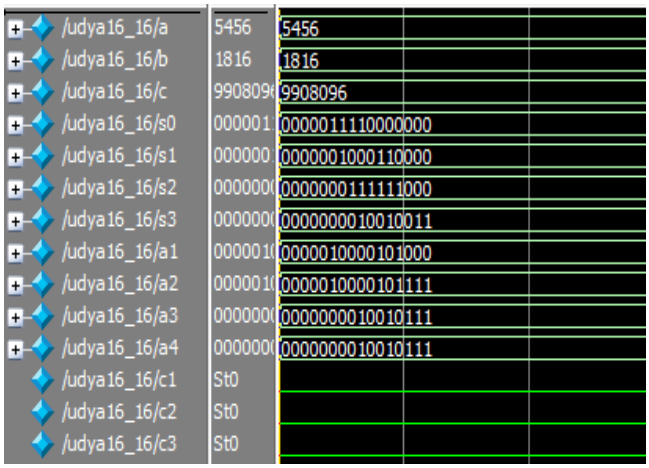


Fig3: simulation result of proposed UR Multiplier

We given the A=5456 and B=1816 in binary format and in that it spitted the upper part and lower part. Then 4 8 UT multiplier take the two part inputs respective to UT sutra and produces the 4 intermediate results s1,s2,s3,s4, then those intermediate sums added to produces the final results

CONCLUSION

The basic features that are related with the optimizing parameters of the reversible logic can be achieved by our proposed method. The pipelining can be adopted by our design hence the critical path delay also reduced. The proposed design has less number of gates and minimum number of ancilla inputs compared to all other designs studied. The quantum cost is better than pervious of the studied designs. Though our design garbage outputs are reduced they can be used out as fan outs for other gates.

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