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Advanced Unsigned Multiplier With Hasten Addition

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ABSTRACT:
In many applications the multiplier plays the vital role, but whereas for some application the area and the power is the important element for that reason some applications may uses the serial multiplications. Without considering the speed parameter as the major element even though the speed is important element the speed can be sacrifice for the small die size issues. For that applications the shift-add mechanism will be used preferably. In this concept the addition place important role refer to the speed and the area. For that reason the different addition methods were introduced and deep research also on going. As the part of that we introduce the novel methods for the addition which is suited for the above stated multiplier.

Key words: ***multiplier, serial multiplications, shifts-add mechanism.***

INTRODUCTION

Even in the present design methods the multiplication itself the critical concern there wise the many methods are introduces for the improvement in basic VLSI consideration. In traditional multiplication internally is the different staged compositor, namely partial product generation, multi-operand addition and final sum generation. In previous attempts different addition strategies and methods were introduces for the multiplier designing. After introduction of booth algorithms the multiplier designing can changed drastically. In general, a multiplier uses Booth's algorithm and array of full adders (FAs), or Wallace tree alternatively to array of FA's., i.e., in general multiplier mainly compose of the three parts: Booth encoder, compression tree for the partial product addition such as Wallace tree, and final sum adder. Because Wallace tree is the parallel addition to make faster processing, it is also related to the operation time proportionally. It uses the fact that counting the number of 1's among the inputs sickens the number of outputs into. In real execution, many counters are used to compress the number of outputs in each stage.

An efficient method for the increase of speed by limiting the partial product count, in general multiplication internal consists stages of additions of partial products. To reduce the internal calculation of addition levels for the partial products, It can be efficient where the addition methods like walles tree MBA algorithm has been applied for the increase in the speed to generation and addition of the partial products. Many parallel architecture are introduces the speed with MBA algorithm, many pipelined multiplication architectures works parallel have been researched. Among them, the design methods based on the Baugh–Wooley algorithm (BWA) have been developed and they have been applied to various digital filtering calculations.

But the major problem that is associated with these methods is the area. Even though these are speed in operation there are not suited for the smaller applications like nodal interconnections and the networks security which having the control points at remote place. In order th satisfy these types of the requirements we turned towards the shift-add multipliers

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MULTIPLACATION ALGORITHM

Let the product register size be 64 bits. Let the multiplicand registers size be 32 bits. Store the multiplier in the least significant half of the product register. Clear the most significant half of the product register. Repeat the following steps for 32 times:

1. If the least significant bit of the product register is "1" then add the multiplicand to the most significant half of the product register.
2. Shift the content of the product register one bit to the right (ignore the shifted-out bit.)
3. Shift-in the carry bit into the most significant bit of the product register.

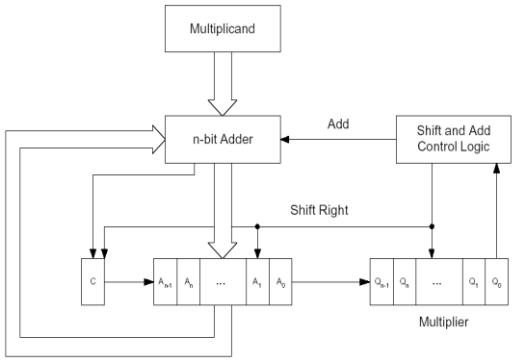

Fig.1. Block Diagram for Such a Multiplier.

From the above diagram two registers were used for storing the multiplier and multiplicand respectively. Adder for the addition based on the add command that initiated by the control logic, and one more register used for the temporary result storage for the next addition.

The design was implemented as a finite state machine with states and transition logic as shown in Fig 2. The Start signal transitions the state machine out of the idle state and into the initialize state whereby it commands the multiplicand and multiplier to be loaded into registers. Once loaded, the state machine goes through a series of test and shift, or test, add and shift operations depending on the status of the LSB bit. Upon reaching the maximum count for the multiplication cycle, the state machine goes back to the idle state and outputs a Stop signal

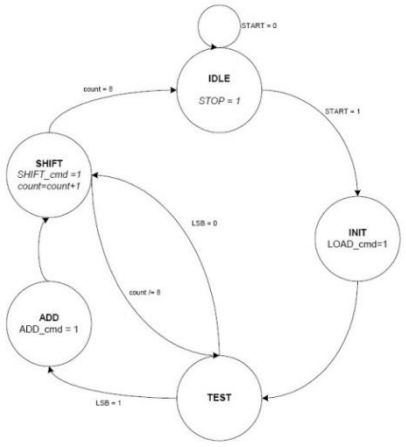

Fig.2. state diagram of the control unit

Introduction to the addition methods

Normal Carry-Select Adders

In normal CSA, total bit length will be number of sub bits for each sub bit block the group of full-adders are used. Where two group of full adder will be used for each sub bit block by giving constant carry for each group of full adder i.e '1' for one set and '0' for another set.

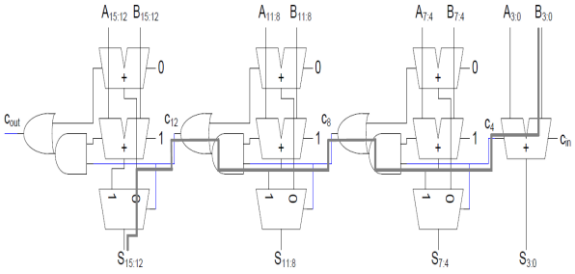

Fig.3. Normal Carry-Select Adder

The major problem with this design the time taken for selection will be high because each operated at same time and same speed.

In order to reduce that waiting time we introduces the new concept called squire root carry select adder.

Regular SQRT CSLA Architecture

The structure of the 16-b regular SQRT CSLA is shown in Fig. It has five groups of different size RCA.

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From the structure of CSLA, it is evident that there is scope for reducing area and power consumption

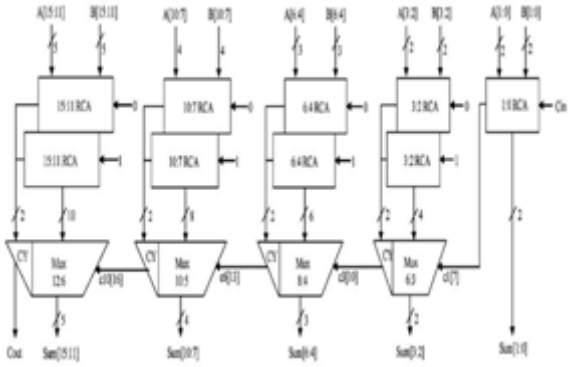

Fig.4. Regular SQRT CSLA architecture

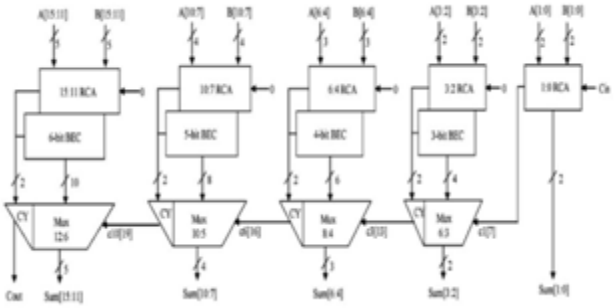

Fig.5. modified BEC SQRT CSLA architecture

In Regular SQRT CSLA also we made the important extension made for the effective area reduction by introducing the BEC (binary to excesss-1 method). In this, as we know for any carry select adder we uses the two sets of full adders there by increases the area in orders to reduce this effect this BEC method used.
As shown in fig.5 we replace one set of full adder are replaced by the BEC, as normal the block of full adders with default carry '0' will perform the it convention operation as that give as the input for the BEC it gives one added output. Based on the previous carry any one output will be selected.

Advanced self checking for the adder

In this we introduce the one more important method of self-checking property for the adder. As we know in present advanced VLSI testing places the important role that can be achieve by adopting the self-checking property.

This can be applied only for this type of adders only because two set of outputs are able to see at the same instant. In previous methods there were used self-checking for the only single full adder structures only but we are applying for the group structures.

For that we use the concept called two-pair two-rail checker. In this at each instant the inputs of the each group of full adder structure will be considered along with the carry, there by the problem that associated by the previous methods refer to the two-pair two-rail checker method. In this block diagram it consists of the only gate as the elements there by no vary for area and power. And more over it is high efficient.

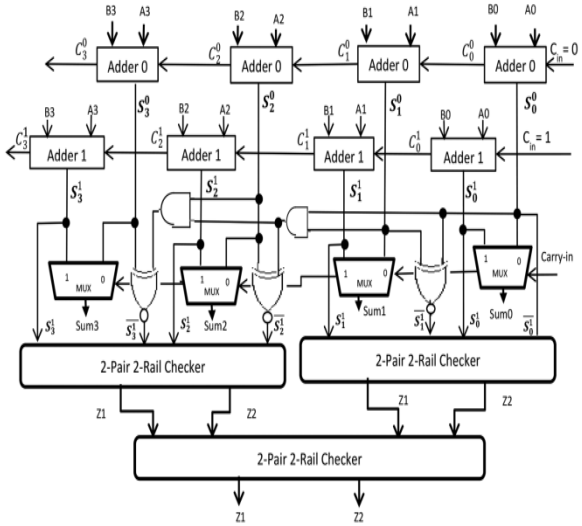

Fig.6. corrected each full adder structure design of self-testing carry-select adder with two rail encoding

RESULT AND DISCUSSION

As shown in below fig, it contains all the data that will be used as outputs of the module. From the timing diagram, it can be seen that once the LOAD_cmd is received, temp_register is loaded with the input byte .b_in., in this case 0x96. If the SHIFT_cmd is received without a prior ADD_cmd, the contents of temp_register will be logically shifted right.

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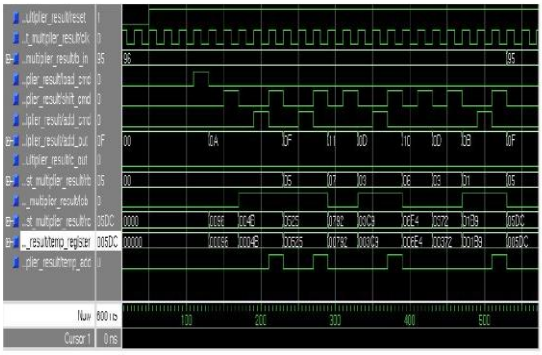

Fig.7. Simulation of proposed adder based multiplier

This can be seen on the next clock edge when 0x96 is shifted to become 0x4B. If the ADD_cmd is received prior to the SHIFT_cmd, the 8 to 16 bits of temp_register will be loaded with the .add_out. input byte and the register will be logically shifted right. This can be seen on the next clock edge when 0xA is loaded into temp_register which contains 0x4B.This changes temp_register to equal 0xA4B which gets shifted right to become 0x525 as shown in the timing diagram.

CONCLUSION

The above discussed adder are designed and that will compared with the proposed adder, which given the good statistics. Using this we designed the shift-add multiplier and the result are also verified. Area and power recent studies have demonstrated that redundant adders can be efficiently mapped on FPGA structures, reducing area overhead and improving speed.

REFERENCES

[1] D.P.Vasudevan,P.K.Lala,andJ.P. Parkerson, "Self-checking carry-select adder design based on two-rail encoding," IEEE Trans. Circuits Syst.I,Reg.Papers, vol. 54, no. 12, pp. 2696–2705, Dec. 2007.

[2] M. Alioto, G. Palumbo, and M. Poli, "Optimized design of parallel carry-select adders," Integration, the VLSI J., vol. 44, no. 1, pp. 62–74, Jan. 2011.

[3] H. Belgacem, K. Chiraz, and T. Rached, "A novel differential XOR-based self-checking adder," Int. J. Electron.,vol.99,no.9,pp.1239–1261, Apr. 2012.

[4] Y. S. Wang, M. H. Hsieh, J. C.-M. Li, and C. C.-P. Chen, "An at-speed test technique for high-speed high-order adder by a 6.4-GHz 64-bit domino adder example," IEEE Trans. Circuits Syst. I, Reg. Papers, vol.59, no. 8, pp. 1644–1655, Aug. 2012

[5] Muhammad Ali Akbar and Jeong-A Lee, Senior Member, IEEE "Self-Checking Carry-Select Adder Design Based on Two-Rail Encoding" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 61, No. 7, July 2014