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Development of Timer Core Based on 82C54 Using VHDL

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Abstract:

This paper proposes a new way to develop a timer based on 82C54 using VHDL. This timer can be used to define performance of AC motors that can be used in GFCs. Gravimetric Feeder Controllers (GFC)s are used in thermal power plants. Coding is done by using VHDL. The simulation tool that has been used here is Xilinx ISE 14.7 software. Firstly, all code for timer circuit was written in VHDL and then simulated. Finally, the required output waveforms were obtained. After the coding was completed, VHDL mapped on to a programmable logic device. Spartan 3A/3AN FPGA starter kit board is the programmable logic device used here. The timer code in VHDL was burnt on to a Spartan 3A/3AN FPGA starter kit board. After completion of that coding and burning method, output was observed on FPGA kit.

Keywords:

Timer, Very High Speed Integrated Circuit Hardware Description Language (VHDL), Field Programmable Gate Array (FPGA), Gravimetric Feeder Controller(GFC).

I.INTRODUCTION:

The chemical energy of the coal converts into electrical energy in a coal based thermal power plants. By railway, in wagons, coal is transported from coal mines to the power plant. There is no uniform size of coal from mines, so it is taken to crusher and crushed. Crushed coal is stored in raw coal bunker. For the grinding of coal, the mechanical device is used called pulverizer. The powdered coal is carried in coal pipes to the boiler, where the temperature of the boiler is 1300 degree centigrade. The water in the boiler tube is converted to steam. In boiler steam is separated from water.

Pulverized coal means a very fine powder will undergo combustion process in furnace and steam is generated by heating the water. In that furnace coal flow monitoring and control is important. This coal flow control is based on conveyor belt speed. Conveyor belt feeds the coal into pulverizer. The prime mover of the conveyor belt is a variable speed drive. Then that speed drive is a combination of AC motor and magnetic clutch. Thetachogenerator can measures the speed of the Ac motor. The output from the tachogenerator is an AC voltage and this AC signal is converted into pulses and becomes the input to timer. That timer had such a large number of uses in distinctive supplies. In that one is the Gravimetric Feeder Controllers (GFCs). In thermal power plants to control power generation we can use Gravimetric Feeder Controllers.

II.RELATED WORK:

The components of an embedded system can either be on the same chip or can be connected externally. Timer is a general and useful component. It is used to generate events at specific times. Timer measures the duration of specific events which are external to the processor. It is a programmable device. The general version of the timer is called a counter. It is used to count events in the form of pulses. It counts the number of occurrences. Timers have three general functions. 1) Keeping time and/or calculating the amount of time between events. 2) Counting the events themselves. 3) Generating baud rates for the serial port. Timer switches on or off for a fixed period of time. The time duration for which a timer has been set is termed the preset and is set. Time bases are typically 10 ms, 100 ms, 1 s, 10 sand 100 s. Thus a preset value of 5 with a time base of 100 ms is a time of 500 ms.The 82C54 was originally designed by as a solution to timing and counting problemsMotor encoder disks, also generate pulses and can be used to increment the 82C54's counters.

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Used in this manner, the 82C54 can count the number of motor rotations. The 82C54 is often called a timer chip, but technically, it is a counter chip. This chip has several versions (namely the 8253, 82C53, 8254 and 82C54). All versions have the same pins and functions. This 24-pin chip has 3 distinct blocks. The first consists of the counter output (OUT0, OUT1, OUT2), enable (GATE1, GATE2, GATE3) and input (CLK0, CLK1, CLK2) pins. Wire up the peripherals (like motors and switches) to these pins. The second block is the eight data lines D0-D7 in which computer's processor uses to transfer (reading and writing) data to and from the 82C54.The third block is the chip select (/CS), reading and writing (/WR and /RD) and mode select lines (A0 and A1).

III. PROPSED WORK:

A.Timer:

This timer has inputs like DATAIN bits of D0, D1, D2, D3, D4, D5, D6, D7. This timer can be used as timer as well as counter. So this timer consists of three counters in which of these three counters each can be selected by using selection lines like in case of multiplexers. Those are A0 and A1. Already we know that timers had in built clock so for that we are giving CLK0 for counter0, CLK1 for counter1 and CLK2 for counter2. For up counting purpose we are giving DR bit means direction as 0. RST bit is for reset the timer. LOAD bit is for loading whatever the data in bits into data out bits. Data out bits are the outputs of timer. Data out bits can be represented as DATAOUT0, DATAOUT 1 DATAOUT2 in which these three are 8-bit respectively. CTR0, CTR1, CTR2 are the three outputs of three counters. If we make use this timer, then wire up the

AC motor and other peripherals to the counter outputs. Then now AC motor rotation speed is taken by using Tachometer then that speed is in terms of Revolutions Per Minute (RPM). That RPM is converted into pulses by tachogenerator. These pulses can be given as input to timer. AC motor performance is calculated by observing that how many pulses having rising edges occurring in the fixed time period and how many time periods are occurring. By calculating these we can tell performance of AC motors. These AC motors are used in GFCs to rotate the weighing belt of weighing machine.This weighing machine measures the coal why coal wants to measure means according to output power requirement at Grid coal can be used so that is why we measures coal.

Sometimes means in Summer power requirement is high and in winter somewhat less. So power generation in Thermal power plants we can use GFCs containing this AC motor along with timer. Here the difference between the 82C54 timer and proposed timer is RDN, WRN with Read/write logic and control word register were not need. Mentioned above inputs and outputs are enough to define the performance of AC motor.

B.SOFTWARE IMPLEMENTATION-VHDL:

For synthesis and analysis of HDL designs, Xilinx produced a software tool called Xilinx ISE (Integrated Synthesis Environment).It enables the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, and configure the target device.ISE primary user interface is the Project Navigator, it includes the Sources, a source code editor called workplace, and processes.

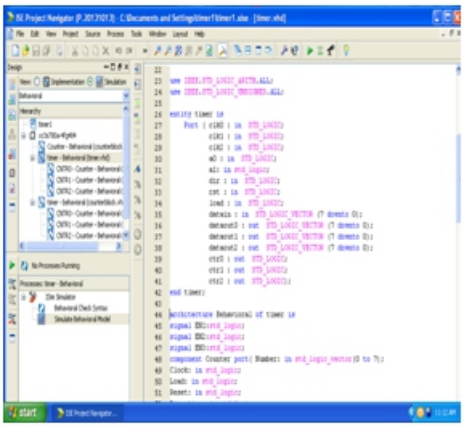
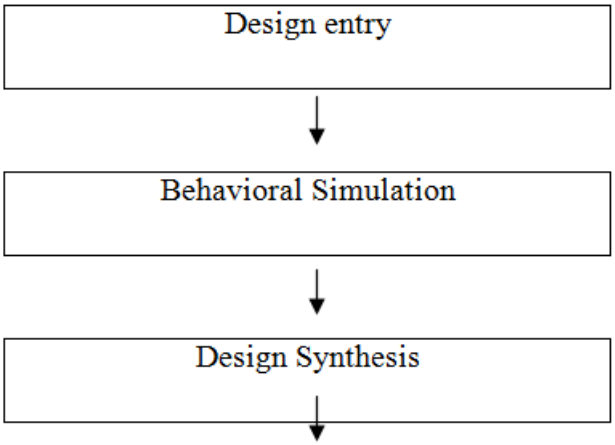


Fig 1: VHDL code compilation

C ISE DESIGN FLOW:



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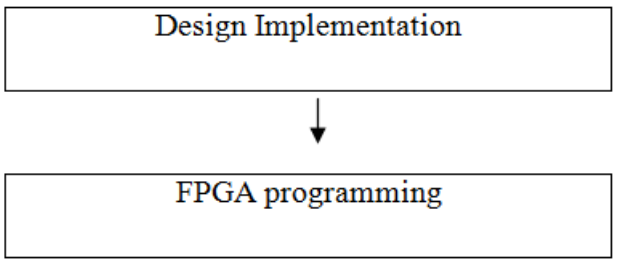

Fig 2: ISE Design Flow Chart.

Fig.2. shows ISE Design flow. The VHDL model uses some software tools to create actual digital circuits in a process known as synthesis. For describing and modeling a digital system at various levels and is an extremely complex language VHDL is intended.

IV. SIMULATION RESULTS:

The proposed timer code is written in VHDL by using Xilinx ISE 14.7 as software. The results are shown in following figures.

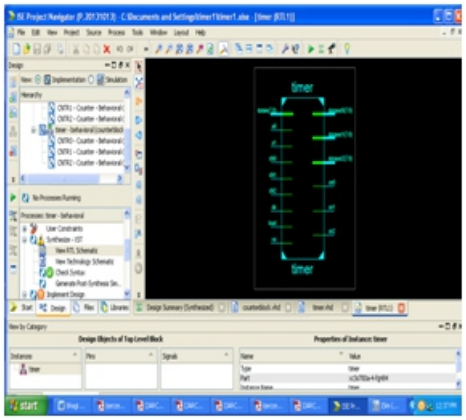

Fig 3: RTL view or VHDL synthesis of Timer

Firstly make the RST and LOAD bits to be set. After that give DATAIN bits (D0….D7) which are called data bits then we obtain DATAOUT0, DATAOUT1, DATAOUT2 as undefined because the reset (RST) initially is set.

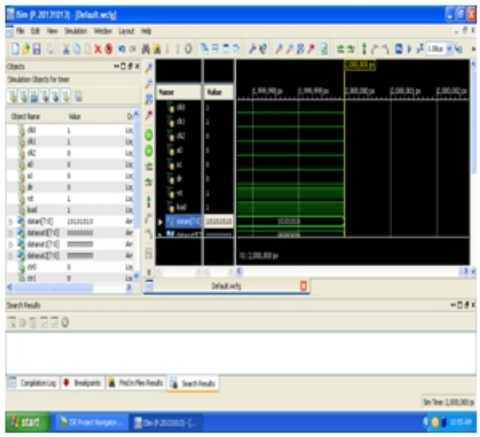

Fig 4: Simualtion result for loading Counter0 when RST is set.

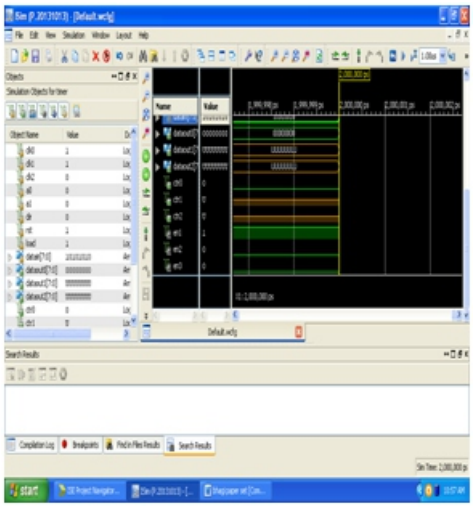

Fig 5: Simulation result for reading Counter0 when RST is set.

Then to observe whether the DATAIN becomes DATOUT0, DATAOUT1 and DATOUT2 first select one counter of the three counters by using selection or address bits A0, A1. If A0 and A1 bits are 00 then it considers Counter0.

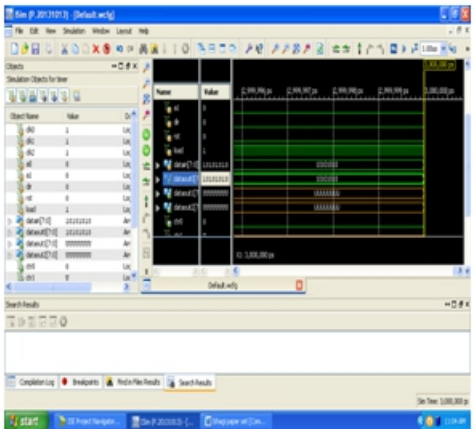

Fig 6: Simulation result for reading counter0 when RST is 0

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If A0 and A1 bits are 01 then it selects counter1.

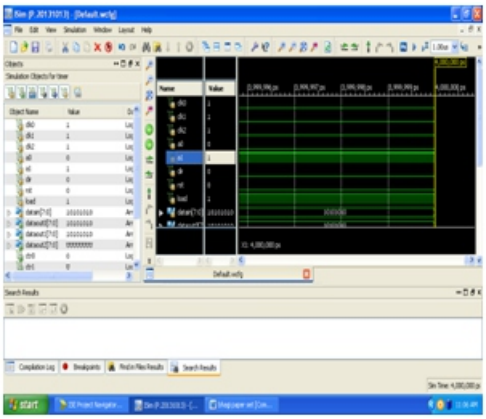

Fig 7: Simulation result for selecting counter1

If A0 and A1 bits are 10 then the counter2 is selected.

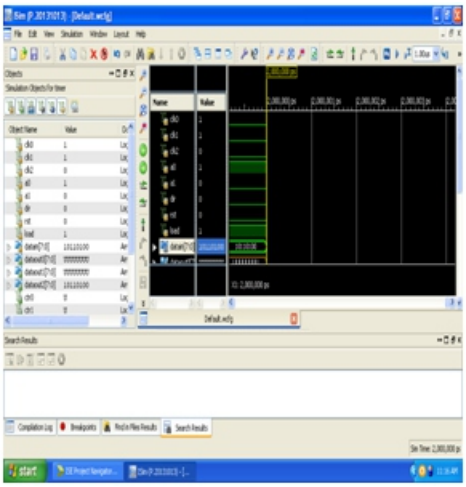

Fig 8: Simulation result for loading DATAIN bits into counter2 .

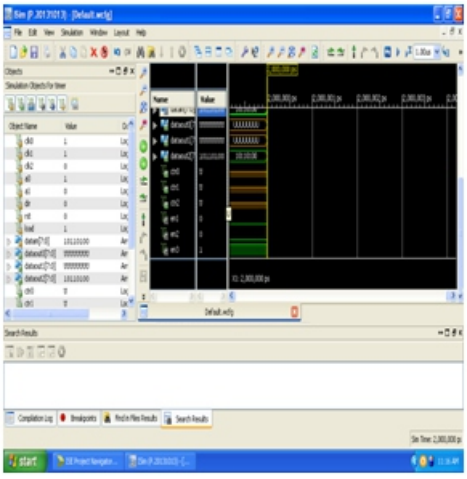

Fig 9: Simulation result for reading DATAIN bits from counter as DATAOUT2.

LOAD bit always said to 1 because if LOAD bit is 1 then only DATAIN bits loaded and gives DATOUT will comes as output. This is the general operation of timer circuit.

Fig 10: FPGA Implementation

For hardware implementation we used Xilinx Spartan-3-XC3S700A –FGG484AGQ0813 FPGA starter kit is used. The Spartan-3AN FPGA internal configuration interface is completely self-contained, increasing design security. From design specification, design will be coded using Very High Speed Integrated Circuit Hardware Descriptive Language. Simulation and verification will be done on Xilinx software. Results are then synthesized on Xilinx ISE. Generated Bitstream file will need to program the FPGA.

V. CONCLUISON:

The main objective of this paper to develop a timerby making use of Xilinx ISE.This project is useful to define the behavior of AC motor. This is a real time project so we can implement it in GFCs in Thermal power plants.

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