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Implementation Optimized Carry Select Adder Using Half Sum Half Carry Methodology

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ABSTRACT:

The carry-ripple adder is composed of many cascaded single-bit full-adders. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. In the carry select adder, N bits adder is divided into M parts. Each part of adder is composed two carry ripple adders with cin_0 and cin_1, respectively. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal.

Area-efficient carry select adder by sharing the common Boolean logic term. After Boolean simplification, we can remove the duplicated adder cells in the conventional carry select adder. Alternatively, we generate duplicate carry-out and sum signal in each single bit adder cell. By utilizing the half sum and half carry implementation delay can be overcomes the parallel architecture in the conventional carry select adder.

Tags:
Carry Ripple Adder, Half Sum Half Carry, Binary To Excess Code.

I.INTRODUCTION:

The conventional SQRT CSA architecture uses multiple sets of ripple carry adder block at each stage to reduce area and power dissipation. A modified SQRT CSA architecture is realized by replacing one ripple carry adder block with a binary-to-excess-1 converter. All the building blocks of SQRT CSA are implemented with CMOS TG. Also, 1-bit full adder needed for CSA is designed using CMOS TG based XOR gates . In the modified SQRT CSA, the BEC block is implemented using standard cells of CMOS inverter, TG based XOR and AND gates. To select the true sum and carry at each stage, a CMOS TG based 2:1 Mux is used.

II.RELATED WORK:

Adder is most commonly used arithmetic block in applications like central processing unit (CPU) and digital signal processing (DSP) [1]. Therefore design of area efficient, low power and high performance adder circuit is of utmost importance [2] [3] [4] [5]. This paper presents the analysis of 16-bit addition operation using SQRT CSA and its performance is evaluated in terms of MOS transistor count, total power dissipation and propagation delay. The conventional SQRT CSA architecture uses multiple sets of ripple carry adder block at each stage to reduce area and power dissipation.

A modified SQRT CSA architecture is realized by replacing one ripple carry adder block with a binary-to-excess-1 converter [2] [3].All the building blocks of SQRT CSA are implemented with CMOS TG. Also, 1-bit full adder needed for CSA is designed using CMOS TG based XOR gates. In the modified SQRT CSA, the BEC block is implemented using standard cells of CMOS inverter, TG based XOR and AND gates. To select the true sum and carry at each stage, a CMOS TG based 2:1 Mux is used.

III.IMPLEMENTATION LOGIC EXPRESSION OF BEC-BASED CSLA:

BEC-based CSLA consists of binary to excess-l converter in the place of RCA-2 in conventional CSLA as shown in Fig.4. The RCA is same as that of RAC-l in the conventional CSLA; it calculates n-bit sum {so I (i)} and

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carryout {CO out} corresponds to Cin = O. Inputs to the BEC unit is {so I (i), CO out} and output is (n+ 1)-bit excess-l code. The most significant bit (MSB) of the output of BEC unit represents Clout and remaining n least significant bits (LSBs) represents.

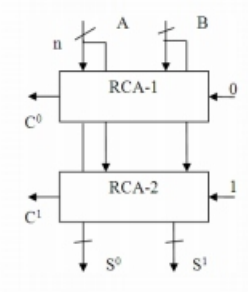

Fig.1. Structure of Ripple Carry Adder

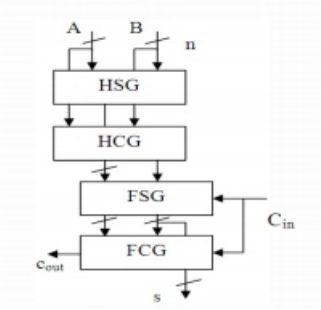

Fig.2.Structure of SCG unit

The logic expressions of BEC-based CSLA is given as,

$$S^1_1(0) = s^0_1(0) \quad (3a)$$

$$C^1_1(0) = s^0_1(0) \quad (3b)$$

$$S^1_1(i) = s^0_1(i) \oplus c^1_1(i\text{-}1) \quad (3c)$$

$$C^1_1(i)\,c = s^0_1(i).c^1_1(i\text{-}1) \quad (3d)$$

$$C^1_{out} = c^0_1(n\text{-}1) \oplus c^1_1(n\text{-}1) \quad (3e)$$

(For $1 \le i \le n\text{-}1$).

From (3d) we can say that c I I depends on s o" in the case of conventional CSLA c I has no dependence on s\ Therefore BEC based CSLA has much data dependant compare to conventional CSLA. From (lc)-(2c) it can be observed that S O l and s I I are identical except the terms C O I and c I I since (so o=s I 0). In addition to that C O l and C l l depend on {so, CO ,Cin}. Since C O l and c I have no data dependence on S O I and s I I the logic . ° I 'of c I and c I can be calculated before calculating and we can select any one from set using selection unit for the sum of CSLA.

Most of the logic resources of CSLA are spent on calculating S1}d .Rejecting one sum-word is not efficient approach after calculation of two sums. Instead of this we can select any one of carry words using carry input Cin for calculating final sum.

IV.RESULTS:

RCA Carry Select Adder

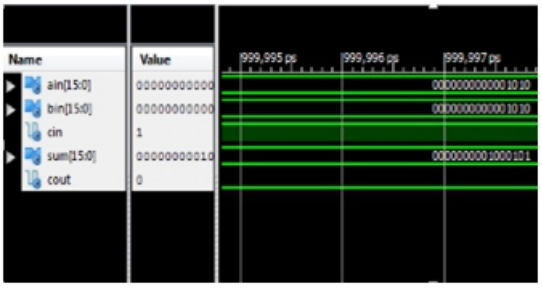

Fig 3: RCA carry select adder resultant

Ripple carry select adder is a mux based implementation as discussed in the chapter2.The resultant is show in the above result with carry given 1.

Proposed Adder:

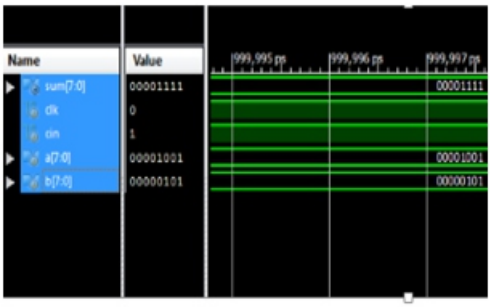

Fig 4: proposed adder simulation result

Proposed adder is implemented using half sum and half carry method .To input a and b are 9 and 5 respectively .and the carry is 1.the final resultant is 15 shown in sum with 8 bits

	proposed	conventional
slices	25	25
Flip flops	43	46
4 input luts	42	43
Iob	26	50

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V.CONCLUSION:

After Boolean simplification, we can remove the duplicated adder cells in the conventional carry select adder. Alternatively, we generate duplicate carry-out and sum signal in each single bit adder cell. By utilizing the half sum and half carry implementation delay can be overcomes the parallel architecture in the conventional carry select adder. In this way, the circuit area and lut count can be greatly reduced and power delay product of the adder circuit can be also greatly lowered

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