ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Reversible 2:4 Decoder and Its Applications

Sayyad Khaja Moinuddin
MTech(DECS),
Alhabeeb College of Engineering, Hyderabad.

Syed Samiuddin M.Tech,
Associate Professor,
Alhabeeb College of Engineering, Hyderabad.

Abstract:

In this paper realization of 2:4 reversible decoderis proposed which can provide active high as well as active lowoutputs. The proposed decoder uses Feynman and Fredkin gatesand has low quantum cost The proposed gate is fist extended to3:8 decoder followed by an n-input decoder. The theoreticalproposition is verified through SPICE simulations. A comparisonwith existing reversible decoders is also included.

Keywords:

Reversible decoder, Feynman and Fredkin gates.

I. INTRODUCTION:

The encoded input information need be preserved at theoutput in computational tasks pertaining to digital signalprocessing, communication, computer graphics, andcryptography applications [1]. The conventional computingcircuits are irreversible i.e. the input bits are lost when the output is generated. This information loss during computationculminates into increased power consumption. According toLandauer [2], for each bit of information that is lost during the computation generates KTln2 Joules of heat energy where Kand T respectively represent oltzmann's constant andabsolute temperature. The information loss becomes morefrequent for high speed systems thereby leading to increasedheat energy. C. Bennett [3] demonstrated that powerdissipation in can be significantly reduced the same operationis done reversibly. Reference [4] describes that reversible logicallows the circuit to go back at any point of time therefore nobit of information is actually lost and the amount of heatgenerated is negligible.In digital design, decoders find extensive usage – inaddressing a particular location for read/write operation inmemory cells [5], in I/O processors for connecting a memorychips to the CPU [6]; and also in Analog to Digital (ADC) andDigital to Analog Converters (DAC) which are used in variousdifferent stages of a communication system. This papertherefore addresses the design of reversible decoders.

Theliterature survey on reversible decoders [7 - 11] shows that thefocus is on either developing topology based on availablereversible gates [7 - 9] or present an altogether new gate for thesaid purpose [10, 11]. The topology [7] employs DoubleFeynman and Fredkin gates for realization whereas the onepresented in [8, 9] is based on Fredkin gates. The formertopology is cost efficient and later has higher cost metrics.Comparatively larger number of constant inputs and garbageoutputs are present in [7]. A new gate R2D is proposed in [10]for developing reversible decoders. It, however, has largeconstant inputs and garbage outputs. Yet another reversibledecoder is presented in [11] which has attractive cost metricsbut it cannot be extended further into a generalized n- inputdecoder. The reversible decoders [7-11] provide only activehigh mode of operation. This study introduces a reversibledecoder which can provide both active high and active lowmode of operation and utilizes Feynman and Fredkin gates. Acomparison in terms of number of constant inputs, quantumcost and the number of garbage outputs is also given. Theproposed topology is implemented using transmission gates.The functionality of the theoretical proposition is verifiedthrough SPICE simulations using 180 nm TSMC CMOStechnology parameters.

A. Proposed 2:4 Reversible Decoder:

The proposed 2:4 Reversible decoder is shown in Fig. 2. Ituses two Feynman gates (FG) and two Fredkin gates (FRG). Ithas three inputs A, B and S where A and B are the inputs tothe decoder and S is the select line which will select the modeof operation for decoder. The output lines of decoder are takenfrom the outputs of the two cascaded Fredkin gates wherein each of the Fredkin gates provides two of the four outputs ofthe decoder. The active high outputs are achieved for S=0,therefore only a single output will be at logic high and all The operation of the circuit is given in Table 1. The proposed decoder uses twoconstant inputs and a single garbage output; and has quantumcost of 12. other outputs will be at logic low. Conversely, S=1 providesactive low operation thus single output will be at logic low andall other outputs will assume logic high.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Thus, the proposed circuit performs the operation in active high as well as active low mode in a very costefficient manner. The next section describes theimplementation of 3:8 decoder using decoder of Fig. 2.

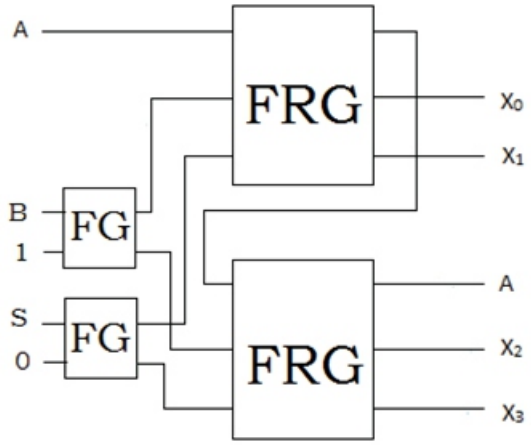


Fig. 2. Proposed 2:4 Reversible Decoder

Table 1 Truth Table for proposed 2:4 reversible decoder:

Inputs		Outputs(S = 0)				Outputs(S = 1)			
A	B	X_2	X_0	X_3	X_1	X_0	X_2	X_1	X_3
0	0	1	0	0	0	0	1	1	1
0	1	0	1	0	0	1	0	1	1
1	0	0	0	1	0	1	1	0	1
1	1	0	0	0	1	1	1	1	0

B. Proposed 3:8 Reversible Decoder:

The block diagram of the proposed 3-to-8 decoder is hown in Fig. 3 where A, B and C are the inputs to thedecoder, S is the select line and Yi (i = 0, 1, ..7) represent theoutputs. It uses the proposed 2-to-4 decoder and cascade itwith Fredkin and Feynman gates. It also uses an dditional 1to 5 tracer circuit in order to remove the fan out problem in thereversible decoder in case S had been the output of any otherreversible gate.

This block copies input S to 5 different linesand comprises of Feynman gates. Each of the tracer circuitoutput is applied to the input to the Fredkin gates. The tracercircuit, however, will not be needed if S is the not an output of any other reversible gate. Table 2 and 3 show the truth tablesof the proposed decoder with select line S = 0 and 1respectively.

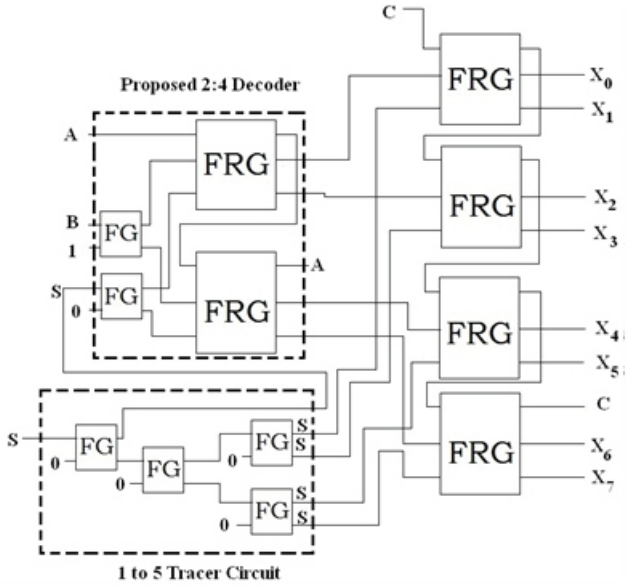


Fig. 3. Proposed 3:8 Reversible Decoder.

The proposed 3:8 decoder can easily be extended to ageneralized m: 2m reversible decoder where n is greater than orequal to 3. The generalized decoder will use a 1 to (2m - 3) tracer circuit which will copy the input S to each of the 2m – 3lines and can easily be implemented by using Feynman gatesin the same manner in which 1 to 5 tracer circuit was implemented. Figure 4 shows the generalized m:2m reversibledecoder, here A1, A2,…, Am are its inputs and outputs arerepresented as Z0, Z1, …, Zn (n=2m), and S is the select line.

Table 2 Truth table for Proposed 3:8 reversible Decoder with S=0

Table 2 Truth table for Proposed 3:8 reversible Decoder with S=0

Inputs			Outputs							
A	B	C	Y_4	Y_5	Y_1	Y_0	Y_6	Y_7	Y_2	Y_3
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table 3 Truth table for Proposed 3-to-8 reversible Decoder with S=1

Inputs			Outputs							
A	B	C	Y_0	Y_1	Y_4	Y_5	Y_2	Y_3	Y_6	Y_7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

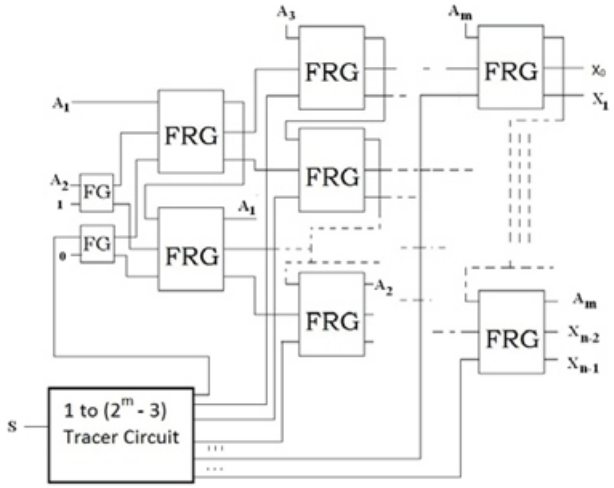
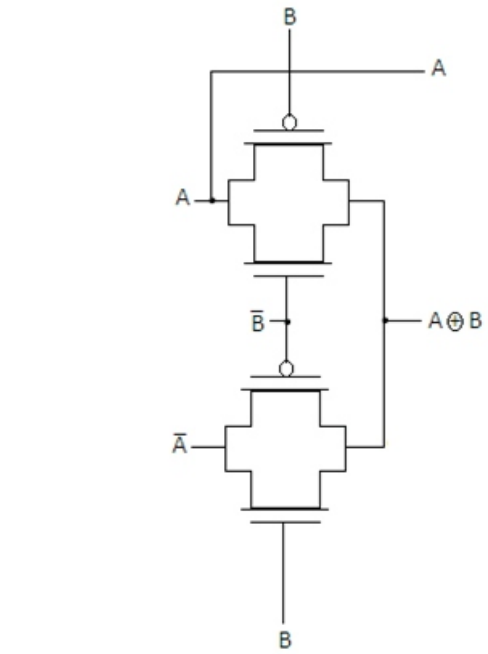


Fig.4. Generalized block diagram for m:2m Reversible Decoder

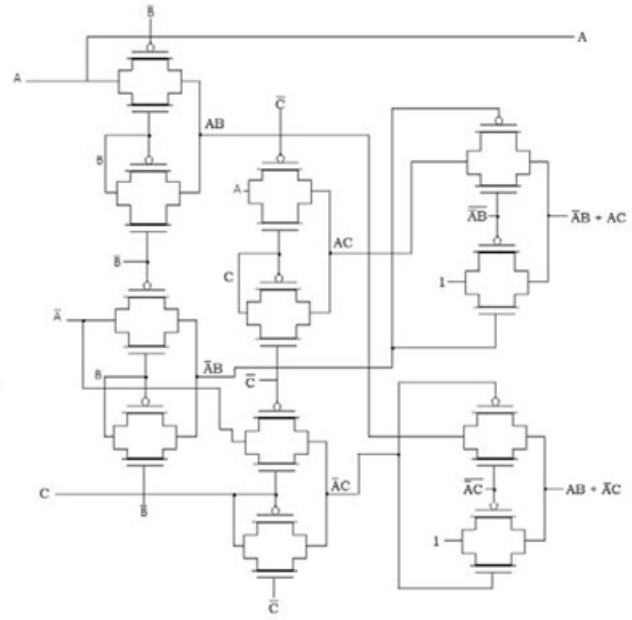
C. Transmission Gate based implementation of Feynman andFredkin gates:

A transmission gate (TG) is parallel connection of NMOSand PMOS switch and is shown in figure 5. The inputs X and S(applied to gate terminals) are called pass and control input and the gate provides. The output of TG is represented as Y.

Whenthe control signal S=0, the output will be in high impedancestate while following the pass input (X) for S=1. The advantage of TG gate over NMPS or PMOS pass gate lies in the fact thatthe output is not degraded in the former one. The TG basedimplementation of Feynman and Fredkin gates is given in Fig.
5.



(a)



(b)

Fig. 5. TG based implementation of (a) Feynman and (d) Fredkin Gates

III. SIMULATION RESULT AND ANALYSIS:

The theoretical proposition is verified using SPICEsimulations using 0.18m TSMC CMOS technologyparameters. Proposed 2:4 and 3:8 reversible decoders havebeen implemented using the TG representation of FG andFRG gates given in Fig. 5.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The aspect ratios of all NMOS andPMOS transistors are taken as 0.2m/0.27m and0.5m/0.27m respectively. Figures 6 and 7 depict thesimulated result for active high mode of operation of poposed2:4 and 3:8 decoders. Similar results are obtained for activelow mode of operation. The simulated results for 2-to-4 and 3-to-8 reversible decoders adhere to their functionality.The proposed 2:4 and 3:8 decoders are compared withtheir existing counterparts and are summarized in Table 4. Theproposed 2:4 decoder show 50% reduction in the number ofconstant inputs and garbage outputs as compared to the oneproposed in [7] with no increase in quantum cost.

Though theproposed 3:8 decoder has a higher quantum cost (12.5%) than[7] but uses lesser number of constant inputs and garbageoutputs and an advantage of providing active high and activelow mode of operation. Similarly, while comparing theproposed 2:4 decoder with the one given in [8], it is observedthat there is 66.67% , 50% and 20% improvement in constantinputs, garbage output and quantum cost. Compared todecoders of Ref. [9], the proposed decoder is better in terms of constant inputs and garbage outputs.

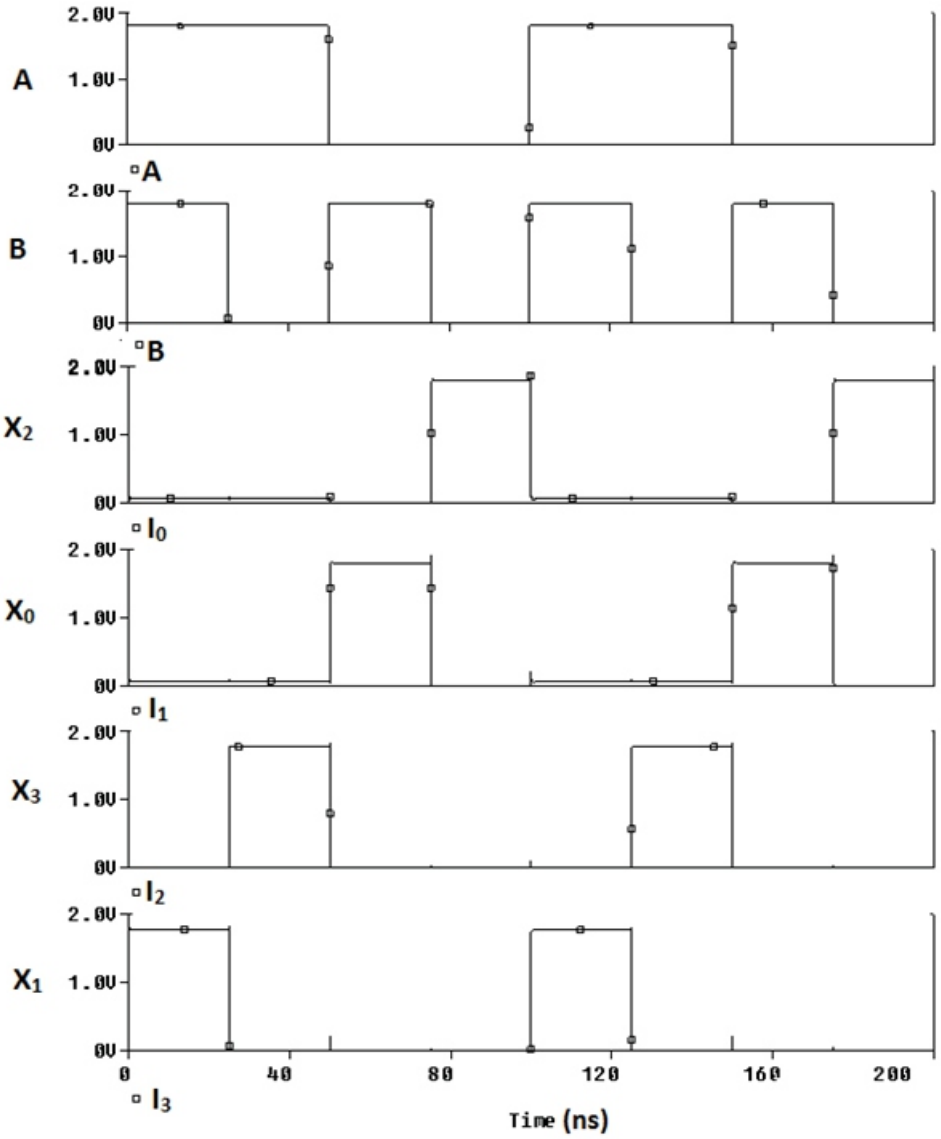


Fig. 6. Simulated waveforms of proposed 2:4 decoder

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table 4 Comparison of Proposed 2:4 and 3:8 reversible decoders with their existing counterparts:

Ref. [7]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	4	2	12
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+50%	+50%	0%
3:8 Decoder	8	3	32
Proposed 3:8 Decoder	6	2	36
Percentage Improvement	+25%	+33%	-12.5%

Ref. [8]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	6	2	15
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+66.67%	+50%	+20%

Ref. [9]	Constant Inputs	Garbage Outputs	Quantum Cost
2:4 Decoder	3	1	11
Proposed 2:4 Decoder	2	1	12
Percentage Improvement	+33.33%	+0%	-9.09%
3:8 Decoder	8	3	35
Proposed 3:8 Decoder	6	2	36
Percentage Improvement	+25%	+33.33%	-2.85%

IV. CONCLUSION:

Reversible decoder of size 2:4 is presented in thispaper and the design is extended to 3:8 decoder. The design is-generalized to n-to-2n reversible decoder. The propose-dreversible decoders used Feynman and Fredkin gates whichare implemented using TG logic. The proposed reversibledecoders can be used in active high or active low mode ofoperation depending upon the select line. The structure ismore efficient than its previous counterparts. The cost metrics of the proposed decoder can further be reduced if the selectline 'S' is assumed not to be the output of any other reversible gate.

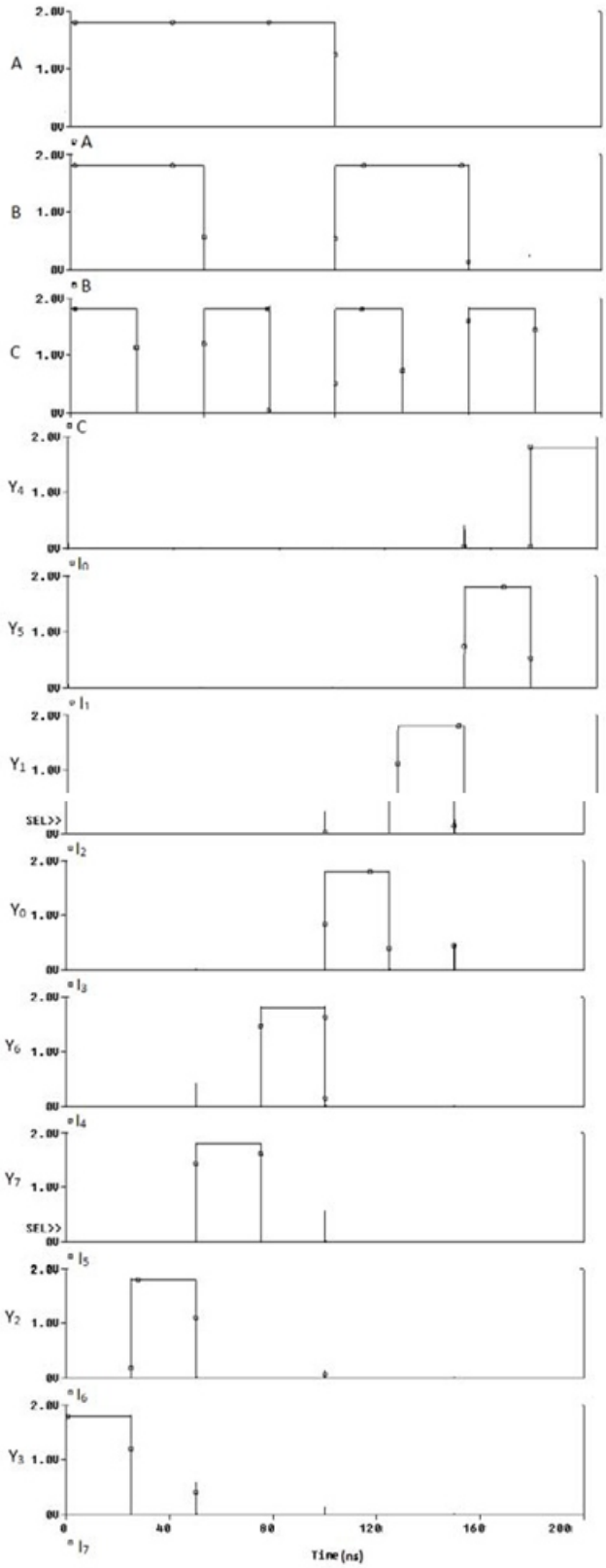


Fig. 7. Simulated waveforms of proposed 2:4 decoder

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Reference:

[1] V. V. Shinde, A. K. Prasad, I. L. Markov, and J. P. Hayes, "Synthesis ofReversible Logic Circuits," IEEE Tran Computer-aided Design of Int. Cir. AndSyst., vol. 22, pp. 710-722, 2003.

[2] R. Landauer, "Irreversibility and heat generation in the computationalprocess," IBM J. Res. Develop., vol. 5, pp. 183–191, 1961.

[3] C. H. Bennett, "Logical reversibility of computation," IBM J.Res. and Develop., vol. 17, pp. 525-532, 1973.

[4] A. De Vos, "Reversible computing," Prog. Quantum Electron., vol. 23,no. 1, pp. 1–49, Jan. 1999.

[5] R. J.. Tocci, Digital Systems: Principles and Applications, Printice Hall,1988.

[6] M. Morris Mano, Computer System Architecture, Pearson..

[7] M. Shamsujjoha, and H. M. H. Babu, "A Low Power Fault TolerantReversible Decoder Using MOS Transistor," 2013 26th InternationalConference on VLSI Design and the 12th International Conference onEmbedded Systems, pp. 368 – 373, 2013.

[8] S. K. Noor Mahammad, S. K. Sastry Hari, S. Shroff, and VKamakoti, " Constructing online testable circuits using reversible logic",Proceedings of the 10th IEEE VLSI Design and Test Symposium(VDAT), Goa, India, August 2006, pp. 373-383.

[9] R. Aradhya, R, Chinmaye, and K. Muralidhara, "Design, Optimizationand Synthesis of Efficient Reversible Logic Binary Decoder,"International Journal of Computer Applications, vol. 46, pp. 45-51,2012.

[10] M. Morrison, and N. Ranganathan, "Design of a Moore Finite StateMachine using a Novel Reversible Logic Gate, Decoder andSynchronous Up-Counter," 2011 11th IEEE International Conference onNanotechnology Portland Marriott, pp. 1445-1449, 2011.

[11] M. Nachtigal, and N. Ranganathan, "Design and Analysis of a NovelReversible Encoder/Decoder", 2011 11th IEEE InternationalConference on Nanotechno'logy, Portland Marriott, pp. 1543-1546,2011.

[12] H. Thapliyal and N. Ranganathan, "Design of Reversible SequentialCircuits Optimizing Quantum Cost, Delay, and Garbage Outputs," ACMJ. on Emerging Technologies in Computer Systems, vol. 6, pp. 14.1-14.31, 2010.

[13] M. Nielsen, I. Chuang, Quantum Computation and QuantumInformation, Cambridge University Press, 2000[14] E. Fredkin, and T. Toffoli, "Conservative logic," International J. Theor.Physics, vol. 21, pp. 219 - 253,1982.