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Simulation of Three Phase Hybrid Multilevel Inverter Using Switched Capacitor Units Fed Induction Motor Drive

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Abstract:

This paper highlights a hybrid multilevel inverter for A.C electrical drives. In recent days multilevel inverters has become very popular for motor drive applications of industry. This hybrid topology has more advantageous of industrial applications. In conventional methods, the need of converters to supply the cells of reversible multilevel converters increases the cost and losses of such inverters. Moreover the advantages like high quality power output, low switching losses, low electro-magnetic interference (EMI) and high output voltage made multilevel inverter as a powerful solution in converter topology.

In this paper two new topologies have been proposed for multilevel inverters. The proposed topologies consist of a combination of the conventional series and the switched capacitor inverter units. The proposed method introduces 17, 25 levels and three phase 25level Inverter fed Induction Motor drive. With the use of high level inverter, resolution is increase and also the harmonics is highly reduced. The simulation results are presented by using Matlab/simulink software.

Index Terms:

Multilevel inverter, series inverters, series– parallel connection, switched capacitor, induction motor.

I. INTRODUCTION:

Multilevel inverters include an array of power electronic devices and voltage sources with shunt capacitances, the output of which are voltages generated in the form stepped waveforms.

The commutation of the switches provides the addition of the capacitor voltages, thus reaching high voltage at the output, while the power devices must withstand only reduced voltages [8]. These multilevel inverters (MLI) have become an effective solution for increasing power and reducing harmonics of AC waveform [7].It involves the concept of utilizing a large number of active semiconductor switches to perform the power conversion in small voltage steps for higher voltage and reduction in harmonic distortion.The proposed inverter does not have any inductors can be smaller than a conventional two-stage unit which consists of a boost converter and an inverter bridge, which make the system large. The structure of the inverter is simpler than [3] the conventional switched-capacitor inverters. THD of the output waveform of the inverter is reduced compared to the conventional single phase full bridge inverter as the conventional multilevel inverter. In this paper, an SC inverter whose structure is simpler than the conventional SC inverter is proposed. It consists of a Marx inverter structure and an H-bridge. The proposed inverter can output larger voltage than the input [3] voltage by switching the capacitors in series and in parallel. The proposed inverter does not have any inductors which make the system large [4]. The output harmonics of the proposed inverter are reduced by the multilevel output.The proposed topologies have a modular structure and can benefit the advantages of the series multilevel inverters [10]–[13]. The fundamental switching method is used in this investigation. In addition, to produce all voltage levels at the output (even and odd), a new algorithm for the determination of the magnitude of the isolated dc voltage sources is proposed. Finally, the loss calculation is done, and the performance of the proposed topologies is verified by simulation results of single-phase 25- and 17-level inverters.

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II.PROPOSED SWITCHED CAPACITOR TOPOLOGY:

Fig.1. shows the proposed switched capacitor unit. This topology is yield from series combination of several basic units. In this figure, the switches Si (i=1, 2, n) connect the capacitors in series, and the switches Pi connect the capacitors in parallel with the dc voltage sources. To produce zero and negative voltage levels, an H-bridge has been used at the output. The blocked voltage by each switch in Fig.1. is Vdc.

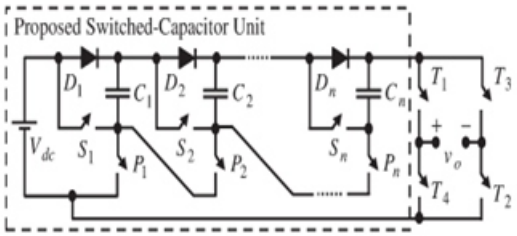

Fig.1. Proposed switched capacitor unit.

Thus, the proposed switched capacitor unit is also proper for a high frequency application that is not the aim of this paper. The other advantage of the proposed topology is the boosting ability of the input dc voltage without using any transformer. This feature reduces the size and cost of the system and increases its efficiency. The maximum numbers of output voltage levels (Nstep), required insulated-gate bipolar transistors (IGBTs) (NIGBT), and diodes (Ndiode) for the proposed topology shown in 3.3 are calculated by the following equations, respectively,

$$N_{\text{step}} = 2n + 3 \quad (1)$$

$$N_{\text{IGBT}} = 2n + 4 \quad (2)$$

$$N_{\text{diode}} = n \quad (3)$$

Where n is the number of capacitors. The maximum output voltage that can be produced (Vomax) is equal to

$$V_{o,\max} = (n+1)V_{\text{dc}}. \quad (4)$$

In order to reduce the capacitor voltage drop during the series connection, the pulse width-modulation switching pattern can be used between the it h and (i+1) th consecutive voltage levels (i=0, 1, 2, n), which, in turn, will increase the losses. On the other hand, more capacitors are needed to produce more levels at the output. Greater number of series capacitors increases their voltage drop.

Thus, generating desirable voltage waveform without using of filtering elements will be difficult and requires more complex switching schemes. To produce greater number of voltage levels at the output and reduce the capacitor voltage drop, several units shown in Fig.1. can be used in series. In this condition, the first unit, the second unit, and the kth unit have n1, n2, and nk capacitors and dc voltage sources with magnitudes ofV1, V2, and Vk, respectively.

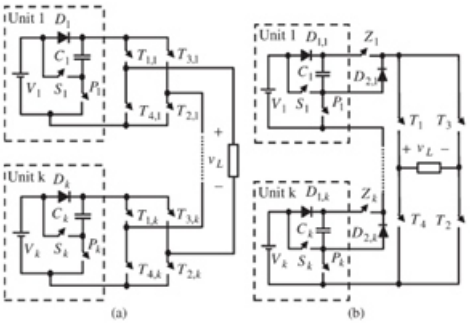

Fig.2. (a) First proposed topology. (b) Second proposed topology.

The general form of the equations that show the number of voltage levels and the number of IGBTs can be expressed as follows:

$$N_{\text{step}} = a\left[\prod_{j=1}^{k}(bn_j + c)\right] + d \quad (5)$$

$$N_{\text{IGBT}} = 2\left(\sum_{j=1}^{k} n_j\right) + ek + f \quad (6)$$

Where a, b, c, d, e, and fare the integer numbers that depend on the unit connection order. In order to produce the maximum number of voltage levels at the output with using a specified number of IGBTs, (6) can be rewritten as follows:

$$N_{\text{IGBT}} = 2(n_1 + n_2 + \ldots + n_k) + ek + f = cte. \quad (7)$$

$$n_1 + n_2 + \ldots + n_k = \frac{N_{\text{IGBT}} - ek - f}{2} = cte. \quad (8)$$

Considering (5) and (8), the number of voltage levels in (5) will be maximum when the following condition is satisfied

$$n_1 = n_2 = \ldots = n_k = n \quad (9)$$

From (8)–(10), N step is obtained as follows

$$N_{\text{step}} = a(bn + c)^{\frac{N_{\text{IGBT}} - f}{2n + e}} + d \quad (10)$$

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Equation (10) will be maximum when nets its minimum value. Thus, the proposed topologies produce the maximum number of voltage levels at the output form=1. This result is independent of the units' connection order. The proposed topologies have been presented in the next sections with considering n=1.

A. First Proposed Topology:

Fig.2.(a) shows the first proposed topology. In this topology, the switched capacitor units have been connected in series by using H-bridges. Each unit can only produce positive voltage levels. The H-bridge produces zero and negative voltage levels. There are a lot of ways to determine the magnitude of the dc voltage sources. Some of these algorithms are not able to produce all voltage levels at the output, and some of them produce repetitive voltage levels. In order to prevent the mentioned problems and produce the maximum number of voltage levels, the magnitude of the dc voltage sources in the jth unit can be as follows:

$$V_j = (5^{j-1}) \quad V_1 \tag{11}$$

Voltage and current ratings of the switches in a multilevel inverter play important roles in the total cost of the inverter. In all topologies, the currents of all switches are equal to the rated current of the load. This is, however, not the case for the voltage. Hence, there is a need for a criterion to evaluate the multilevel inverter from the viewpoint of blocked voltage by power switches and the total cost of system. This criterion is captioned as "standing voltage". The standing voltage is equal to the sum of all blocked voltages by power switches in a converter. The standing voltage of the switches is equal to the sum of the blocked voltages by switches S and P and the H-bridge switches for all units.

B. Second Proposed Topology:

Fig.2.(b) shows the second proposed topology. In this topology, each unit is bypassed when the switch Pj and the diode D2,j are on and the switch Zj is off. When the switch Zj is on, the diodeD2, j becomes reverse biased. Thus, the diode D2,j prevents the backward current flowing during the unit bypassing when an inductive load is used at the output. In other words, the second proposed topology can produce the desirable voltage waveforms for resistive loads. On the other hand, by replacing the diode D2,j with a power electronic switch, the second proposed topology can be used for resistive-inductive loads.

The magnitude of the dc voltage sources and the number of voltage levels can be calculated as follows:

$$V_j = (3^{j-1}) \quad V_1 \tag{12}$$

The number of voltage levels (Nstep), the number of required IGBTs (NIGBT), the number of diodes (Ndiode), the maximum output voltage (Vo, max), the standing voltage of the switches (Vst and), the number of dc voltage sources (Ndc), and the variety of the dc voltage source magnitude (Nvariety) can b calculated for the first and second proposed topologies, as shown in Table I.

III. COMPARISON OF THE PROPOSED TOPOLOGIE SWITH OTHER CONVENTIONAL TOPOLOGIES:

In this section, the first proposed topology has been compared with three main topologies of multilevel inverters, namely, the diode-clamped multilevel one, capacitor

TABLE I:CALCULATION OF DIFFERENT PARAMETERS OF THE PROPOSED TOPOLOGIES:

Parameter	Proposed Topology	
	First	Second
N_{step}	5^k	$(2\times3^k)-1$
N_{IGBT}	$6k$	$3k+4$
N_{diode}	k	$2k$
$V_{o,max}$	$2\sum_{j=1}^{k} V_j$	$2\sum_{j=1}^{k} V_j$
V_{stand}	$10(1+5+\cdots+5^{k-1})V_1$ $=5\left(\frac{5^k-1}{2}\right)V_1$	$11(1+3+\cdots+3^{k-1})V_1$ $=11\left(\frac{3^k-1}{2}\right)V_1$
N_{dc}	k	k
$N_{variety}$	k	k

TABLE II:COMPARISON OF THE FIRST PROPOSED TOPOLOGY WITH THE TOPOLOGIES PRESENTED IN [9]

Topologies	N_{step}	N_{switch}	N_{diode}	$N_{capacitor}$	N_{dc}
First topology	25	12	2	2	2
DCM	13	24	132	12	1
CCM	13	24	0	66	1
CMM	13	24	0	6	1
CBSCM	13	10	12	6	1
SCBM	13	11	3	2	1
HSSCM	13	21	4	5	3

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Clamped multilevel one, and cascaded multi cell multilevel one. Also, the proposed topology has been compared with a cascade-boost switched capacitor converter multilevel inverter, a switched capacitor boost multilevel inverter, and a hybrid-source switched capacitor multilevel inverter [9]. Table II shows the numbers of switches, diodes, capacitors, and voltage levels for the proposed topology and the topologies presented in [9]. Table II proves the advantages of the proposed topology. In order to show the advantages of the proposed topologies in comparison with some recently presented topologies that use isolated dc voltage sources, the proposed topologies have been compared with the cascaded multilevel inverter using bidirectional switches (CMIBS), cascaded multilevel inverter using binary units (CMIBU), optimal topologies for cascaded sub multilevel inverters (OCSMI), cascaded multilevel inverter with reduced number of components for high-voltage applications (CMIHV), multilevel inverter with reduced number of power electronic components (MIRC) , and multilevel inverter using switched series/parallel dc voltage sources (MISSP) from different aspects. Fig.3. shows the number of required IGBTs for producing specified voltage levels at the output of the proposed topologies and the topologies presented. As can be seen, the proposed topologies need fewer IGBTs for realized Nstep voltage levels at the output.

IV.INDUCTION MOTOR:

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

V.MATLAB/SIMULINK RESULTS:

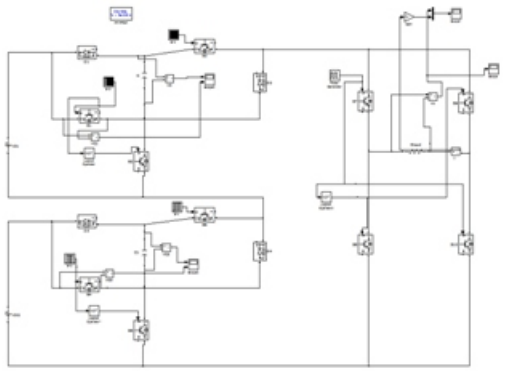

Fig.4.Matlab/Simulink model of 17-level inverter based proposed topology.

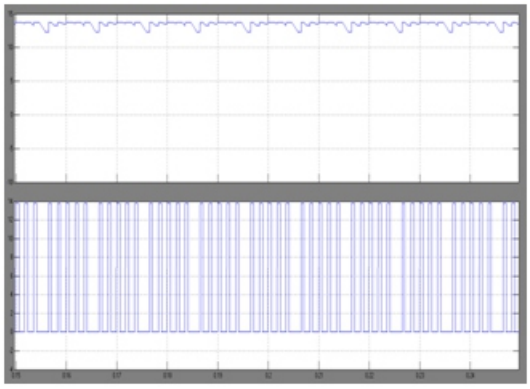

Fig.5. capacitor voltage (Vc1) and switch voltage(S1).

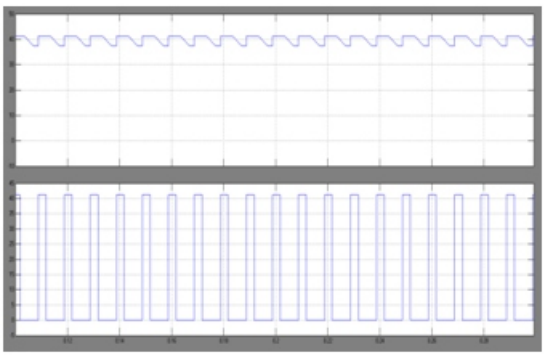

Fig. 6. capacitor voltage(Vc2) and switch voltage(S2).

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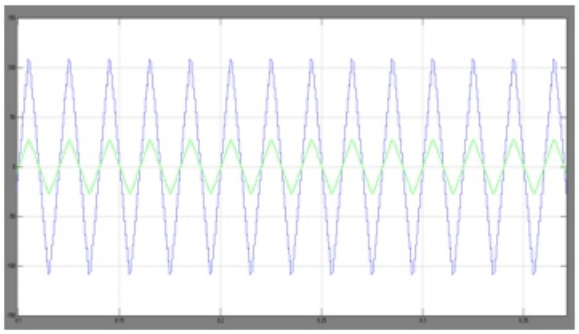

Fig.7. Simulated load voltage and current waveforms for 17-level inverter.

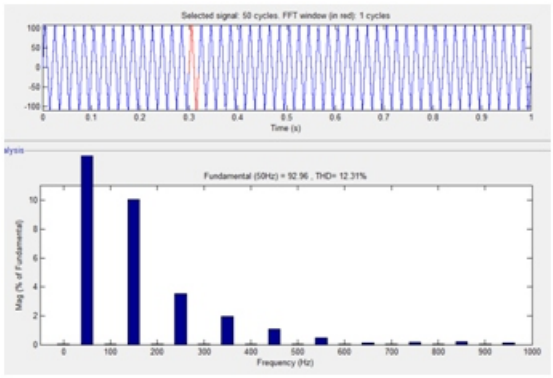

Fig.8.total harmonic distractions for 17 Level inverter.

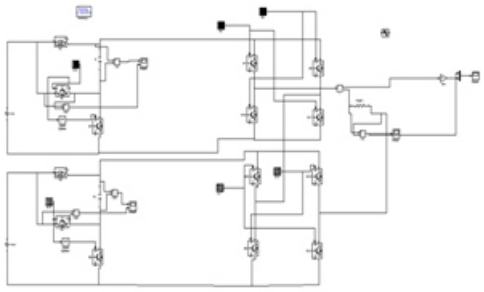

Fig.9.Matlab/Simulink model of 25-level inverter based proposed topology.

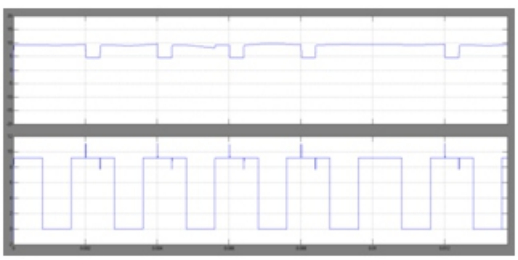

Fig.10 capacitor voltage (Vc1) and switch voltage(S1).

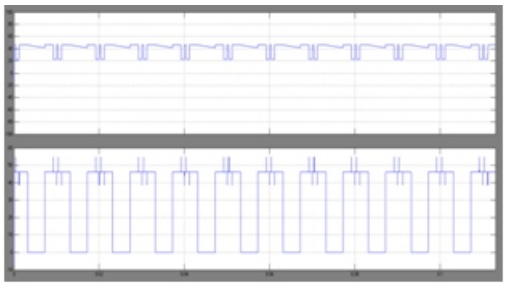

Fig.11.capacitor voltage (Vc2) and switch voltage (S2).

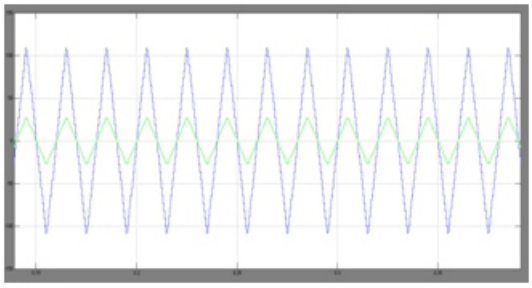

Fig.12. Simulated load voltage and current waveforms for 25-level inverter.

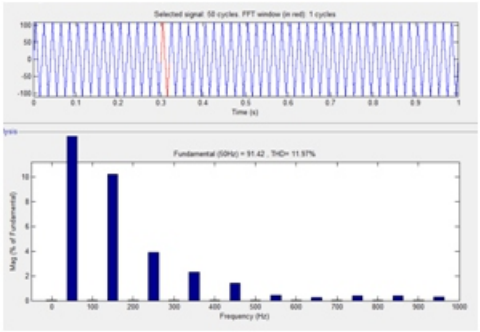

Fig.13.total harmonic distractions for 25 Level inverter.

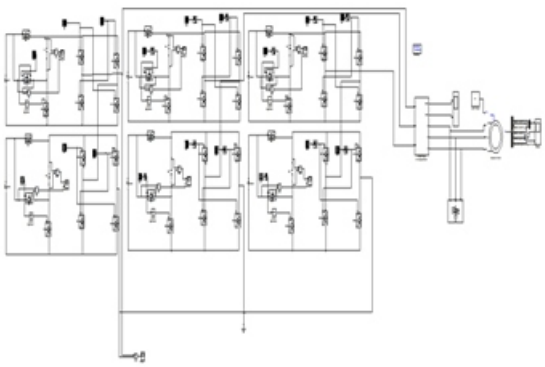

Fig.14.Matlab/Simulink model of three phase 25-level inverter based proposed topology with induction motor.

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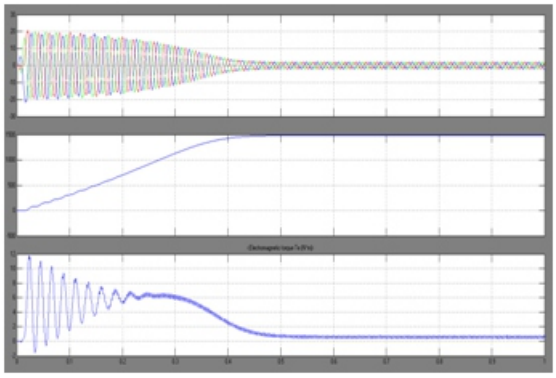

Fig.15. Stator Currents, Speed, Electromagnetic Torque.

Fig.15. Stator Currents, Speed, Electromagnetic Torque of Proposed Three Phase 25 level inverter Applied to Induction machine Drive.

VI.CONCLUSION:

In this paper, two new topologies have been proposed for multilevel inverters. The algorithms for the determination of the dc voltage source values have been presented, and the optimal number of switches and dc voltage sources to produce the maximum number of voltage levels at the output has been obtained. The loss calculations have been done. The number of on–off times in one cycle and the conduction intervals offal switches have been calculated as a function of the output voltage levels. The proposed topologies reduce the number of switches and isolated dc voltage sources, the variety of the dc voltage source values, and size and cost of the system in comparison with conventional series topologies. The first proposed topology produces a 25-level voltage for all load power factors by using 12 IGBTs, 2 diodes, and 2 isolated dc voltage sources. It is also observed that the proposed topology decreased the number of required power electronic switches compared to a cascaded H-bridge inverter to obtain the same 17 and 25 level output voltage with lower THD. The induction motor performance curves such as speed, torque and current are presented. The simulation results show that the hybrid H-bridge fed Induction Motor drive has a satisfactory performance.

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