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Reconfigurable Approximation Technique for Video Encoding Using Arithmetic Units

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Abstract:
The research community in the last few years from the field of approximate computing has received significant attention, particularly in the context of different signal processing. Image and video compression algorithms such as JPEG, MPEG and so on, which can be exploited to realize highly power-efficient implementations of these algorithms. However, existing approximate architectures typically fix the level of hardware approximations statically and are not adaptive to input data. This project addresses this issue by proposing a reconfigurable approximate for MPEG encoders that optimizes power consumption with the aim of maintaining a particular peak signal-to-noise ratio threshold for any video. I design reconfigurable adder/subtractor blocks, and subsequently integrate these blocks in the motion estimation and discrete cosine transform modules of the MPEG encoder. I propose two heuristics for automatically tuning the approximation degree of the RABs in these two modules during runtime based on the characteristics of each individual video. Dynamically adjusting the degree of hardware approximation based on the input video respects the given quality bound PSNR degradation across different videos while power saving a dual mode full adder is greater than the full adder, when compared to existing implementations. Index terms- approximate circuits, low power design, approximate computing, and quality configurable.

I. INTRODUCTION:

Digital signal processing (DSP) blocks from the Backbone of various multimedia applications used in portable devices.

Most of the DSP blocks implement image and video compression algorithms. Approximate computing architectures exploit the fact that a small relaxation in output correctness can result in significantly simpler and lower implementations. However, most approximate hardware architectures proposed so far suffer from the limitation that, for widely varying input parameters, it becomes very hard to provide a quality bound on the output, and in some cases, the output quality may be severely degraded. The main reason for this output quality fluctuation is that the degree of approximation (DA) in the hardware architecture is fixed statically and cannot be customized for different inputs. This paper adopts a different approach to addressing this problem by dynamically reconfiguring the approximate hardware architecture depending on the inputs. Following contributions are

1) I demonstrate that, for a fixed level of hardware approximation in an MPEG encoder, the output quality varies widely across different videos, often going below acceptable limits. This shows that setting the level of hardware approximation statically is insufficient.

2) I investigate, for this paper, the use of dynamically reconfigurable approximate hardware architectures that vary the degree of approximation during run-time across multiple computational cycles, depending on the inputs.

3) Toward this end , I propose the design of reconfigurable adder/subtractor blocks for four commonly used adder architectures, viz, ripple carry adder , carry look ahead adder, carry bypass adder, and carry select adder, and subsequently integrate them

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into the MPEG encoder to enable quality configuration execution.

4) I propose a design methodology to adapt a degree of approximation dynamically based on the characteristics with the main aim of maintaining the output quality.

5) I have implemented the proposed architecture for an MPEG encoder on a Dual mode full adder (DMFA). My experimental results show that the proposed architecture results in power savings compare to a baseline approach that uses reconfigurable approximate architecture with the goal of maintaining a particular peak signal-to-noise ratio (PSNR) threshold for any video.

Ii. Background

MPEG Compression Scheme

MPEG is mostly preferred for the video compression scheme in modern video devices and applications. MPEG- 2/MPEG-4 standards are used to squeeze to very small sizes. MPEG uses both Inter frame and Intra frame encoding for video compression. Intra frame encoding involves encoding the entire frame of data, while Inter frame encoding utilizes predictive and interpolative coding techniques as means of achieving compression. The inter frame version exploits the high temporal redundancy between adjacent frames and only encodes the differences in information between the frames, thus resulting in great ratios. In this case, the encoding takes placed based upon the differences between the current frame and previous frame in the video sequence.

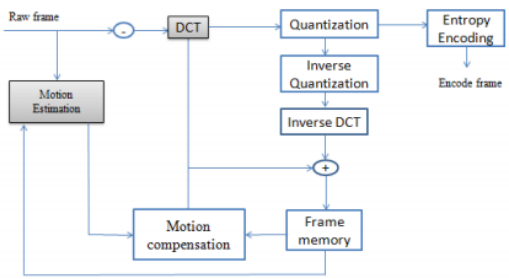

Fig.1 MPEG encoder block diagram

There are three kinds of frames used in MPEG encoding:

1. I-frames means intraframe encoded.
2. P-frames means predictive encoded.
3. B-frames means bidirectional encoded.

I-frame is encoded as it is without any data loss and usually precedes each MPEG data stream. P-frames are constructed using the difference between the current frame and the immediately preceding I or P frame.

B-frames are produced neighbor to the closest two (I/P) frames on either side of the current frame. The I, B and P frames are compressed when subjected to DCT. It is used to remove the existing frame. A significant portion of the interframe encoding is spent in calculating motion vectors (MVs) from the computed differences.

Every non encoded frame is divided into Macro blocks (MBs), such as 16 × 16 pixels. The Motion vectors (MVs) actually contain the information regarding the relative displacements of the Macro blocks (MBs) in the present frame in comparison with the reference.

Quality of a video:

The advantage of encoding operation s used to find from the output quality of the decoded video peak signal-tonoise ratio (PSNR), SAD, and so on are used to measuring the quality of video. PSNR metric as a means of video quality estimation. PSNR of a video means the average PSNR over a constant number of frames (50) of the video.

II. PROPOSED ARCHITECTURE

Reconfigurable Adder/Subtractor Blocks In degree of approximation is dynamically varied which can be done when each of the adder/subtractor blocks with one or more of its approximate copies. Reconfigurable Adder/Subtractor blocks are able to switch between them as per requirement and can include any approximation version of these blocks. 1-bit dual mode full adder is consists A, B, Cin are the inputs and outputs are Sum = A and Cout = A. When each full adder (FA) cell of the adder/subtractor with a dual-mode full adder (DMFA) from the proposed scheme.

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In which each full adder cell can perform operating either in fully accurate or in some approximation mode depending upon the state of the control signal APP. When operating in the approximate mode the full adder act as power gated.Dual-mode full adder can operated in either the two approximation modes. Approximation was selected for its higher probability of giving the accurate output result than the truncation. In which does not variably outputs 0 irrespective of the input.

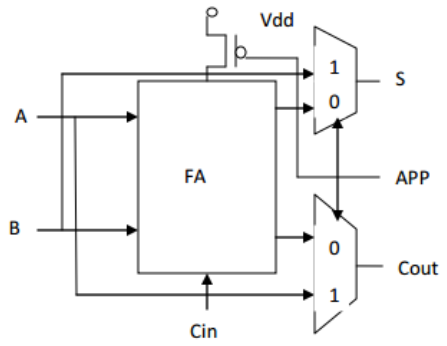

Fig.2 1-bit DMFA

In figure 2 shows the logic block diagram of the dual mode full adder cell (DMFA), when replace the constituent full adder cells of an 32-bit Ripple Carry Adder as shown in the figure of 3. In addition, it is also consists of the approximation controller for generating the appropriate select signals for the multiplexers. From the point of controlling the approximation magnitude

TABLE 1

POWER CONSUMPTION OF DIFFERENT DMFA MODES

Original FA(μw)	DMFA accurate mode(μw)	DMFA approximate mode(μw)
1.53	1.74	0.01

By using a Multimode full adder cell. Because multimode full adder cell would provide even a better alternative to the dual-mode full adder. It also improve the complexity in the decoder block, it is used for select the right signals to the multiplexers as well as logic overhead for the multiplexers themselves.

DMFA overhead:

Dual-mode full adder is consists the power gating transistor and the multiplexers are design to incur the possible overhead.

Dual-Mode full adder experiments show that the switching power of the CMOS transistors contributes toward the most of the total power consumption of the full adder and dual-mode full adder blocks. Table 1 shows Difference between the power consumption of the full adder and dual-mode full adder for different modes obtained by Xilinx 13.2 version. It shows that the power improved by 0.21μw when we operate Dual-mode full adder in accurate mode as compared to the original mode. It shows the power consumed during the dual-mode full adder approximate mode is almost removed when compared with the accurate mode. In which is due to power gating of the full adder block by the Pmos transistor. To reduce the input switching activity of the multiplexers is also a secondary cause for this low amount of power.

The additional overhead is used to switching of the power gating transistor can be rejected, hence it is switching algorithms. This is mainly due to the spatial and temporal locality of the pixel values across the consecutive frames.The concept of the adder/subtractor blocks is extend to other adder architectures as well. Adder architecture is consists CBA and CSA, which also contain full adder as the fundamental building blocks, can be made accuracy configurable by direct substitution of the full adders with DMFAs.

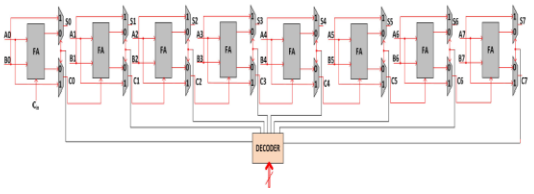

Fig.3. 8-bit reconfigurable RCA blocks

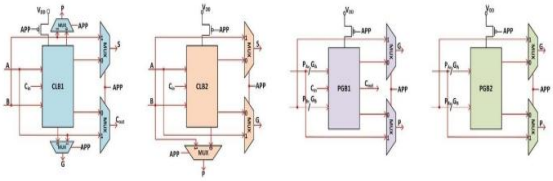

Fig. 4 1-bit dual-mode carry propagate generate blocks.

As an example, I implemented a 32-bit carry look ahead adder consisting four different types of basic blocks figure 5 depending upon the presence of sum

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(s), Cout, carry propagation (P), and carry generation (G) at different levels. To address this blocks present at the first level or the lowest level of a carry look ahead adder (CLA), which have inputs is coming directly, as carry look ahead adder blocks, such CLB1 and CLB2. The difference among the CLB1 produces an additional Cout signal compared with CLB2. Their corresponding to the dual-mode versions, DMCLB1 and DMCLB2, have both sum S and propagate P approximated by input operand B and both Cout and generate G approximated by input operand A, as shown in figure 4. The basic blocks present in the higher levels of carry lookahead adder CLA hierarchy are represented as the configurable as propagate P and generate G blocks, PGB1 and PGB2.

In this case PGB1 generate an extra Cout output as compared with PGB2. As shown in figure 4, the configurable dual-mode versions, DMPGB 1 and DMPGB 2, use inputs Pa and Pb as approximations for outputs propagate and generate. These approximations ensuring that the ratio of the probability of match output to the additional circuit overhead for each of the blocks is large. Table 2 shows and realize the additional circuit overhead for each of the Dual-mode full adder blocks. When operating in either accurate or else approximate mode. Reconfigurable of Carry lookahead adder (CLA), Dual-mode carry look ahead blocks such as DMCLB1 and DMCLB2 blocks are approximated in according with the Dual-mode (DA).

However the Dual-mode propagate generator blocks such as DMPGB1 and DMPGB2 blocks approximated when each and every Dual-mode carry propagate generator blocks such as DMCLB1, DMCLB2, DMPGB1 and DMPGB2 block, which belongs to the transitive fan-in cones of the concerned block is approximated. Otherwise, the block is performed in the accurate mode. For example, any Dual-mode propagate generator blocks (DMPGB) block at the second level of the carry look ahead adder (CLA) can be performed in approximate mode, and both of its constituent DMCLB1 and DMCLB2 blocks are performed in the approximate mode.

In each DMPGB block can be approximated only when both of its constituent DMPGB1 and DMPGB2 blocks are approximated. This architecture can be realize extrapolated to other similar type Carry look ahead adders (CLAs), and so on.

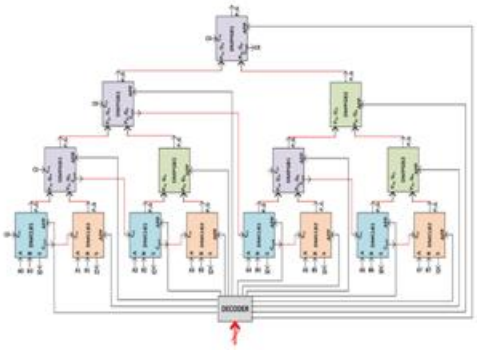

Figure.5 8-bit reconfigurable CLA block

TABLE 2
DUAL-MODE BLOCK OUTPUTS FOR ACCURATE AND APPROXIMATE MODES

Basic block (adder type)	Output for APP=0 (accurate mode)	Output for APP=1 (approximate mode)
DMFA (RCA,CBA,CSA)	S=A+B+Cin	S=B Cout=A
DMCLB1 (CLA)	P=A+B G=AB S=P+Cin Cout=G+PCin	P=B G=A S=B
DMCLB2 (CLA)	P=A+B G=AB S=P+Cin	P=B G=A S=B
DMPGB1 (CLA)	P=PA PB G=GB+GAPB Cout=G+PCIN	P=PA G=GB Cout=G+PCin
DMPGB2 (CLA)	P=PA G=GB	

III.RESULTS:

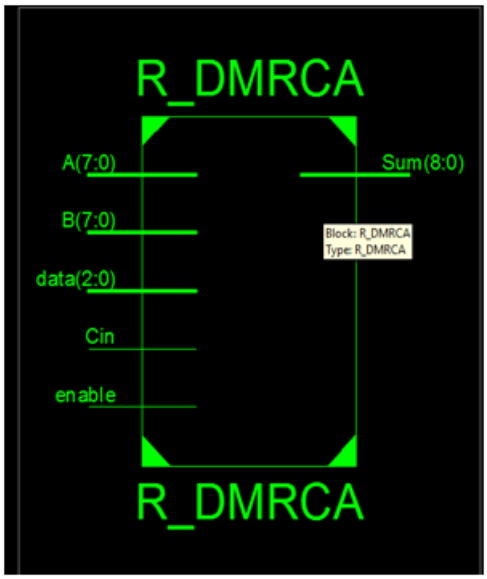

Figure.6 RTL schematic of 8-bit reconfigurable CLA block

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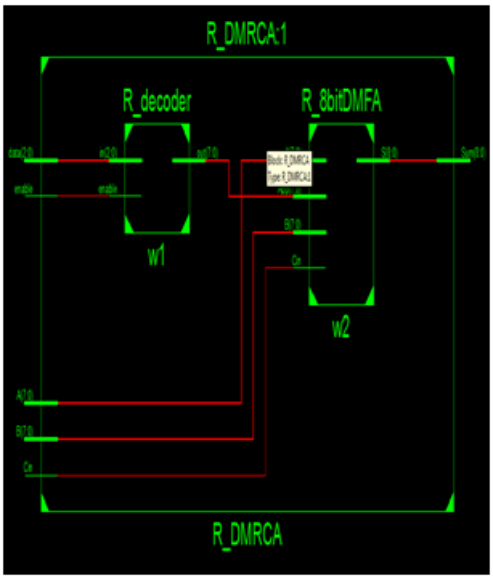

Figure.7 Sub RTL schematic of8-bit reconfigurable CLA block

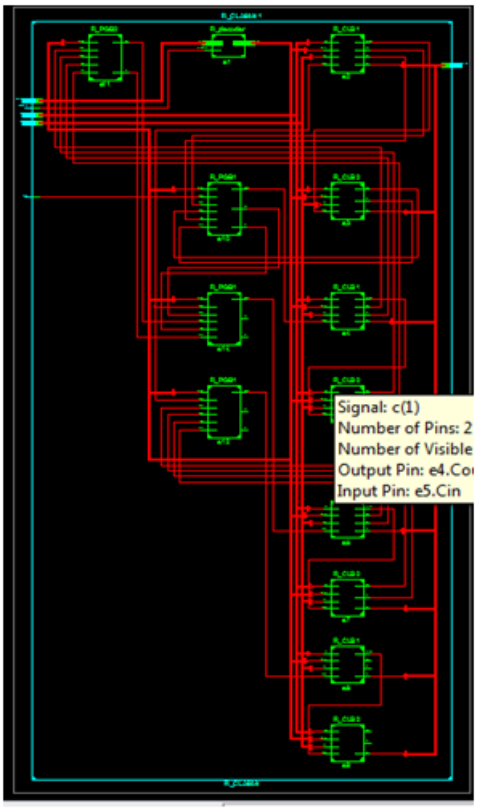

Figure.8 Technology schematic 8-bit reconfigurable CLA block

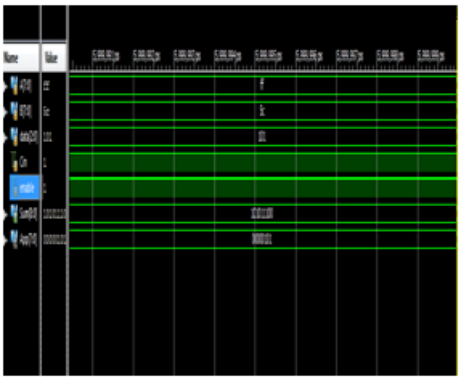

Figure.9 Simulation output for 8-bit reconfigurable CLA block

IV.CONCLUSION:

Background Subtraction Technique is a better algorithm when compared with the other two algorithms, in detecting moving objects. Due to its unique technique of selecting the background image, it is less complex and consumes less amount of memory as background image will be stored once at the time of initializing. Since background image will not be stored again and again computation time required for this process is less. By implementing Morphological Techniques the exact shape of the moving object can be acquired. Moving Object can be detected. Blurriness can be further reduced. And in depth details of the moving object can be acquired, due to the memory limitations on the FPGA board entire algorithm could not be implemented on the hardware module. Moving Object can be detected directly from the hardware module. The response on the hardware for performing Background Subtraction process on the background frame and foreground frame is much faster when compared with the response on implementing the same algorithm on software. This technique can be implemented in applications like High – level computer vision tasks such as robot navigation, collision avoidance, path planning and video surveillance, Computer guided Surgery, Study of anatomical Structure, Face Recognition. As this technique consumes less power when implemented on Hardware, Provide High Performance, Area Consume is very low.

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