ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Implementation of Sequential Counters Using Reversible Logic Gates with Mach-Zehnder Interferometer

A.Rudramadevi
M.Tech(ES & VLSI Design),
Nalgonda Institute of Technology and Science.

P.Lachi Reddy, M.Tech,(Ph.D)
Professor,
Nalgonda Institute of Technology and Science.

Abstract:
This work presents all optical reversible implementation of sequential counters using semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) switches. With the advancements in semiconductor technology, there has been an increased emphasis in low-power design techniques over the last few decades. Reversible computing has been proposed by several researchers as a possible alternative to address the energy dissipation problem.

Several implementation alternatives for reversible logic circuits have also been explored in recent years, like adiabatic logic, nuclear magnetic resonance, optical computing, etc. Recently researchers have proposed implementations of various reversible logic circuits in the all-optical computing domain. Most of these works are based on semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI), which provides desirable features like low power, fast switching and ease of fabrication.

All the designs are implemented using minimum number of MZI switches and garbage outputs. This design ensures improved optical costs in reversible realization of all the counter circuits. The theoretical model is simulated to verify the functionality of the circuits. Design complexity of all the proposed memory elements has been analysed.

Keywords:
Reversible computing, Mach-Zehnder Interferometer (MZI), counter, optical cost, optical delay, garbage.

I. INTRODUCTION:

Like Boolean logic functions, reversible logic function [1-3] is a special type of logic function where there always exists a bijective mapping between inputs to outputs. For a given reversible function, it is always possible to extract original inputs from its outputs correctly, that means it ensures no loss of information while retrieving original data. The concept of reversible logic was first introduced by Landauer [1] and Bennet [4]. According to their claims, if a process or function is reversible, then there is no loss of information which causes heat generation from the system. They also experimentally established that a certain amount of energy ($KTlogn_2$Joules) would be dissipated as heat in the traditional logic computation for every bit of information loss during the computing process. So, it is seen that if a logic circuit can be made reversible, then it ensures zero heat dissipation [2] and no loss of information characteristics.

The problems with traditional logic circuit has been highlighted by Ralph Merkle from Xerox PARC, who experimented [6] on 1GHz computer processor packed with 1018 traditional logic gates in a volume of 1 cm3operating at a room temperature and found that a huge amount of power nearly 3MW releases from the surface area of that processor. Now a day's, the VLSI industry is facing serious challenges due to the heat generation problem in Integrated Circuits (IC) and this problem will become severe in next 10-20 years according to Moore's Law [7] due to the increasing miniaturization and the exponential growth of number of transistors in integrated circuits. To address these issues, the reversible computing has evolved as an alternative as it promises zero power dissipation [2] in the several emerging technologies like ultra low power

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

CMOS design, optical computing [5], nanotechnology [6] and DNA computing [1]. Design of the reversible carry-look-ahead adder using control gate and its physical implementation have been first reported in [8] where the circuit is powered by their input signals only and does not need any additional power supplies. Recently, the researchers are aiming at the development of the optical digital computer system for processing binary data using optical computation. Photons are the source of optical technology. This photonic particle provides unmatched speed with information as it has the speed of light. The installation of optical components in the electronic computer system produces optical-electronic hybrid network. The researchers are trying to combine the optical interconnects with the electronic computing devices. The implementation of reversible logic circuits with optical technology can be performed using Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches which has significant advantages of the high speed, low power, fast switching time and ease of fabrication [11-10].

The optical computing concept in design and synthesis of reversible logic circuit has first been introduced in [12]. Generalized implementation of reversible gate like Toffoli, Fredkin, and CNOT using optical technology has been reported in [10], where Mach–Zehnder interferometer (MZI) is used to implement all-optical reversible logic gates. Reversible implementation of NOR gate using SOA based MZI switches is realized in [11]. The optical implementation of functionally reversible Mach-Zehnder Interferometer based binary adder has been proposed in [12], where two new optical reversible gates ORG-I and ORG-II have been proposed in addition to existing Feynman gate to implement the architecture. The implementation of All-optical XOR gate using SOA-based MZI and micro resonators has been reported in [13] and [14], respectively. Apart from use of MZI to design reversible gates, TOAD (terahertz optical asymmetric de-multiplexer)-based and alloptical fiber-based implementation of Fredkin gate is presented in [15] and [16], respectively.

The sequential circuit is one of the most important components of the computer system and the efficient of the memory element is a primary concern in this circuit. As the reversible circuit promises information lossless and no heat generation property, an intensive research is going on design and implementation of the sequential circuit using reversible technology. In the initial phase of the reversible logic circuit design, the researchers have primarily focused on the design and implementation of the reversible combinational circuits because the researchers have predicted that the feedback is not allowed in reversible computing. However, based on his fundamental work reported in [3], Toffoli argued that “a sequential network is reversible if its combinational part (i.e., the combinational network obtained by deleting the delay elements) is reversible” i.e. feedback can be allowed in the reversible computing. The first design of the reversible sequential circuit with JK latch having the feedback loop from the output has been presented by Fredkin in [19].

Further, Rice has also proved in [17] that the sequential reversible networks are also reversible in nature. The necessity for the sequential reversible logic is discussed by Toffoli [3] and Frank [18], but any structure for its realization has not been presented. The first realization of sequential element in the form of a JK flip-flop using conservative logic has been proposed by Fredkin and Toffoli [19]. Picton has presented a reversible RS-latch in [22]. But Picton's model faces one problem that this model cannot avoid fan-out problem which is essential property of the reversibility. This fan-out problem of Picton's model [22] has been solved by Rice [17] in 2006. In [18], Rice has implemented reversible RS latch. Recently, Rice [20] has analyzed the design of the reversible RS latch in details. The work proposed in [21] has shown that how transistor can be used to design reversible sequential circuit from the physical implementation point of view. Till date, insufficient number of works on reversible memory element has been reported.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Some preliminary works on the reversible implementation of latches, flipflops, shift register, counters using quantum technology have been reported. We have reviewed works where all optical functionally reversible gates are designed by various researchers. Getting inspired by the existing works in the domain of reversible implementation of sequential circuits, after several investigations we have focused on the designing of all optical implementation of reversible counters.

II. BACKGROUND

In this section, first, the fundamental of reversible logic and circuit is introduced. Next, the optical architecture of MZI switch and its working principle are explained. Design of basic reversible gates like CNOT, Toffoli, and Fredkin using all optical MZI switches are presented [10-11].

A. Reversibility:

A fan-out free circuit (Cnf) with circuit depth (d) over the set of input lines X ={x1, x2, …,xn} is said to be reversible (Rc) if the mapping from input to output is bijective (f : Bm_ Bn) and the number of inputs (m) is equal to number of outputs (n) i.e. m = n and also the circuit consists of reversible gates (g_i) only i.e. Cnf=g_0 .g_1.g_2. … .$g_{(d-1)}$,where $g_i$represents i^{th} reversible gate of the circuit.

B. MZI Architecture:

Design of reversible logic gates like NOT, k-CNOT, Toffoli, Fredkin, Peres may be possible in many ways. Among them, the quantum and optical technology are two very prominent. From the quantum technology point of view, the basic quantum gates such as NOT, CNOT, V and V+ are used to implement the reversible gates. In optical domain, MZI based optical switches are used to implement optical reversible gates [10-11].
An optical MZI switch can be designed using the following components: two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C-1, C-2) as shown in Fig. 1. MZI switch has two inputs ports namely, A and B and two output ports known as bar port and cross port, respectively.

The optical signals coming at port B and port A at the input side are the control signal (2), and the incoming signal (1), respectively. The working principle of a MZI is explained as follows.

• When both incoming signal at port A and control signal at port B are high (i.e. A=1, B=1), then the light will appear at the output bar port and no light is seen at the output cross port.

• Again, due to the absence of control signal at input port B and the presence of incoming signal at input port A (i.e.A=1, B=0), then the light appears at the output cross port and no light at the output bar port is observed.

• In all other cases, (i.e. A=0, B=1 and A=0, B=0), no light appears at output bar port and output cross port. The logic values of the absence of the light and the presence of light are denoted by 0 and 1, respectively. From the perspective of boolean functions, the above behavior of MZI switch can be written as R (Bar Port) =A.B and S (Cross Port) =AB'.

C. Beam Combiner (BC) and Beam Splitter (BS):

Beam combiner (BC) simply combines the optical beam while the beam splitter (BS) splits the beam into two optical beams. According to [11-12], the optical cost and the delay of beam combiner and beam splitter are very negligible. Hence, while calculating optical cost of a circuit, they are assumed to be zero.

D. Optical cost and delay

As the optical cost of BS and BC is comparatively small, the optical cost of a given circuit is the number of MZI switches required to design the realization. Optical delay is estimated as the number of stages of MZI switches multiplied by a unit Δ

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

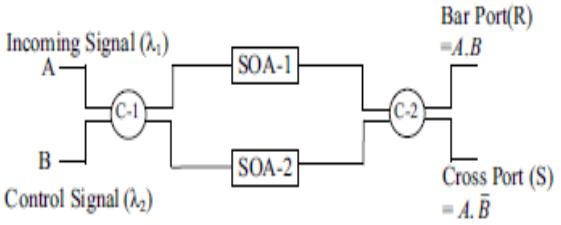

Fig. 1: Semiconductor Optical Amplifier based MZI Switch

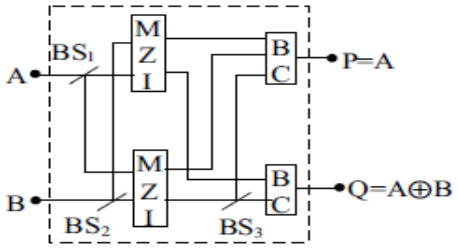

Fig. 2(a): MZI based opticalimplementation of Feynman gate

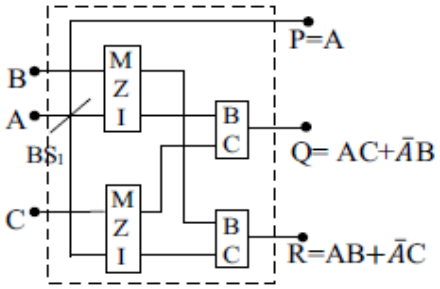

Fig. 2(b): MZI based opticalimplementation of Fredkin gate

E. Design of reversible gates with MZI

MZI-based optical design of functionally reversible Feynman and Fredkin gate are depicted in Fig. 2(a) and Fig. 2(b), respectively. Standard optical cost and delay of some reversible benchmarks are presented in Table-I.

Table-I: Optical cost and delay of reversible gates [10]

Cost Metrics / Reversible Gates	No. of MZI	No. of BS	No. of BC	Optical Cost	Delay
Feynman gate	2	3	2	2	Δ
Peres gate	4	5	3	4	2Δ
Fredkin gate	2	1	2	2	Δ
Toffoli gate	3	4	1	3	2Δ
n-controlled Toffoli gate	*n*+1	*n*+2	1	*n*+1	$(\lceil \frac{n+1}{2} \rceil + 1)\Delta$

III. PROPOSED WORK

In this section, we present all optical implementation of counters with the property of functional reversibility. Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches are used to design the sequential circuits. Our primary objective in this work isto achieve the reversible implementation of counters with minimum number of ancilla lines and MZI switches. All optical implementation of MZI-based asynchronous and synchronous counter is presented. Mathematical model to simulate the proposed architecture has also been presented.Finally, design complexities of all the counters are analyzed.

A. Asynchronous Counters

Asynchronous counter is known as ripple counter. Design architecture and working principle of all optical functionally reversible asynchronous down counter is presented here. The mathematical model for simulation of this memory element is described.

A.1. Design of 2-bit positive edge triggered down counter

The schematic diagram of MZI based 2-bit positive edge triggered down counter is depicted in Fig. 3(a), which is constituted with two positive edge triggered D flip flops viz. FF-0 and FF-1. Each of the positive edge triggered D flipflop consists of three MZI switches viz. MZI-1, MZI-2 and MZI-3, two beam combiner (BC) namely BC-1, BC-2 and four (expect the last flip flop viz. FF-1) beam splitters namely BS-1, BS-2, BS-3, BS-4. For proper understanding, we discuss the signal flow characteristic of the counter as shown in Fig. 3(a). A light from input port CP (Clock Pulse) directly incidents on MZI- 1 of FF-0 and acts as incoming signal. Similarly, another light signal from input port D0 directly enters into MZI-1 of FF-0 and acts as control signal of MZI-1. The light from bar port of MZI-1(B1) and a part of light from cross port of MZI-3(C3) is combined by BC-1 together to produce control signal of MZI-2. In the same way, the output lights from cross port of MZI-1 (C1) and MZI-2 (C2) are combined by BC-2 and acts as control signal of

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

MZI-3. A constant light signal (denoted by 1) incidents on the beam splitter (BS-1) and splits into two parts, where one part acts as incoming signal of MZI-3 and another part again incidents on another beam splitter (BS-2) and splits into two parts. One part appears to MZI-2 as incoming signal and another part that goes to next flip flop (FF-1) acts as a constant input light signal. The light from the cross port of MZI-3(C3) is the final output Q0 where as another light signal which emits from the cross port of MZI-2 (C2) goes back to port D0 and acts as incoming signal. A part of light comes from BS-5 of FF-0 incident on MZI-1 of FF-1 and acts as clock pulse of FF-1. Again, D1 acts as the input value of FF-1. We have obtained both the signals (clock pulse and input signal) for FF-1 and as the design architecture of FF-1 is same as FF-0, we omitted the control flow description of FF-1.

A.2. Operational principle of 2-bit positive edge triggered down counter

The operational principle of all the optical asynchronous down counter as shown in Fig 3(a), is described below. Here, the presence of light is denoted as 1 state and absence of light is denoted as 0 state.

• **State I:** Let Q0=0 and Q1=0. As D0 is directly connected to Q_0', hence, the value of D0 is 1. Now, the value of clock pulse is 1 i.e., both the control signal and incoming signal are present in MZI-1. Hence, according to the working principle of MZI, only bar port of MZI-1 of FF-0 emits light which incidents on BC-1 and as a result, an output light signal emits from BC-1. On the contrary, the cross port of MZI-1 emits no light which incidents on BC-2. Now, the output signal of BC-1 acts as the control signal of MZI-2 and the input signal of MZI-2 is also present. Therefore, the cross port of MZI-2 emits no light, as a result, no light incidents on BC-2. The output signal of BC-2 emits no light and as a consequence, the control signal of MZI-3 is absent. As the input signal of MZI-3 is present, the cross port of MZI-3 of FF-0 receives light which is the final output Q0 i.e. Q0=1. Now, this Q0 acts as incoming signal of MZI-1 of FF-1 and D1, which is directly connected to the $Q_{1bar,}$ acts as control signal of MZI-1. Therefore, both the incoming signal and control signal are present at MZI-1 as both the value of D1 and Q0 are 1. Hence, the operational principle of FF-1 becomes similar to FF-0 and the cross port of MZI-3 of FF-1 emits light i.e. the final output Q1=1. So the next state becomes Q1=1 and Q0=1.

• **State II:** Now, Q1= Q0= 1. Again the clock pulse (CP = 1) and D0 (equals the value of Q_0') act as incoming signal and control signal of MZI-1 of FF-1 respectively. Hence, only incoming signal is present at MZI-1. According to the working principle of MZI, the bar port of MZI-1 of FF-0 emits no light and cross port of MZI-1 of FF-0 emits light which incidents on BC-2. So the output signal of BC-2 is present that acts as control signal of MZI-3. Again, the input signal of MZI-3 is also present. So the cross port of MZI-3 receives no light i.e. the value of final output Q0=0. This output Q0 acts as incoming signal of MZI-1 of FF-1 and D1 is directly connected toQ1bar. So the value of D1 is 0. As both the incoming signal and control signal are absent at MZI-1 of FF-1, no operation is performed in FF-1. Hence, the final output value of FF-1 does not change and it is same as the previous state's output value of Q1. Therefore, the final output of FF-1 is Q1=1.So the next state becomes Q1=1 and Q0=0.

Table-II: Different States of Asynchronous Positive Edge-triggered Down Counter

Clock Pulse	FF-0				FF-1			
	CP_0	Q_0	D_0 $(\bar{Q}_0)$	Q_0^+	CP_1 (Q_0^+)	Q_1	D_1 $(\bar{Q}_1)$	Q_1^+
First	1	0	1	1	1	0	1	1
Second	1	1	0	0	0	0	1	1
Third	1	0	1	1	1	1	0	0
Fourth	1	1	0	0	0	0	1	0
Fifth	1	0	1	1	1	0	1	1

State III: Now, Q1 =1 and Q0 =0. The value of D0 (directly connected to Q0bar) is 1 and the value of clock pulse is 1 i.e. both the control signal and incoming signal are present at MZI-1. So the situation becomes same as that of FF-0 at first stage. Hence, according to working principle of FF-0 described in first stage, the final output of FF-0 is 1 i.e. Q0=1.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

As Q0 acts as incoming signal of MZI-1 of FF-1 and D1 is directly connected to , so the value of D1 is 0. Therefore, only incoming signal is present at MZI-1 of FF-1. This situation is same as FF-0 of second stage. Hence, according to the working principle of FF-0 as described in second stage, the final output of FF-1 is 0 i.e. Q1=0. So the next state becomes Q1=0 and Q0=1.

• **State IV:** In this state, Q1=0, Q0=1 and the value of D0 (control signal of MZI-1) is 0. As the value of clock pulse is 1, only incoming signal is present at MZI-1 of FF-0. This situation is same as FF-0 of second stage. Hence, according to working principle of FF-0 as described insecond stage, the final output of FF-0 is 0 i.e. Q0=0.

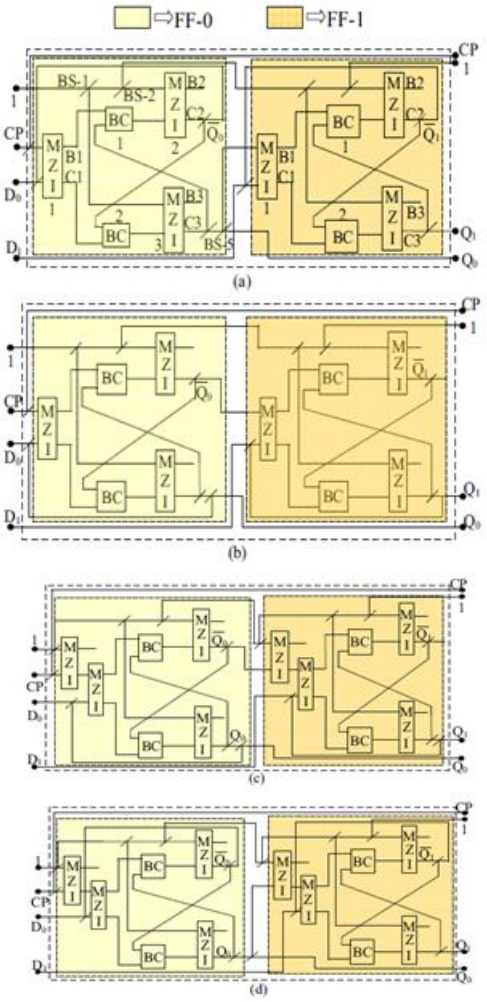

Fig. 3: Design of all optical reversible (a) asynchronous positive edgetriggereddown counter, (b) asynchronous positive edge-triggered upcounter (c) asynchronous negative edge-triggered down counter (d)asynchronous negative edge-triggered up counter using MZI switch.

BC: Beam Combiner; BS: Beam Splitter; CP: Clock Pulse

Now, this Q0 acts as the incoming signal of MZI-1 of FF-1 and D1 is directly connected to complement of Q1. So the value of D1 is 1. As the incoming signal is absent at MZI-1 of FF-1, no operation is performed in FF-1. Therefore, the final output value of FF-1 is not changed and it is same as previous state of Q1. Finally, the output of FF-1 is Q1=0. So the next state becomes Q1=0 and Q0=0. The states of the counter are shown in Table II. The pictorial representation of positive edge triggered asynchronous up counter, negative edge triggered asynchronous down and up counter is depicted in Fig. 3(b), Fig 3(c), Fig 3(d), respectively. MZI switch as shown in Fig. 1(a) are defined [13] as

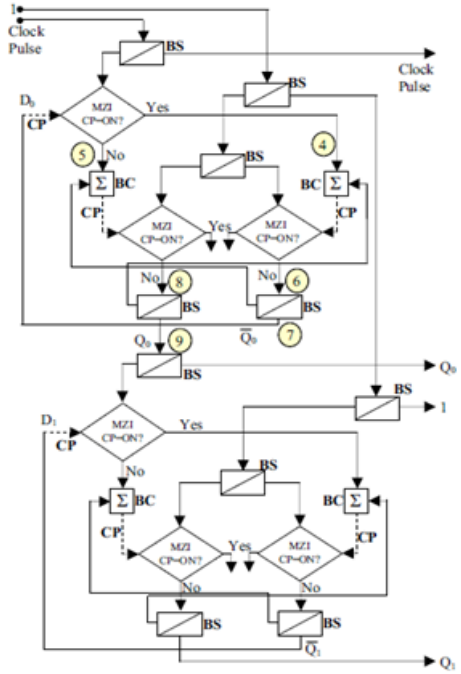

Fig. 3(e): Control flow analysis of Asynchronous Positive edge-triggereddown counter.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

CP: Control Pulse; BS: Beam Splitter; BC: Beam Combiner

A.3. Theoretical model of simulation

In this section, we simulate asynchronous positive edge triggered down counter theoretically using characteristics equation of SOA-based MZI switch. MZI is very powerful optical switch to realize ultrafast all-optical switching. The transmission characteristics at bar port and cross port of

$$T_R(t)=\frac{1}{4}G_1\{k_1k_2+(1-k_1)(1-k_2)R_G - 2\sqrt{k_1k_2(1-k_1)(1-k_2)R_G}\cos(\Delta\varphi)\} \quad \ldots (1)$$

$$T_S(t)=\frac{1}{4}G_1\{k_1(1-k_2)+k_2(1-k_1)R_G - 2\sqrt{k_1k_2(1-k_1)(1-k_2)R_G}\cos(\Delta\varphi)\} \quad \ldots (2)$$

Here RG=G2/G1, where G1 and G2 are time-dependent gain and k1, k2are ratios of couplers of C1 and C2 respectively. We take 50:50 couplers (for simplicity of our calculation) and fixed the values of $k_1$and $k_2$to ½. The output signal power at bar port and cross port of MZI switch is

$$P_j(t)=P_{ip}(t)T_j(t), \quad j=R,S \quad (3)$$

Where Pip(t)=power of incoming signal. Using the previous equations power at the different ports of FF-0 can be expressed as

$$P_{B1}(t)=\frac{1}{2}P_{CP}(t)T_R(t). \quad (4)$$

$$P_{C1}(t)=\frac{1}{2}P_{CP}(t)T_S(t). \quad (5)$$

$$P_{C2}(t)=\frac{1}{4}P_1(t)T_S(t). \quad (6)$$

$$P_{\overline{Q_0}}(t)=\frac{1}{2}P_{C2}(t). \quad (7)$$

$$P_{C3}(t)=\frac{1}{4}P_1(t)T_S(t). \quad (8)$$

$$P_{Q_0}(t)=\frac{1}{2}P_{C3}(t). \quad (9)$$

Similarly, the output power of the different ports of FF-1can be expressed in similar way. The flow chart of this simulation is shown in Fig. 3(e).The equation numbers are given with respect to each output power in the flowchart.

B. Synchronous Counter

In the synchronous counter, all the flip-flops are triggered simultaneously. As we have already explained the working principle of asynchronous counter with detailed diagram, here only the pictorial representation of all optical reversible architecture of MZI based synchronous up counter (negative edge triggered) and down counter (positive edge triggered) is depicted in Fig. 3(f) and Fig. 3(g), respectively. Analysis of design complexities of all optical reversible counters is presented in table III.

Table III: Analysis on design complexities of all optical reversible counters

Different types of n-bit counters		No. of MZI (Optical Cost)	No. of Beam Combiner	No. of Beam splitter	Garbage Output
Asynchronous	down counter (positive edge-triggered)	3n	2n	6n	4
	up counter(negative edge-triggered)	4n	2n	7n	6
Synchronous	up counter(negative edge-triggered)	4n	2n	7n	6
	down counter (positive edge-triggered)	3n	2n	6n	4

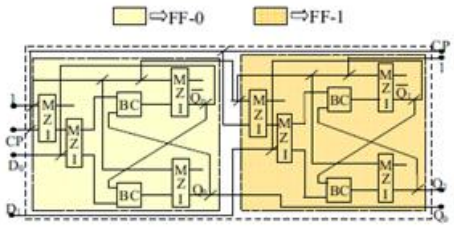

Fig. 3(f): Synchronous negative edge-triggered up counter implementedby MZI switch

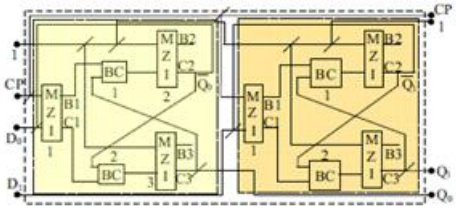

Fig. 3(g): Synchronous Positive edge-triggered down counterimplemented by MZI switch

IV. SYNTHESIS AND SIMULATION RESULTS:

We have coded the reversible sequential counters in Verilog HDL using the proposed with Mach-Zehnder Interferometer design and the existing sequential counters designs of [6] and [7] . All the designs are synthesized with the Xilinx Synthesis Tool and Simulated using Xilinx ISE simulator. The simulation results are shown below.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

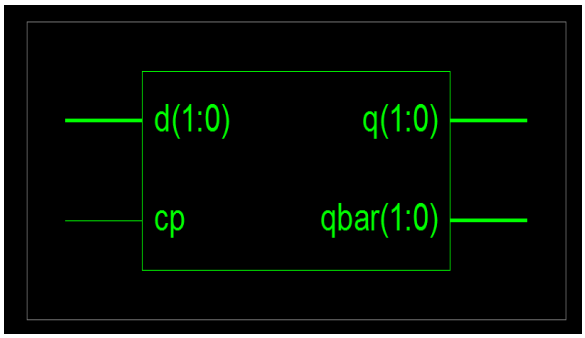

Figure 4: RTL schematic of Synchronous Positive edge-triggered down counter

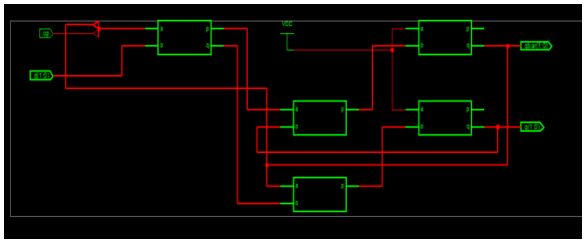

Figure 5: RTL schematic of Synchronous Positive edge-triggered down counter

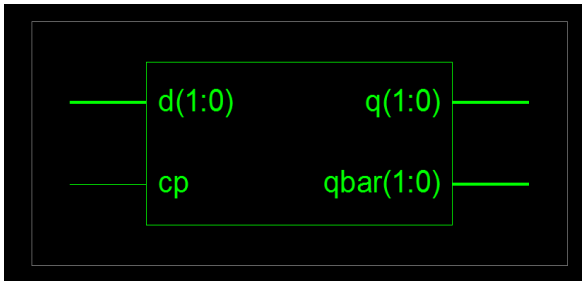

Figure 6: Technology schematic of Synchronous Positive edge-triggered down counter

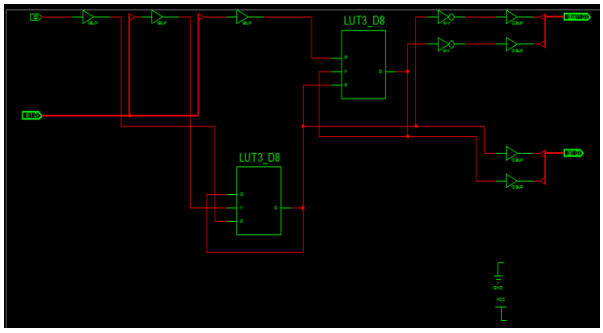

Figure 7: Technology schematic of synchronous positive edge-triggered up counter

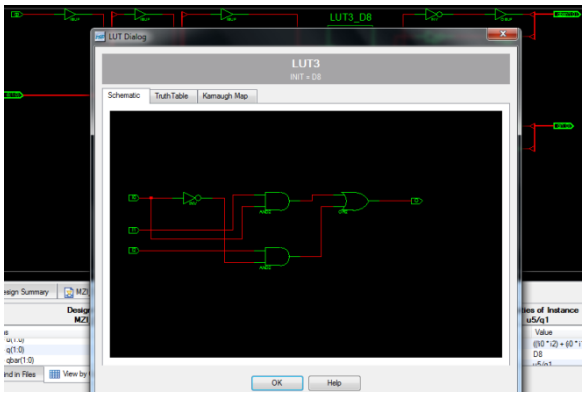

Figure 8: Internal block of synchronous positive edge-triggered up counter

Table IV: Synthesis report of asynchronous positive edge-triggered up counter

MZI_COUNTERS Project Status			
Project File:	MZI_COUNTERS.ise	Current State:	Synthesized
Module Name:	MZI_COUNTB	• Errors:	
Target Device:	xc3s200-4ft256	• Warnings:	
Product Version:	ISE 9.2i	• Updated:	Fri Dec 18 18:06:57 2015

MZI_COUNTERS Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	1920	0%
Number of 4 input LUTs	4	3840	0%
Number of bonded IOBs	7	173	4%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Dec 17 11:40:28 2015			
Translation Report					
Map Report					
Place and Route Report					

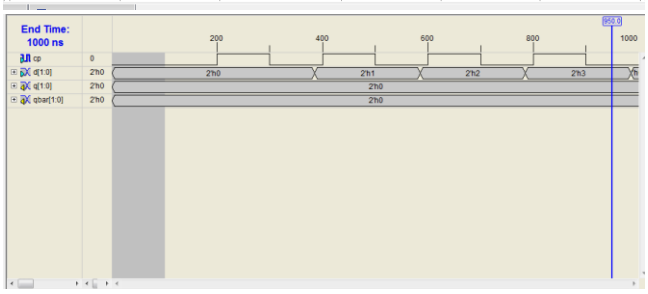

Figure 9: Test Bench for asynchronous positive edge-triggered up counter

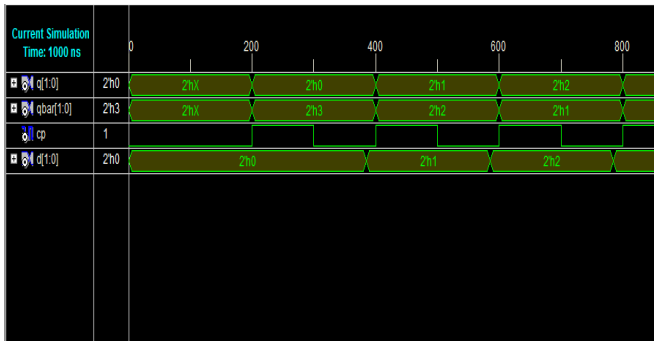

Figure 10: Simulated output for asynchronous positive edge-triggered up counter

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

V.CONCLUSION

In this work, various architectures of MZI based functionally reversible all optical counters have been proposed. As far as our knowledge is concerned, the design of reversible all optical counter is a newer one. Our proposed design can be generalized for n-bit counter also. The proposed design techniques implement all the optical functionally reversible counters with minimum number of ancillary lines and minimum optical cost. Mathematical model has also been formulated.

FUTURE WORK

We can extend this project n bit counters low garbage outputs based reversible logic gates and we can also design all combinational circuits with novel reversible logic gates.

REFERENCES

[1] R. Landauer "Irreversibility and heat generation in the computing process", IBM Journal of Research and Development, 5:183–191, July 1961.

[2] C. H. Bennett "Logical reversibility of computation. IBM Journal of Logical Research and Development", 6:525–532, November 1973.

[3] T.Toffoli, "Reversible computing", Tech. Memo-MIT/LCS/TM-151, MIT Lab for Comp. Sci, 1980.

[4] C. H. Bennett, "Notes on the history of reversible computation", IBM Journal of Research and Development, 32:16–23, January 1988.

[5] R. Cuykendall, D.Andersen, "Reversible optical computing circuits", Optics Letters 12(7), 542-544 (1987).

[6] R.Merkle, "Reversible electronic logic using switches", Nanotechnology 4, 21-40 (1993).

[7] G. E. Moore "Cramming more components onto integrated circuits", Electronics, 38, January 1965.

[8] B.Desoete, A.De.Vos, " A reversible carry-look-ahead adder using control gates", INTEGRATION the VLSI Jour. 33(1-2), 89-104 (2002).

[9] M. Nielsen and I. Chuang, "Quantum Computation and Quantum Information", Cambridge Univ. Press, 2000.

[10] C. Taraphdara, T. Chattopadhyay, and J. Roy, "Mach-zehnder interferometer-based all-optical reversible logic gate," Optics and LaserTechnology, vol. 42, no. 2, pp. 249–259,2010.

[11] Kotiyal, S ,Thapliyal, H. and Ranganathan, N. "Mach-Zehnder Interferometer Based All Optical Reversible NOR Gates". IEEE Computer Society Annual Symposium on VLSI.2012.

[12] S. Kotiyal, H.Thapliyal, N. Ranganathan, "Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder", DATE 2012, pp. 721 –726.

[13] M. Zhang, Y. Zhao, L. Wang, J. Wang, and P. Ye, "Design and analysis of all-optical XOR gate using SOA-based Mach- Zehnder interferometer," Optical Communications, 223:301–308, 2003.