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Design of Carry Select Adder with Binary Excess Converter and Brent Kung Adder Using Verilog HDL

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Abstract:
A binary multiplier is an electronic circuit; mostly used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. In this paper, a high speed and low power 16×16 Vedic Multiplier is designed by using low power and high speed carry select adder. Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay.

Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. This paper presents a technique for N×N multiplication is implemented and gives very less delay for calculating multiplication results for 16×16 Vedic multiplier. Comparisons with existing conventional fast adder architectures have been made to prove its efficiency. The performance analysis shows that the proposed architecture achieves three fold advantages in terms of delay-area-power. The synthesis results of the carry select adders and Vedic multiplier has compared with different conventional techniques.

Keywords:
Brent Kung (BK) adder, Ripple Carry Adder (RCA), Regular Linear Brent Kung Carry Select Adder, Modified Linear BK Carry Select Adder, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA; Vedic Multiplier.

I. INTRODUCTION:

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and llR. Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI.

In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder [1] is designed using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by brent kung adder. As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced.

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Also the square root adder architectures of CSA [2] are designed using brent kung adder in order to reduce the power and delay of adder. In this paper, Modified Square Root Carry select Adder using Brent Kung adder is proposed using single BK and BEC instead of dual RCAs in order to reduce the power consumption with small penalty in speed. This paper is organized as follows: In section 2, parallel prefix adders are illustrated. Section 3 explains Regular Linear BK CSA and section 4 give details of Modified Linear BK CSA. In section 5, Regular Square Root BK CSA is elucidated. The structure of Modified Square Root BK Carry Select Adder is enlightened in Section 6. Simulation Results and comparison are evaluated in section 7 and section 8 concludes.

II. PARALLEL PREFIX ADDERS:

Parallel prefix adders [3] are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders [4] . Tree structures are used to increase the speed [5] of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix adder [6] involves three stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

Pre-possessing stage:

Generate and propagate signals to each pair of inputs A and B are computed in this stage. These signals are given by the following equations:

$$P_i = A_i \text{ xor } B_i \quad (1)$$

$$G_i = A_i \text{ and } B_i \quad (2)$$

Carry Generation Network:

In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel.

After the computation of carries in parallel they are segmented into smaller pieces. Carry propagate and generate are used as intermediate signals which are given by the logic equations 3& 4:

$$CP_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \quad (3)$$

$$CG_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \quad (4)$$

The operations involved in fig. 1 are given as

$$CP0 = P_i \text{ and } P_j \quad (3(i))$$

$$CG0 = (P_i \text{ and } G_j) \text{ or } G_i \quad (3(ii))$$

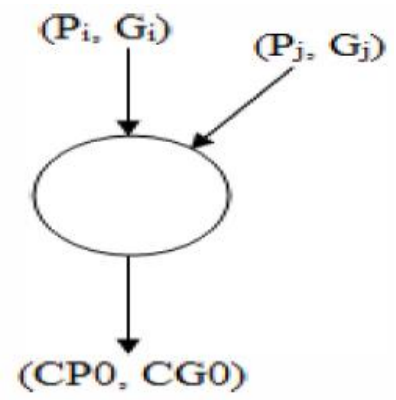

Fig. 1 Carry Network

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 5& 6:

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \quad (4)$$

$$S_i = P_i \text{ xor } C_{i-1} \quad (5)$$

Brent-Kung Adder:

Brent-Kung adder [7] is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in brent kung adders. But the gate level depth of Brent-Kung adders [8] is 0 (log2(n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig. 2.

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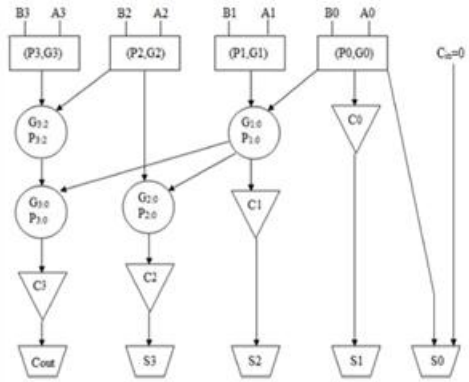

Fig. 2 Block Diagram of 4-Bit Brent Kung Adder

III. REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder [9] has reduced delay as compared to Ripple Carry Adder. So, Regular Linear BK CSA is designed using Brent Kung Adder

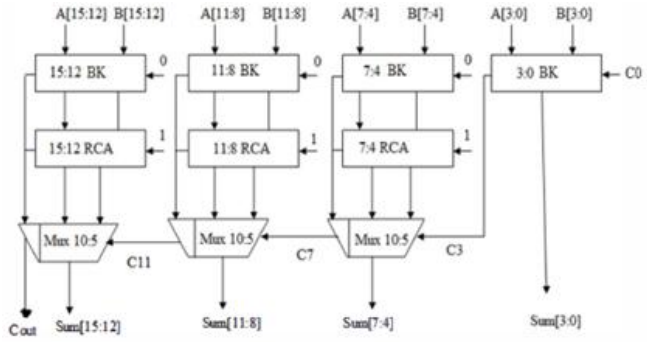

Fig. 3 Block Diagram of 16-bit Regular Linear BK Carry Select Adder

Regular Linear KS CSA consists of a single Brent Kung adder for Cin=O and a Ripple Carry Adder for Cin=1. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung adder to increase the speed of arithmetic operation. The block diagram of Regular Linear BK CSA is shown in Fig. 3. In group 2 of Regular Linear CSA, there are single BK for Cin=O and single RCA for Cin=1.

Now, the C3 tells whether the input carry is 0 or 1 and depending on its value the output of particular block is selected. If C3=0 then the output of BK with Cin=O is selected using 10:5 multiplexer and if C3=1 then output of RCA with Cin=l is selected using the MUX. A 4-bit Sum [7:4] and an output carry, C7 is obtained at the output of group 2.

IV. MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER:

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=O and brent kung adder for Cin=l and is therefore area-consuming. So, different add-one schemes like Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here Brent Kung adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less. A circuit of 4-bit BEC and truth table is shown in Fig. 4 and Table I respectively.

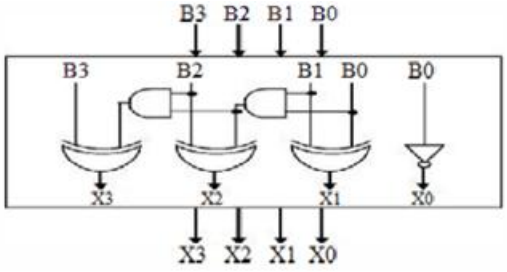

Fig. 4bit Binary to Excess-I code Converter

The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols, - NOT, & AND, /\ XOR).

XO = -BO
Xl = BO (l)/\Bl
X2 = B2 /\ (BO &Bl)
X3 = B3 /\ (BO & B 1 & B2)

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Binary Logic $B_0 B_1 B_2 B_3$	Excess-1 Logic $X_0 X_1 X_2 X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

TABLE I. TRUTH TABLE OF 4-BIT BINARY To EXCESS-I CONVERTER

Linear Modified BK CSA is designed using Brent Kung adder for Cin=O and Binary to Excess-l Converter for Cin=l in order to reduce the area and power consumption with small speed penalty. Linear Modified BK CSA consists of 4 groups. Each group consists of single BK adder, BEC and multiplexer. The block diagram of Linear Modified BK CSA is shown in Fig. 5.

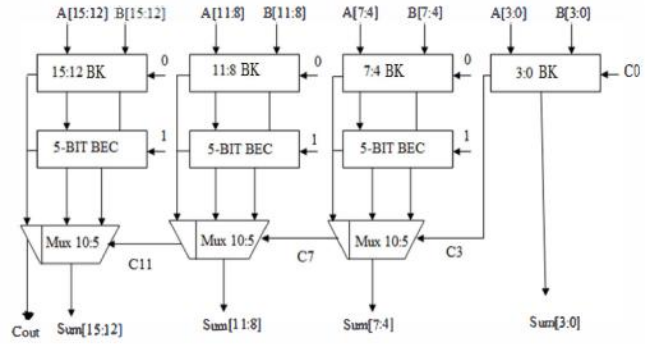

Fig.5 Block Diagram of 16-bit Linear Modified BK Carry Select Adder

To replace the N-bit Brent Kung adder, aN+l bit BEC is required. The importance of BEC logic comes from the large silicon area reduction when designing Linear Modified BK CSA for large number of bits.

V. REGULAR SQUARE ROOT BRENT KUNG CARRY SELECTS ADDER:

Regular Linear Brent Kung Carry Select Adder consumes large area and to reduce its area a new design of adder is used i.e. Regular Square Root Brent Kung Carry Select Adder.

Regular Square Root BK CSA has 5 groups of different size brent kung adder. Each group contains single BK for Cin=O,RCA for Cin=1 and MUX. The block diagram of the 16-bit regular SQRT BK CSA is shown in Fig. 6. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA [10]. It is an improved version of linear CSA. The time delay of the linear adder can decrease, by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder.

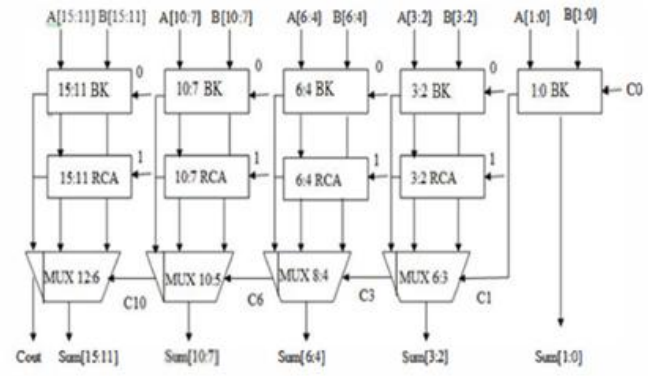

Fig. 6 Block Diagram of l6-bit Regular Square Root BK Carry Select Adder

There are 5 groups in Regular Square Root BK Carry Select Adder [11] . Here single Brent Kung adder is used for Cin=O and ripple carry adder is used for Cin=l and then there is a multiplexer stage. Due to the presence of RCA and BK, this circuit consumes large area.

VI. MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER:

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent kung adder for Cin=O and BEC for Cin=l and then there is a multiplexer stage. It has 5 groups of different size Brent kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area.

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The block diagram of the 16-bit modified Square Root BK Carry Select Adder is shown in Fig. 7.

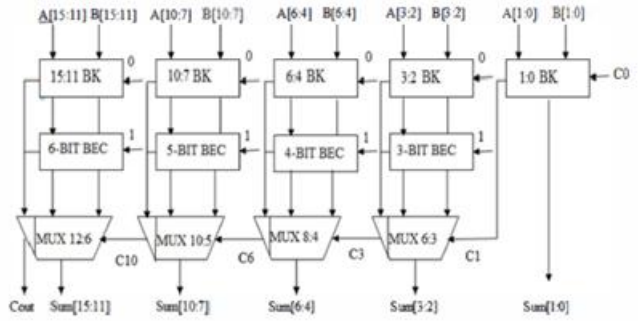

Fig. 7 Block Diagram of 16-bit Modified SQRT BK CSA

Each group contains one BK, one BEC and MUX. For N bit Brent Kung adder, N+ 1 Bit BEC is used.

VII. VEDIC MULTIPLER USING MODIFIED SQRT BK CSA

A high speed and low power 16×16 Vedic Multiplieris designed byusing low power andhigh speed modified c arry select adder. Modified Carry Select Adder employ s a newly incremented circuit in the intermediate stages of the Carry Select Adder (CSA) which is known to be the fastest adder among the conventional adder structures. A Novel technique for digit multiplication namely Vedic multiplication has been introduced which is quite different from normal multiplication by shift and addition operations. Normally a multiplier is a key block in almost all the processors and also introduces high delay block and also a major power dissipation source.

This paper presents a new design methodology for less delay and less power efficient Vedic Multiplier based up on ancient Vedic Mathematic techniques. For clear understanding, observe the block diagrams for 16x16 as shown in Figure8 and within the block diagram 16x16 totally there are four 8x8 Vedic multiplier modules, and three modified carry select adders which are of 16 bit size are used. The 16 bit modified carry select adders are used for addition of two 16 bits and likewise totally four are use at intermediate stages of multiplier.

The carry generated from the first modified carry select adder is passed on to the next modified carry select adder and there are eight zero inputs for second modified carry select adders. The arrangement of the modified carry select adders is shown in below block diagram which an reduces the computational time such that the delay can be decrease.

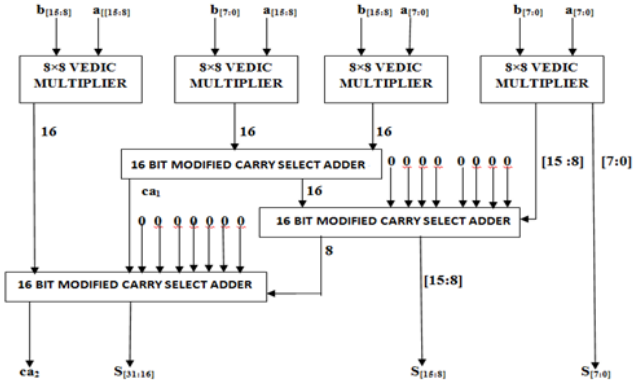

Figure 8 Block Diagram of 16x16 bit Vedic Multiplier

VIII. SIMULATION RESULTS:

We have coded the all carry select adders techniques in Verilog HDL. All the designs are synthesized in the Xilinx Synthesis Tool and Simulated using Xilinx ISE 14.4 simulator. The synthesis and simulation results are as shown below figures.

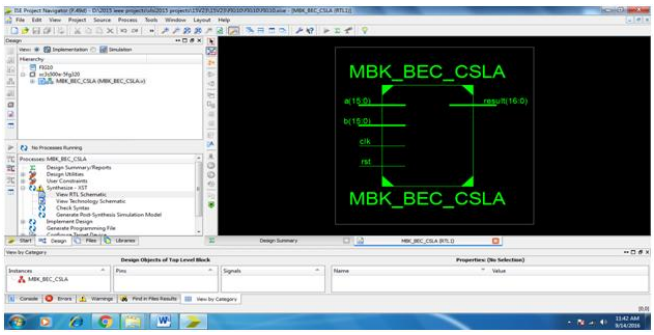

Fig8: Block diagram of 16bit-BK-BEC Carry select adder

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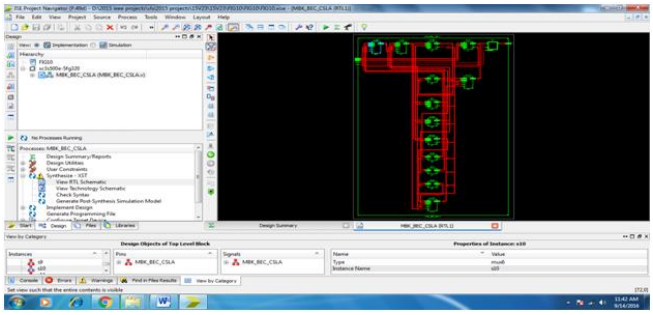

Fig9: RTL Schematic of 16bit-BK-BEC Carry select adder

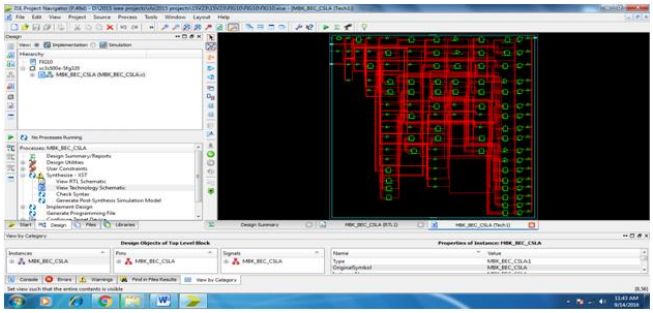

Fig10: Technology Schematic of 16bit-BK-BEC Carry select adder

MBK_BEC_CSLA Project Status (08/30/2016 - 11:16:10)

Project File:	FIG10.xise	Parser Errors:	No Errors
Module Name:	MBK_BEC_CSLA	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	No Errors
Product Version:	ISE 14.4	• Warnings:	4 Warnings (0 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	27	4656	0%
Number of 4 input LUTs	48	9312	0%
Number of bonded IOBs	51	232	21%
Number of GCLKs	1	24	4%

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Sep 3 13:30:11 2016	0	4 Warnings (0 new)	0
Translation Report					

MBK_BEC_CSLA (RTL1) MBK_BEC_CSLA (Tech1)

Fig11: Design summary of 16bit-BK-BEC Carry select adder

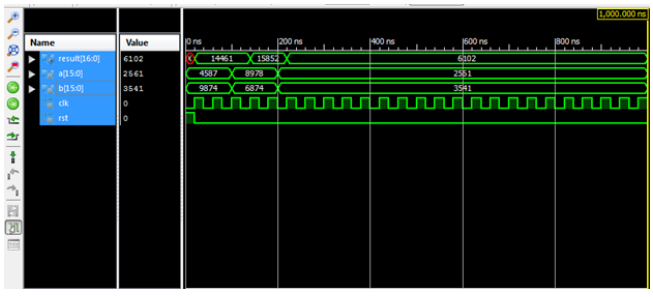

Fig12: Simulation output waveform of 16bit-BK-BEC Carry select adder

VIII.CONCLUSION:

In this work, a Modified Square Root BK Carry Select Adder is proposed which is designed using single Brent kung adder and Binary to Excess-l Converter instead of using single Brent kung adder for Cin=0 and Ripple Carry Adder for Cin=l in order to reduce the delay and area consumption of the circuit. Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular SQRT BK CSA and Modified SQRT BK CSA are designed for 16-Bit word size only. This work can be extended for higher number of bits and Vedic Multiplier also. By using parallel prefix adder, delay and area consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent Kung adder is used. The synthesized results show that delay consumption of Modified SQRT BK CSA is reduced in comparison to Regular Linear CSA.

REFERENCES:

[1] ShivaniParmar and Kirat Pal Singh," Design of High Speed Hybrid CarrySelect Adder", IEEE's 3rd International Advance Computing Conference(IACC) Ghaziabad, ISBN: 978-1-4673-4527-9,22-23 February 2013.

[2] Yajaun He, Chip-Hong Chang, and JiangminGu, "An area efficient 64-Bit square Root carry-select adder for low power Applications, " in Proc.IEEE International Symposium Circuits and Systems, vol. 4, pp. 4082-4085,2005.

[3] M. Snir, "Depth-Size Trade-Offs for Parallel Prefix Computation",Journal of Algorithms, Vo!.7, Issue-2, pp.185-201, June 1986.

[4] David Jeff Jackson and Sidney Joel Hannah, "Modelling and Comparisonof Adder Designs with Verilog HDL", 25th South-eastern Symposium on System Theory, pp.406-4tO, March 1993.

[5] Belle W.Y. Wei and Clark D. Thompson, "Area-Time Optimal Adder Design", IEEE transactions on Computers, vo!.39, pp. 666-675, May1990.

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International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[6] Y. Choi, "Parallel Prefix Adder Design", Proc. 17th IEEE Symposium on Computer Arithmetic, pp. 90-98, 27th June 2005.

[7] J. M. Rabaey, "Digital Integrated Circuits- A Design Perspective", New Jersey, Prentice-Hall, 2001.
[8] R. Brent and H. Kung, "A regular layout for parallel adders", IEEE Transaction on Computers, vol. C-31,n o.3,p p. 260-264,M arch 1982.

[9] AdilakshmiSiliveru, M. Bharathi, "Design of Kogge-Stone and BrentKung adders using Degenerate Pass Transistor Logic", International Journal of Emerging Science and Engineering, Vol.-I, Issue-4, February 2013.

[10] K. Saranya, "Low Power and Area-Efficient Carry Select Adder", International Journal of Soft Computing and Engineering, Vol.-2, Issue-6, January 2013.

[11] DeepthiObul Reddy and P. Ramesh Yadav, "Carry Select Adder with Low Power and Area Efficiency", lnlernalional Journal of Engineering Research and Developmenl, Vol. 3, Issue 3, pp. 29-35, August 2012.

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