ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Three-Level Hybrid Boost Topology for Renewable Energy Systems

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Abstract:
In order to deal with mismatched voltage levels between parallel-connected low-voltage photovoltaic (PV) arrays and the required higher voltage of the grid, a novel hybrid boost three level dc–dc converter is proposed based on the traditional single phase diode-clamped three-level inverter. Only one inductor, two capacitors in series, and those power switches and diodes, which are easy to be integrated, are adopted to establish the topology with transformer less high voltage gain. The operation principle of the proposed topology is analyzed, and then the pulse width modulation (PWM) control method is obtained according to the switching functions about the output pulse voltages of both half-bridges.

Therefore, the proposed converter cannot only operate with high voltage gain, but also make the duty cycles of power switches closer to 0.5. Moreover, voltages across the capacitors in series are well-balanced in both steady and dynamic states, and the blocking voltages of the power switches are half of the output dc voltage. Finally, a 1-kW prototype is set up in our laboratory, and the measured maximum efficiency of the proposed converter is about 93.1%. All experimental results verify the feasibility of the proposed topology and validity of the PWM control method.

Index Terms:
High voltage gain, hybrid boost dc–dc converter, non extreme duty cycles, photovoltaic (PV) generation, three levels.

I.INTRODUCTION:

BOTH photovoltaic (PV) and wind power generations have become important parts of renewable energy sources, due to worldwide exhausted fossil fuel and world's demand for clean energy [1], [2]. In grid-connected PV generation systems, a single-PV array can only supply lower dc voltage, but higher voltage level is demanded for the grid-connected side [3]. Therefore, the mode of PV arrays in series has been adopted to offset the differential voltage levels between dc bus and grid side. Unfortunately, low-voltage PV arrays are always subjected to inevitable cloud, dust, shadow, and so on, which will limit the Manuscript received August 23, 2012; revised October 24, 2012; accepted November 15, 2012. Date of current version January 18, 2013.

This work was supported in part by the Special Scientific and Research Funds for Doctoral Speciality of China Institution of Higher Learning under Grant 20110032120082, and in part by the National Natural Science Foundation of China under Grant51207104. Recommended for publication by Associate Editor C. C. Mi.Y. Zhang and Y.-F. Wang are with the School of Electrical Engineering and Automation, Tianjin University, Tianjin 300072, China (e-mail:zhangy@tju.edu.cn; wayif@tju.edu.cn). J.-T. Sun is with the High Voltage Division, China Electric Power ResearchInstitute, Beijing 100085, China (e-mail: sun.jt@foxmail.com). Color versions of one or more of the figures in this paper are available onlineat http://ieeexplore.ieee.org. Digital Object Identifier 10.1109/TPEL.2012.2229720.

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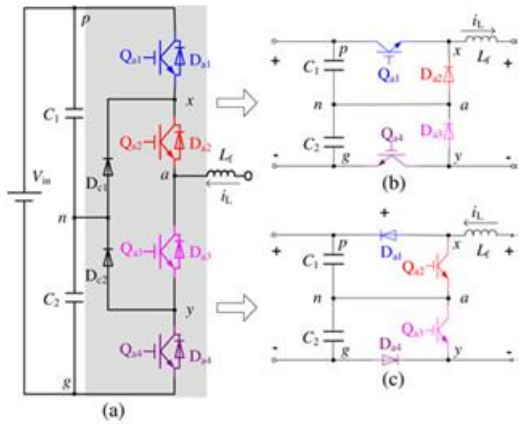

Fig. 1. Single-phase diode-clamped three-level inverter and two classical three-level dc–dc converters.

output current of the total PV arrays, and then the efficiency of the entire PV generation system will be degraded [4], [5].Naturally, the other mode of PV arrays in parallel has also been proposed, and the power generation level can be improved by extending the parallel-connected PV arrays flexibly [6].As to the parallel-connected PV configuration, one of the most important problems is that the low dc-bus voltage has to be boosted with high step-up gain. Therefore, high-step-up dc–dc converters are introduced to fulfill the voltage conversion between low-voltage parallel-connected PV arrays and the demanded high-voltage grid-connected side [7], as well as the maximum power point tracking (MPPT).

When converters operate with high step-up gains, the power switches in conventional boost two-level converters would sustain high output voltage completely. While the classical boost three-level converters shown in Fig. 1(c) could reduce half of the voltage stress [8], but the extreme duty cycles of power switches limit its voltage gains and switching frequency because of the shorter turn-OFF time of the power switches in each switching period. Cascaded boost converters are also used to extend the voltage gain and duty cycles [9], but one obvious disadvantage is that more separated inductors are demanded, and the power switch of the last power stage cannot avoid the output voltage stress.

In recent years, many researchers have focused on step-up converters with coupled inductor, which has the transformer function to extend the voltage gain and duty cycles [10]–[12]. Althoughthe voltage stress of power switches is low, the output-power level is limited and the input- current ripple is large due to

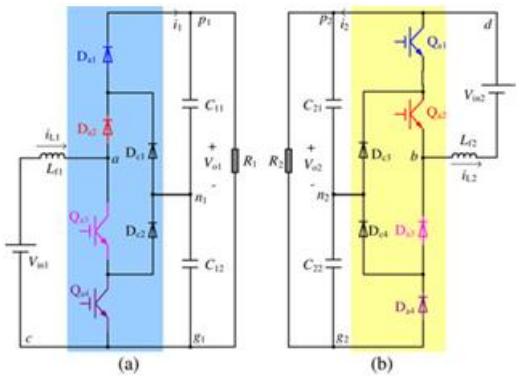

Fig.2. Two deduced boost three-level dc–dc converters.

The single-phase structure. Therefore, the interleaved boost converters with switched capacitors are proposed [13]. However, more switched-capacitor cells are required to obtain a high voltage gain. An interleaved high-step-up converter integrated with winding-cross-coupled inductors and voltage multiplier cells is presented [14], but it sponges on more coupled inductors which are not easy to be integrated or designed in standardization. In addition, the duty cycles of the power switches inclines to 1, due to the increased voltage gain. In this letter, a novel hybrid boost three-level dc–dc converter is proposed, taking the topology established without a transformer or coupled inductors into account. It is composed of only one inductor, two output capacitors in series, and other power semiconductor components, which are easy to be integrated. This proposed converter cannot only realize high step-up gain, but also avoid extreme duty cycles. In Section II, the deduction of the topology synthesis of the hybrid boost three-level dc–dc converter is clarified with the basic topological constraints of pulse width modulation (PWM) converters, based on the topology synthesis technique [15]–[17].

ISSN No: 2348-4845
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The converter's principle of high voltage gain and no extreme duty cycle's operation is explained in Section III. Finally, a 1-kW prototype is set up, and the effective experimental results are obtained.

II.ANALYSIS OF TOPOLOGY SYNTHESIS:

The conventional single-phase diode-clamped three-level inverter is shown in Fig. 1(a), and there are four power switches Qa1 − Qa4 with corresponding antiparallel diodes Da1 − Da4. Based on this topology, two classical three-level dc–dc converters (buck and boost converters) are deduced, as shown in Fig. 1(b) and (c). In fact, there are still two other boost three level converters shown in Fig. 2 [18], which can also be deduced from the inverter in Fig. 1(a). However, these two boost three level converters cannot operate separately, due to the unbalanced capacitor voltages across (C11, C12) or (C21, C22). In order to not only improve the dc-bus voltage and power level of PV generation systems, but also obtain narrower pulse voltages from the difference between wider ones through the idea based on the topology of a single-phase diode-clamped inverter with two three-level legs [19], a novel hybrid boost three

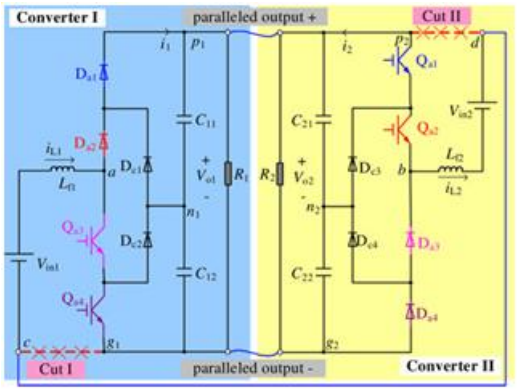

Fig. 3. Synthesized process of the hybrid boost three-level dc–dc converterby the mode of inputs in series and outputs in parallel.

level converter can be synthesized by the two boost three-levelConverters I and II in Fig. 2 naturally. Vin1, Vin2 and Lf 1, Lf 2are the input dc voltages and filtering inductors of Converters I and II, respectively.

Then, the input power level of the hybrid converter can be improved by means of two converters' input sides in series, namely (Vin1 + Vin2), and the output power level of the hybrid converter can also be increased by the parallelconnectedoutputs of Converters I and II, namely (i1 + i2) as shown in Fig. 2. Therefore, the synthesized process of the hybrid converter by the mode of inputs in series and outputs in parallel is depicted in Fig. 3. The input node c is cut-off from node g1 in Converter I, which is denoted "Cut I." In addition, the other input node d is also cut-off from node p2 in Converter II, which is shown as "Cut II." Then, the two input nodes c and d can be connected in series, namely both of the input dc voltage supplies Vin1 and Vin2 are in series. While the output structures of Converters I and II are identical, nodes p1 and p2, as well asg1 and g2 can be connected in parallel, leading to the "paralleled output +" and "paralleled output –" for the hybrid converter as shown in Fig. 3.

The synthesized hybrid boost three-level converter is shown in Fig. 4, the equivalent input dc voltage Vin and inductor Lf can be obtained linearly due to the input sides of Converters I and II in series. In addition, the parallel-connected capacitors (C11, C12) and (C21, C22) as shown in Fig. 3, can be equivalent to Cf 1and Cf 2 in Fig. 4, as well as the parallel-connected load resistors R1 and R2 which are equivalent to RL . However, the neutral points n1 and n2 in Fig. 3 have to be connected together, leading to the neutral point n that may keep the blocking voltages across power switches as the corresponding capacitors' voltages in Fig. 4. Therefore, the proposed hybrid converter, which is synthesized by Converters I and II in Fig. 2, comprises Half-Bridges I and II, as shown in Fig. 4.

III.OPERATION PRINCIPLE OF TOPOLOGY

A. Operation States of Topology

According to Fig. 4, the output pulse voltages of two halfbridges are Vag and Vbg , and then the output pulse voltage Vab of the hybrid converter can be described as

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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$$V_{ab} = V_{ag} - V_{bg}. \qquad (1)$$

As a result, the output dc voltage Vpg = Vo can be obtained from Vab , filtering by capacitors Cf 1 and Cf 2. The corresponding states of power components for instantaneous Vab of the hybrid converter are listed in Table I, and it is also assumed that the voltages across capacitors Cf 1 and Cf 2 are equal, namely VCf 1 = VCf 2 .When the power switches Q1 − Q4 are turned OFF, the capacitors Cf 1 and Cf 2 in series are charged together by both the dc voltage source Vin and the energy stored in Lf through diodes D1 − D4.

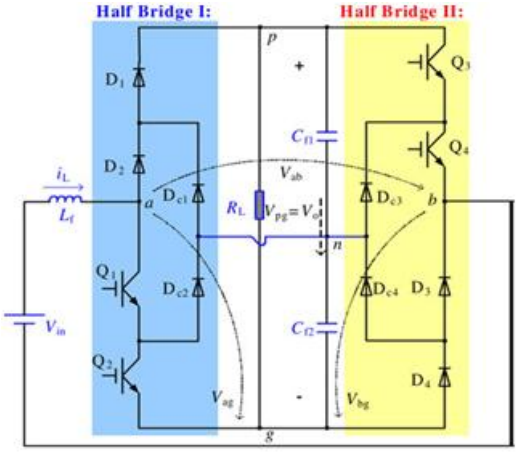

Fig. 4. Proposed hybrid boost three-level dc–dc converter.

TABLE I
CORRESPONDING STATES OF POWER COMPONENTS FOR INSTANTANEOUS OUTPUT PULSE VOLTAGES OF THE HYBRID CONVERTER

V_{ag}	V_{bg}	V_{ab}	Q_1–Q_4	D_1–D_4	L_f	D_{c1}–D_{c4}	C_{f1}	C_{f2}
$V_{Cf1}+V_{Cf2}$	0	V_o	0000	1111	tr.	0000	ch. together	
$V_{Cf1}+V_{Cf2}$	V_{Cf2}	$V_o/2$	0001	1100	tr.	0010	ch.	disch.
V_{Cf1}	0	$V_o/2$	1000	0011	tr.	0100	disch.	ch.
0	0	0	1100	0011	st.	0000	disch. together	
V_{Cf1}	V_{Cf2}	0	1001	0000	st.	0110	disch. together	
$V_{Cf1}+V_{Cf2}$	$V_{Cf1}+V_{Cf2}$	0	0011	1100	st.	0000	disch. together	

*Annotate: the power switch Q_x is "on" when "1" is denoted, otherwise, it is "off" when "0" is denoted, diodes D_x and D_{cx} ($x = 1, 2, 3, 4$) may be deduced by analogy; "ch." and "disch." mean "charged" and "discharged" respectively; "tr." and "st." mean "transferred" and "stored" respectively; Assuming $V_{Cf1} = V_{Cf2} = V_o/2$.

Then, the instantaneous Vab of the hybrid converter is Vo . While Cf 1 is charged by Vin , as well as the energy stored inLf through diodesD2,D1 , and Dc3 when only Q4 is turned ON. At the same time, Cf 2 is discharged for the load, and the instantaneous Vab is Vo /2, which is the voltage across Cf 1 . In addition, the redundant state for the instantaneous Vab = Vo /2 is that Cf 2 is charged by Vin and the energy stored in Lf through diodes Dc2,D4 , and D3 when only Q1 is turned ON. Meanwhile, Cf 1 is discharged for the load, and Vab is the voltage across Cf 2 . When the power switches Q1 and Q2 are turned ON, the energy is stored in Lf through diodes D4 and D3 , while Cf 1 and Cf 2 are discharged together for the load. Then, the instantaneous Vab is zero. Moreover, the other two redundant states for Vab = 0 is that power switch pairs(Q1,Q4), or (Q3,Q4) are turned ON, respectively, the energy is stored in Lf by Vin through the corresponding diodes, while Cf 1 and Cf 2 are discharged together for the load.

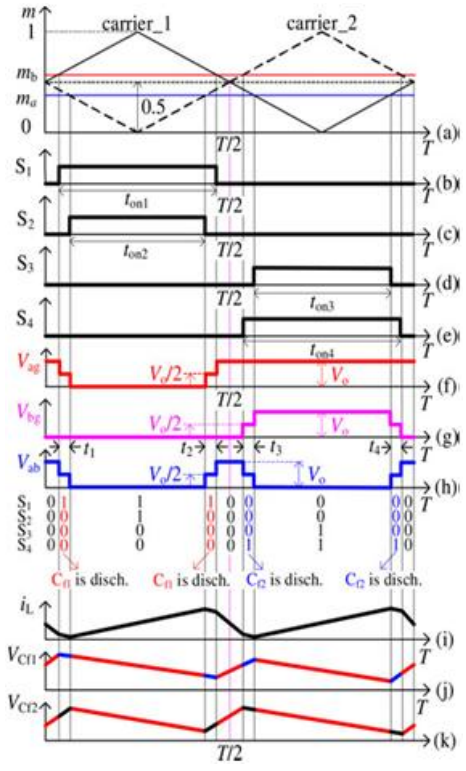

Fig. 5. PWM control method.

B. PWM Control of Topology:

According to Table I, the switching functions of Vag and Vbg for both half-bridges can be described as follows:

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$$V_{ag} = (1-S_1 \cdot S_2) \cdot (V_{Cf1}+V_{Cf2}) - (S_1 - S_2) \cdot V_{Cf1} \quad (2)$$

$$V_{bg} = S_3 \cdot V_{Cf1} + S_4 \cdot V_{Cf2} \quad (3)$$

where Sx (x = 1, 2, 3, 4) = "0" or "1" is the function of the switching state of the corresponding power switch. Accordingto (1)–(3), the switching function of Vab for the hybrid convertercan be written as

$$V_{ab} = [(1 - S_1) \cdot (1 + S_2) - S_3] \cdot V_{Cf1} + (1 - S_1 \cdot S_2 - S_4) \cdot V_{Cf2}. \quad (4)$$

Then, the PWM control method can be depicted in Fig. 5, according to (2)–(4) and the consideration that switching actionsare the least between two adjacent switching states (S1S2S3S4) in one carrier period, as well as the required balancing principlefor charging or discharging of Cf 1 and Cf 2 . In Fig. 5(a), ma and mb are the modulation indexes for thedouble modulation waves, and carrier_1, carrier_2 are designedas π phase-shifted carriers due to the two half-bridges structureof the hybrid converter. In addition, the PWM control law can be described as

$$\begin{cases} m_b > V_{\text{carrier\_1}}, S_1 = 0 \\ m_a > V_{\text{carrier\_2}}, S_2 = 1 \\ m_a > V_{\text{carrier\_1}}, S_3 = 1 \\ m_b > V_{\text{carrier\_2}}, S_4 = 0. \end{cases} \quad (5)$$

As a result, the PWMcontrol signals ofQ1 − Q4 are obtainedin Fig. 5(b) to (e), and then the three-level pulse voltages Vagand Vbg can be achieved according to the operation states ofthe topology, as shown in Fig. 5(f) and (g), as well as Vabshown in Fig. 5(h). When Vab = 0, the energy is stored in Lf , and the inductor current iL increases as shown in Fig. 5(i),otherwise it decreases. According to Table I, there are such threeswitching states in each carrier cycle, namely "0000", "1100"and "0011" that Cf 1 and Cf 2 are charged or discharged together in respective switching state, as shown in Fig. 5(j) and (k). Then, the voltage balancing of Cf 1 and Cf 2 would not be affected bythese three switching states.

However, in the switching states "1000" and "0001,"Cf 1 is discharged during the first half-cycle, while Cf 2 is done in the second half-cycle. If the dischargingtime (t1 + t2) shown in Fig. 5(g) is not equal to (t3 + t4), the voltage balancing of Cf 1 and Cf 2 will be affected seriously. In Fig. 5(b) to (e), ton1 − ton4 are the turn-on time ofQ1 − Q4 respectively, while the carriers are about t = T/4 or t = 3 T/4symmetric in each half-carrier period according to Fig. 5(a), the discharging time of capacitors can be written as

$$\begin{cases} t_1 = t_2 = \dfrac{t_{\text{on1}} - t_{\text{on2}}}{2} \\ t_3 = t_4 = \dfrac{t_{\text{on4}} - t_{\text{on3}}}{2}. \end{cases} \quad (6)$$

In addition, while the carriers are about m = 0.5 symmetric in each carrier cycle, the turn-on time ofQ1 − Q4 can be written as

$$\begin{cases} t_{\text{on1}} = t_{\text{on4}} \\ t_{\text{on2}} = t_{\text{on3}}. \end{cases} \quad (7)$$

Therefore, the discharging time (t1 +t2) ofCf 1 , and (t3 +t4) of Cf 2 can be equal by means of (6) and (7), namely

$$t_1 + t_2 = t_3 + t_4. \quad (8)$$

Fortunately, the load current could be considered constant ineach carrier cycle (T is small enough) [20], and the alternatingdischarging time of Cf 1 and Cf 2 are identical, and then thevoltages across Cf 1 and Cf 2 can be self balanced.

C. Topology Operation With High Voltage Gain

According to the operation states of the hybrid converter, energy Wst is stored in Lf when Vab = 0, otherwise, energy Wtr is transferred. It is assumed that the inductor current iL iscontinuous, and IL is its average current. Then, Wst and Wtr

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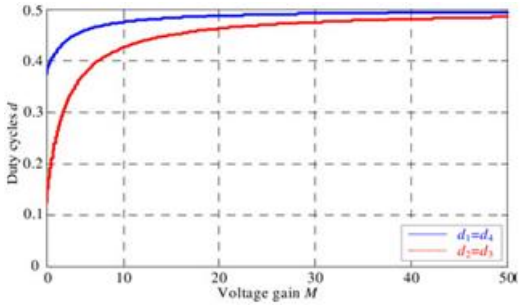

Fig.6. Duty cycles curves versus voltage gain.

Can be described in one carrier period as follows:

$$\begin{cases} W_{st} = V_{in} \cdot I_L \cdot t_{on2} \times 2 \\ W_{tr} = (V_o - V_{in}) \cdot I_L \cdot \left(\frac{T}{2} - t_{on1}\right) \times 2 + \left(\frac{V_o}{2} - V_{in}\right) \\ \qquad \cdot I_L \cdot (t_1 + t_2) \times 2 \\ W_{st} = W_{tr}. \end{cases} \tag{9}$$

As a result, the output dc voltage Vo is obtained from (6) and (9) as follows:

$$V_o = V_{in} \cdot \frac{T}{T - (t_{on1} + t_{on2})} = \frac{V_{in}}{1 - (d_1 + d_2)}. \tag{10}$$

where d1 and d2 are the duty cycles of Q1 and Q2 , respectively. Then, all the duty cycles of power switches can be described asfollows with the modulation indexes ma and mb , by means of(7) and Fig. 5(a)–(e)

$$\begin{cases} d_1 = d_4 = 1 - m_b \\ d_2 = d_3 = m_a. \end{cases} \tag{11}$$

where d3 and d4 are the duty cycles of Q3 and Q4 , respectively. Then, the voltage gain M of the hybrid converter is written as follows by (10) and (11)

$$M = \frac{V_o}{V_{in}} = \frac{1}{1 - (d_1 + d_2)} = \frac{1}{m_b - m_a}. \tag{12}$$

In terms of (12), it can be concluded that the closer mb andma get, the higher the voltage gain is.

Moreover, the extremeduty cycles of the power switches can be avoided, if bothmb andma are around 0.5 with the limited conditions:ma < 0.5< mb ,and mb + ma < 1, by means of (11). As to the given voltagegain M, there is an infinite number of solutions to mb andma . However, a tradeoff between the nonextreme duty cyclesof power switches and the fluctuating amplitude of the inductorcurrent must be well considered, and the better solution in thisletter is described as

$$\begin{cases} m_b = 0.5 + \frac{1}{4M} \\ m_a = 0.5 - \frac{3}{4M}. \end{cases} \tag{13}$$

Combining (11) with (13), the relationship between the dutycycles of the power switches and the voltage gain can be depictedin Fig. 6. It is indicated that the higherM is, the closer to 0.5 dx

TABLE II
EXPERIMENTAL PARAMETERS AND COMPONENTS

Parameters and components	Values (units)
Rated power P_n	1 kW
Input DC voltage V_{in}	50 V
Reference voltage V_{ref}	600 V
Output filtering capacitors C_{f1}=C_{f2}	100 μF
Inductor L_f	317 μH
Switching frequency f_c	11.5 kHz
Load resistor R_L	300~2000 Ω
Power switches Q_1~Q_4	FGA30N60 (600V, 30A)
Diodes D_1~D_4 and D_{c1}~D_{c4}	MUR3060 (600V, 30A)

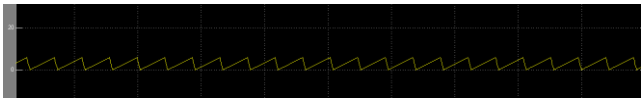

Fig. 7. the inductor current.

(x=1, 2, 3, 4) become. Therefore, the proposed hybrid converteris suitable for the high step-up dc–dc voltage source interface of PV generation systems.

IV.SIMULATION RESULTS:

In order to verify the validity of the proposed topology and the PWM control method, an experimental prototype is set up in our laboratory. The experimental parameters and components are listed in Table II, and

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the PI controller of voltage loop, whichis not discussed in this letter, is adopted to control the output dcvoltage.

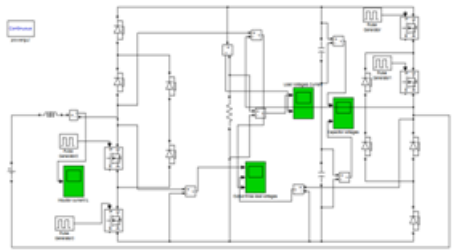

Fig . Simulation Circuit

The blocking voltages acrossQ1,Q2 and the inductor currentin steady state are shown in Fig. 7, when the load resistor RLis 360 Ω. It is shown that the blocking voltages of Q1 and Q2are half of the output dc voltage (600 V), and the duty cyclesd1 and d2 are about 48% and 44% respectively, rather than91.7% (11/12) when the voltage gain is M = 12. In addition,the fluctuating amplitude of iL is about 6.4 A (iL is measuredby Current Sensor-CSM050AP). The output three-level voltages Vag and Vbg of both halfbridgesare shown in Fig. 8, and the output three-level voltageVab (narrow pulse voltage) of the hybrid converter is obtainedby the difference between Vag and Vbg .In order to verify the converter's performance for the stepchange of the load, the voltages across C1, C2 and the load, aswell as the inductor current, are shown in Fig. 9 with the load resistor step change from 720 to 360 Ω. The capacitor voltagesVCf1 and VCf2 , both are stabilized at 300 V before the load stepchange, and Vo is naturally controlled at 600 V stably. WhileiL fluctuates from 7.9 to 14.5 A. After the load step change,both capacitor voltages are stabilized at 300 V again with the

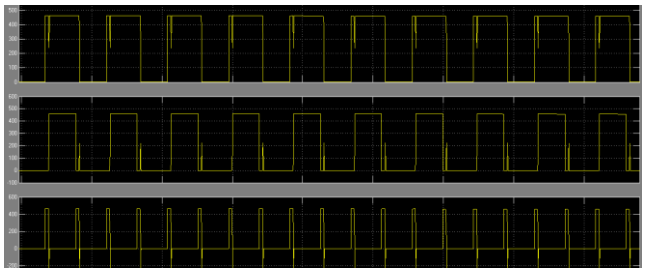

Fig. 8. Output three-level voltages of the converter.

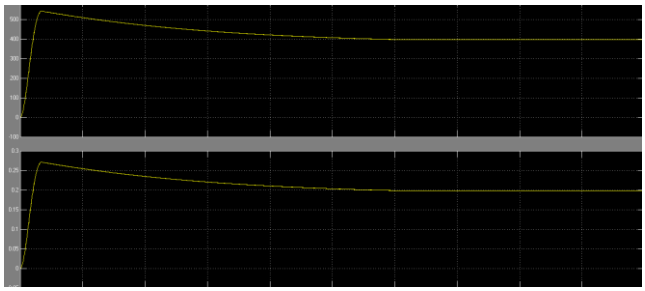

Fig. 9. Output dc voltages and inductor current under the load step change from 720 Ω to 360 Ω.

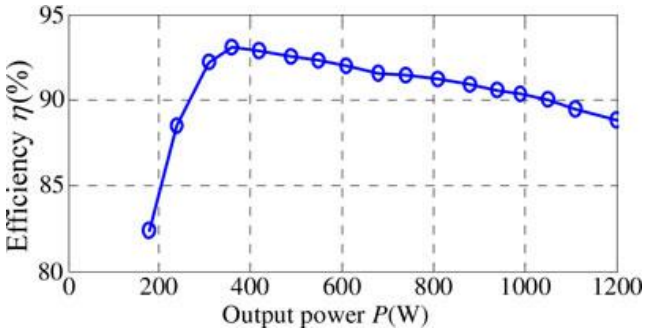

Fig. 10. Measured efficiency of the proposed converter.

Adjustment time about 16 ms, namely, the capacitor voltages canbe balanced, though it is under load step change condition. Inaddition, the inductor current increases and adjusts, and then itfluctuates from 20 to 26.4 A in the steady state. The measured efficiency of the proposed converter is depictedin Fig. 10. When the output power is 180 W, the efficiencyis about 82%, and the maximum efficiency is about 93.1% at360 W. However, it decreases to 90.3% at full load.

V.CONCLUSION:

The hybrid boost three-level dc–dc converter is proposed in this letter, based on the conventional single-phase diode clamped three-level inverter. It cannot only operate with transformer less high voltage gain, but also make the duty cycles of the power switches closer to 0.5 with the increasing voltage gain, instead of the extreme duty cycles. Moreover, the capacitor voltages can be balanced both in dynamic and steady states by the proposed PWM control method and the blocking voltages of the power switches are half of the output dc voltage.

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The measured maximum efficiency of the hybrid converter is about 93.1%. Therefore, the proposed converter is suitable for PV generation systems connected to the grid with parallel-connected low-voltage PV arrays. Naturally, the MPPT of PV arrays will be studied further based on this hybrid converter in the future.

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ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

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