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An Improved Design of Vedic Multiplier Using Reversible Logic

Cheripally Nireshkumar
Master in Technology (VLSI),
Department of ECE,
Jawaharlal Nehru Institute of Technology,
Ibrahimpatnam.

N.Ravi Kumar
Assistant Professor,
Department of ECE,
Jawaharlal Nehru Institute of Technology,
Ibrahimpatnam.

V.Teju
Associate Professor & HoD,
Department of ECE,
Jawaharlal Nehru Institute of Technology,
Ibrahimpatnam.

Abstract:
Multiplier configuration is dependably a testing errand; what number of ever novel outlines are proposed, the client needs requests a great deal more streamlined ones. Vedic arithmetic is widely acclaimed for its calculations that yield faster results, be it for mental estimations or equipment outline. Power scattering is radically lessened by the utilization of Reversible rationale. The reversible UrdhvaTiryakbhayam Vedic multiplier is one such multiplier which is successful both regarding velocity and force. In this paper we plan to upgrade the execution of the past configuration. The Total Reversible Logic Implementation Cost (TRLIC) is utilized as a guide to assess the proposed outline. This multiplier can be proficiently received in planning Fast Fourier Transforms (FFTs) Filters and different utilizations of DSP like imaging, programming characterized radios, remote correspondences.

Keywords: ***Quantum Computing, Reversible Logic Gate, UrdhvaTiryakbhayam, Optimized Design, TRLIC.***

INTRODUCTION

Vedic Mathematics is a standout amongst the most antiquated approachs utilized by the Aryans as a part of request to perform scientific estimations [2]. This comprises of calculations that can come down expansive number-crunching operations to straightforward personality estimations. The above said advantage originates from the way that Vedic science methodology is entirely unexpected and considered near the way a human personality works. The endeavors put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to acquaint Vedic Mathematics with the average citizens and additionally streamline Vedic Algorithms into 16 classifications [1] or Sutras should be recognized and acknowledged. The UrdhvaTiryakbhayam is one such augmentation calculation which is outstanding for its proficiency in decreasing the computations included.

With the headway in the VLSI innovation, there is a perpetually expanding extinguish for versatile and implanted Digital Signal Processing (DSP) frameworks. DSP is inescapable in verging on each building discipline. Quicker augmentations and increases are the request of the day. Increase is the most fundamental and habitually utilized operations as a part of a CPU. Augmentation is an operation of scaling one number by another. Duplication operations additionally frame the premise for other complex operations, for example, convolution, Discrete Fourier Transform, Fast Fourier Transforms, and so on. With everincreasing requirement for quicker clock recurrence it gets to be basic to have speedier math unit. In this way, DSP designers are constantlylooking for new calculations and equipment to execute them. Vedic science can be apropos utilized here to perform duplication.

Another imperative zone which any DSP engineer needs to think is the force scattering, the first being velocity. There is dependably a tradeoff between the force scattered and speed of operation. The reversible calculation is one such field that guarantees zero force dissemination. In this way amid the outline of any reversible circuit the postponement is the main criteria

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that must be dealt with. In [12] a reversible UrdhvaTiryakbhayam Multiplier had been proposed. This paper is an augmentation of the past work which tries to improve the circuit proposed in [12]. The paper is composed as takes after: The segment II gives the nuts and bolts of reversible rationale alongside the writing survey.

Area III clarifies the UrdhvaTiryakbhayam calculation. The segment IV portrays the adjustments of the past configuration with a specific end goal to advance the enhanced outline. Area V contrasts the proposed plan and the other non Vedic multipliers and additionally the past Vedic multiplier outline and make an inference asserting the adaptability of Reversible UrdhvaTiryakbhayam multiplier.

REVERSIBLE LOGIC

Literature Survey and Significance of reversible logic

Traditional combinational rationale circuits are known not warm for all of data that is lost. This is likewise clear from the second law of thermodynamics which expresses that any irreversible procedure prompts loss of vitality.

Landauer [3] demonstrated that any door that is irreversible, fundamentally disseminates vitality, and each irreversible piece produces k*T ln2 joules of warmth where k is Boltzmann's consistent (1.38 x 10-23 joules/Kelvin) and T is temperature in Kelvin. Bringing down the edge voltage and administration of the force supply are generally connected practices to diminish the vitality utilization in any coherent operation [23]. However these advancements of bringing down the vitality utilization will hit a hindrance of kT [24]. So as to ease this, systems, for example, lessening the temperature of PC and developing a thermodynamically reversible PC can be utilized [25].

Straightforward [25] investigated that the second alternative was a superior decision. At the point when the temperature of the framework diminishes to supreme zero, the vitality lessens two requests of greatness however utilizing reversible figuring there can be further more decrease thatmatches with the hypothetical worth.

The cardinal element of reversible figuring is that electric charge on the capacity cell comprising of transistors is not allowed to stream away amid transistor exchanging [26]. This can be reused through reversible registering and subsequently diminish vitality dissemination. Bennett in 1973 [2] demonstrated that an irreversible PC can simply be made reversible. Reversible rationale circuits normally deal with warming subsequent to in a reversible rationale each information vector can be remarkably recuperated from its yield vectors and consequently no data is lost.

Reversible Logic Gates

A Reversible Logic door is a n-information n-yield rationale capacity in which there is a coordinated correspondence between the inputs and the yields. This not just decides the yields from the inputs additionally the inputs can be remarkably recuperated from the yields. On account of this bijective mapping the yield vectors are only changes of the information vectors.

A portion of the essential reversible rationale doors in the writing those are valuable in outlining the Reversible UrdhvaTiryakbhayam Multiplier are the Feynman [5] Gate—the main 2x2 entryway, that is utilized for fan-out purposes and additionally to complement. It has a quantum expense of one. Peres [6] Gate—a 3x3 entryway that is utilized to deliver AND operation and EX-OR operation.

It has a quantum expense of four. New Fault Tolerant entryway (NFT) – is additionally a 3x3 door with a quantum cost five. HNG door which is a 4x4 entryway that can be viably utilized as a full snake and gives least quantum cost usage. It has a quantum expense of six. BVPPG [11] is a 5x5 door with a quantum expense of ten. All the said doors are appeared in the figure 1.

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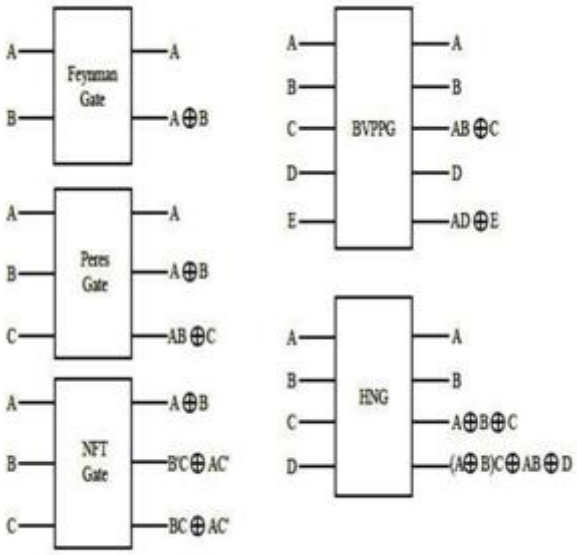

FIGURE 1: REVERSIBLE LOGIC GATES

Optimization parameters for reversible logic circuits

The vital parameters [14] which assume a noteworthy part in the configuration of an advanced reversible rationale circuit are as recorded:

- Constants (CI): This alludes to the quantity of inputs that are to be kept up consistent at either 0 or 1 keeping in mind the end goal to orchestrate the given intelligent capacity.
- Garbage (GO): This alludes to the quantity of yields which are not utilized as a part of the amalgamation of a given capacity. These are exceptionally key, without which reversibility can't be accomplished.
- Gate count (NG): The quantity of reversible entryways used to understand the capacity.
- Flexibility: This alludes to the all inclusiveness of a reversible rationale entryway in acknowledging more capacities.
- Quantum cost (QC): This alludes to the expense of the circuit as far as the expense of a primitive entryway. It is figured knowing the quantity of primitive reversible rationale entryways (1x1 or 2x2) required to understand the circuit.
- Gate levels: This alludes to the quantity of levels in the circuit which are required to understand the given rationale capacities.
- Total Reversible Rationale Implementation Cost (TRLIC) [12]: Let, in a reversible rationale circuit □

URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

UrdhvaTiryakbhayam (UT) is a multiplier in light of Vedic scientific calculations deviced by old Indian Vedic mathematicians. UrdhvaTiryakbhayam sutra can be connected to all instances of increases viz. Paired, Hex furthermore Decimals. It depends on the idea that era of every single fractional item should be possible and after that simultaneous expansion of these halfway items is performed. The parallelism in era of incomplete items and their summation is acquired utilizing UrdhvaTiryakbhayam. Not at all like different multipliers with the expansion in the quantity of bits of multiplicand and/or multiplier does the time delay in calculation of the item not increment proportionately. In light of this reality the season of calculation is autonomous of clock recurrence of the processor. Henceforth one can restrict the clock recurrence to a lower esteem. Likewise, since processors utilizing lower clock recurrence disseminate lower vitality, it is conservative regarding power component to utilize low recurrence processors utilizing quick calculations like the previously mentioned. The Multiplier in view of this sutra has the preferred standpoint that as the quantity of bits increases, door postponement and region increments at a moderate pace when contrasted with other traditional multipliers.

The Algorithm: Multiplication of 101 by 110.

1. We will take the right-hand digits and duplicate them together. This will give us LSB digit of the answer.
2. Duplicate LSB digit of the top number by the second piece of the base number and the LSB of the base number by the second piece of the top number. When we have those qualities, include them together.

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3. Increase the LSB digit of base number with the MSB digit of the main one, LSB digit of top number with the MSB digit of base and after that duplicates the second piece of both, and afterward includes every one of them together.
4. This progression is like the second step, simply move one spot to one side. We will increase the second digit of one number by the MSB of the other number.
5. At long last, basically increase the LSB of both numbers together to get the last item.

OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The traditional rationale outline usage of a 2x2 UrdhvaTiryakbhayam multiplier utilizing the irreversible rationale doors [8] is an appeared in the Figure 3. In [12] the four expressions for the yield bits are gotten from this figure and is utilized to get the reversible execution as appeared in Figure 4. The circuit utilizes five Peres entryways and one Feynman door. This configuration has an aggregate quantum expense of 21, number of rubbish yields as 11 and number of steady inputs 4. The entryway number is 6. This outline does not think about the fan outs. The general execution of the UT multiplier is scaled up by streamlining every individual unit as far as quantum cost, junk yields and so on.

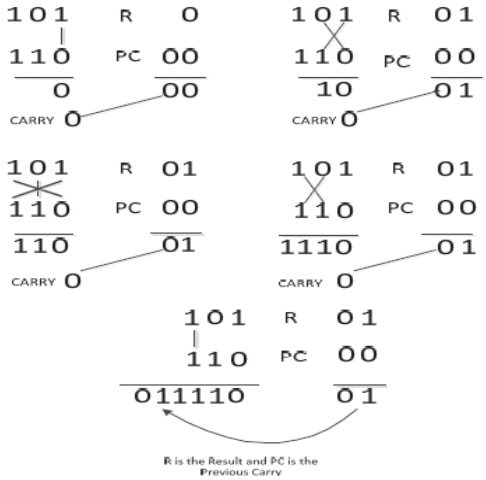

FIGURE 2: URDHVA TIRYAKBHAYAM PROCEDURE FOR MULTIPLICATION

Improved 2x2 UrdhvaTiryakbhayam multiplier

The outline expressions can be coherently adjusted in order to advance the configuration. The new plan makes utilization of one BVPPG, three Peres entryways and a solitary Feynman door. The configuration likewise checks the fan outs. One of the real outline limitations of reversible rationale is the fan out, other being circles not allowed. This implies the reversible rationale circuit with numerous quantities of same inputs is not fitting. One way out is to utilize a different fan out generator or to construct a circuit that innately deals with fan outs utilizing the reversible rationale entryways utilized as a part of the outline. This outline has a quantum expense of 23, number of waste yields as 5, number of entryways 5 and the quantity of steady inputs is 5.

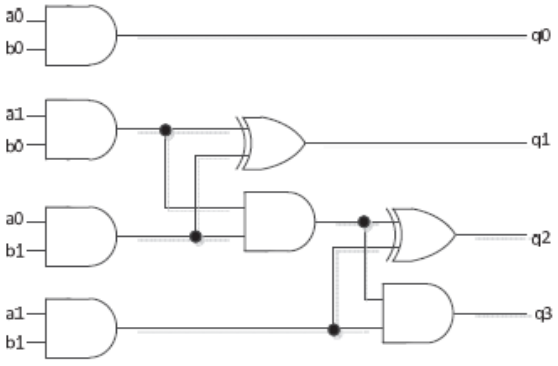

FIGURE 3: CONVENTIONAL 2X2 URDHVA TIRYAKBHAYAM MULTIPLIER

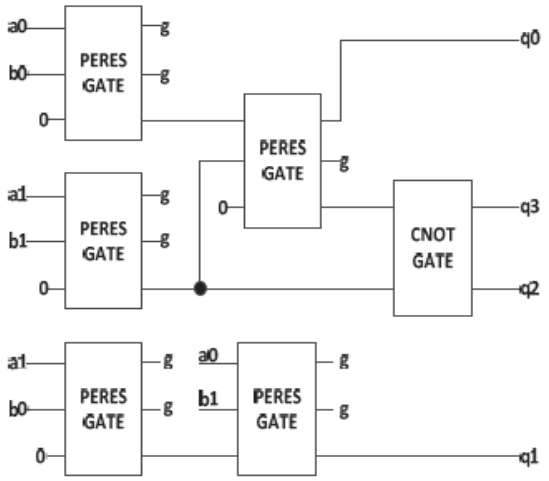

FIGURE 4: REVERSIBLE 2X2 UT MULTIPLIER IN

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The second outline additionally considers the fan out utilizing BVPPG, three Peres doors and one NFT entryway as appeared in the figure 5. The quantum expense of the circuit is 24; number of waste yields as 4, number of doors 5 and the quantity of consistent inputs is 5. I1, I2, I3 (Fig 5 and 6) and I4 (Fig 6) are the middle of the road yields that are utilized for fan-out purposes.

Design of 4x4 UrdhvaTiryakbhayam multiplier

The Reversible 4X4 UrdhvaTiryakbhayam Multiplier outline exudes from the 2X2 multiplier. The square chart of the 4X4 Vedic Multiplier is displayed in the figure 6. It comprises of four 2X2 multipliers each of which obtains four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the yield of the initial 2X2 multiplier are ensnared as the most minimal two bits of the last aftereffect of duplication. Two zeros are linked with the upper two bits and given as contribution to the four piece swell convey snake. The other four information bits for the swell convey snake are acquired from the second 2X2 multiplier. Moreover the yields of the third and the terminal 2X2 multipliers are given as inputs to the second four piece swell convey viper. The yields of these four piece swell convey adders are thus 5 bits every which should be summed up. This is finished by a five piece swell convey viper.

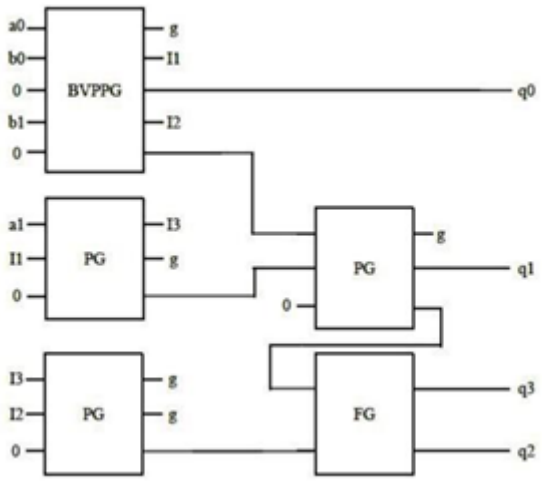

FIGURE 5: PROPOSED MODIFIED DESIGN 1

Which produces a six piece yield? These six bits frame the upper bits of the last result.

Modification in the design of ripple carry adder

The configuration appeared in [12] comprises of just HNG doors. The quantity of HNG doors is 4 if the swell convey snake is utilized as a part of the second stage or five if the swell convey viper is utilized as a part of the last phase of the 4X4 UrdhvaTiryakbhayam Multiplier. the swell convey snake can be adjusted as under. Since for any swell convey snake the information convey for the primary full viper is zero, this certainly implies the principal snake is a half viper. In this way a Peres entryway can effectively supplant a HNG. This chop down the quantum cost by two for any swell convey viper and the trash yield by one. The Constant inputs and the door check stay unaltered.

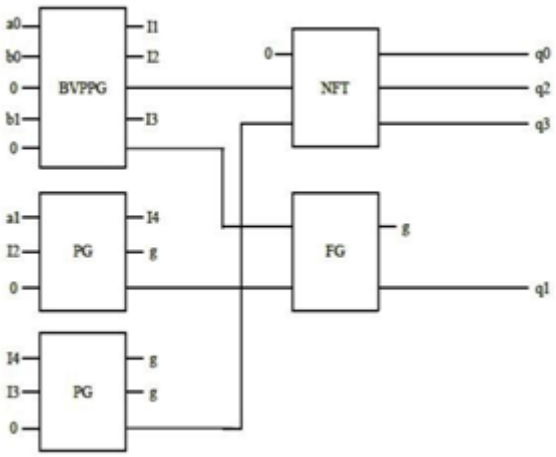

FIGURE 6: PROPOSED MODIFIED DESIGN 2

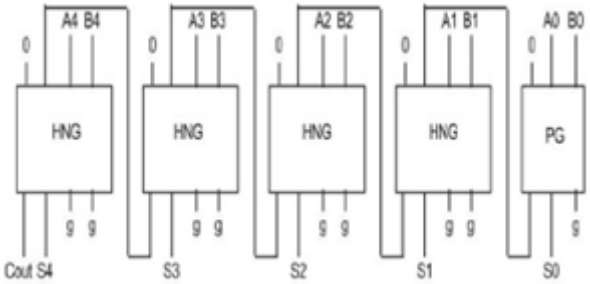

FIGURE 7: PROPOSED MODIFIED 5 BIT RIPPLE CARRY ADDER DESIGN

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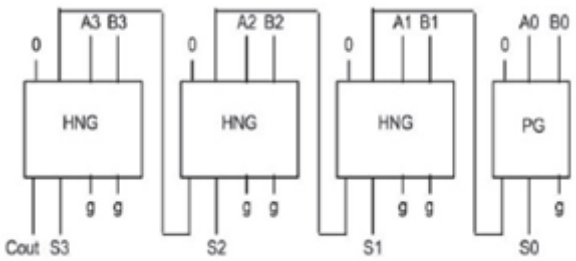

FIGURE 8: PROPOSED MODIFIED 4 BIT RIPPLE CARRY ADDER DESIGN

The 4x4 UT multiplier structure is as shown in figure 9.

RESULTS AND COMPARISONS

The outline of the reversible 2x2 and 4x4 multipliers is sensibly confirmed utilizing XILINX 9.2i and MODELSIM. The recreation results are as appeared in figures 10 and 11 separately. The accompanying are the imperative outline requirements for any reversible rationale circuits.

1. Reversible rationale circuits ought to have least quantum cost.
2. The outline can be streamlined in order to deliver least number of junk yields.
3. The reversible rationale circuits must utilize least number of steady inputs.
4. The reversible rationale circuits must utilize a base number of reversible gates.

Since TRLIC is the aggregate of all these design parameters, it is praiseworthy to have a minimum estimation of TRL IC. The proposed configuration of Reversible UT Multiplier is contrasted and upwards of 11 distinctive unmistakable multiplier outlines s in the writing regarding Quantum cost, junk yields, number of doors, number of consistent inputs furthermore as far as TRLIC qualities. This additionally incorporates an examination with our own past outline and the advancement is plainly clear from the table of Comparison as appeared in table 1.

The proposed configuration of 4x4 UT multiplier as of now said deals with the fan-outs too. In spite of the fact that there is a slight increment in the quantum expense of the 2x2 UT multiplier (it is 23 in proposed outline 1 and 24 in proposed plan 2) when contrasted with past [12] outline (where it was 21), there is a significant diminishing in the quantity of waste yields (from 9 to 5 and 4 separately in plans 1 and 2) and the door number qualities (from 6 to 5 in both the outlines). Likewise there is a lessening in the quantum expense of all the swell convey adders by 2 because of the basic adjustment including substitution of first HNG door by a Peres Gate and diminishment in trash yield by one because of the same reason. Along these lines, regardless of the fact that the quantum cost has expanded somewhat, the decline in the rubbish yields and entryway check have completely invalidated its impact. The base change in the TRLIC is at 5.86% which is as for [12] and the greatest change stand high at 33.6% worst [22]. Also from the table unmistakably both proposed plans have a base entryway consider well as least rubbish yields when contrasted with every other multiplier contemplated here. The quantity of consistent inputs is superior to anything 10 of the 11 outlines. Along these lines we c a say that the configuration is especially improved when contrasted with others examined here.

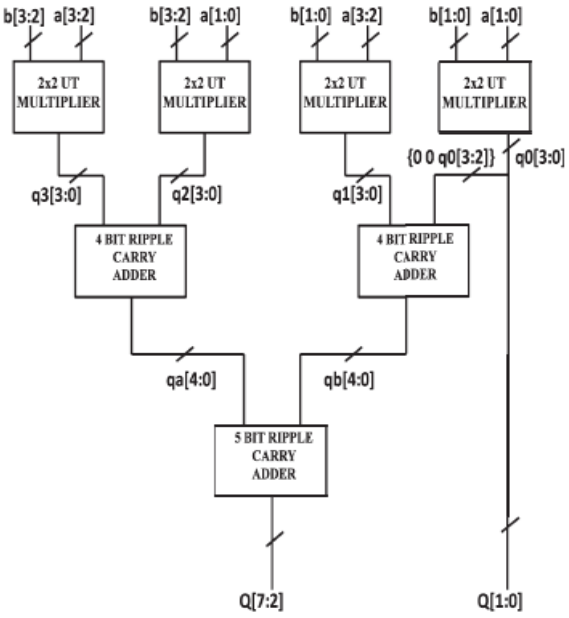

FIGURE 9: BLOCK DIAGRAM OF 4X4 UT MULTIPLIER

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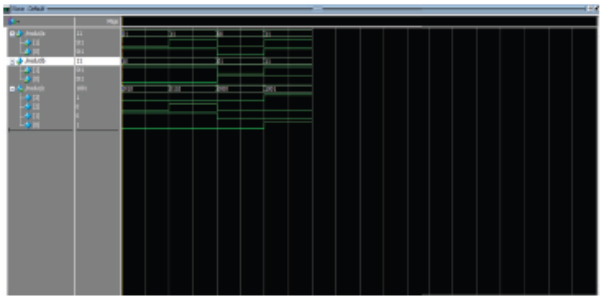

FIGURE 10: SIMULATION RESULTS FOR 2X2 UT MULTIPLIER

FIGURE 11: SIMULATION RESULTS FOR 4X4 UT MULTIPLIER

TABLE 1: COMPARISON OF THE PROPOSED MULTIPLIER DESIGNS

Multiplier Designs	No. of Gates	Constant Inputs	Garbage Outputs	Quantum Cost	TRLIC	Percentage Improvement
Proposed 1	33	33	43	164	273	--
Proposed 2	33	33	39	168	273	--
[12]	37	29	62	162	290	5.86%
[13]	40	52	52	152	296	7.77%
[14]	52	52	52	152	308	11.4%
[15]	52	52	52	152	308	11.4%
[16]	52	52	52	152	308	11.4%
[17]	52	52	52	168	324	15.8%
[18]	52	56	56	208	372	26.6%
[19]	44	56	64	236	400	31.8%
[20]	53	58	58	234	403	32.3%
[21]	48	52	64	244	408	33.1%
[22]	64	55	56	236	411	33.6%

CONC LUSIONS

The center of this paper is for the most part to plan a low power rapid multiplier which is finished by developing the multiplier utilizing reversible rationale entryways. T he technique is completed to yield an enhanced outline when contrasted with those in the writing. The effectiveness of a reversible rationale circuit is described as far as parameters, for example, quantum cost, number of steady inputs, trash yields and number of entryways used to understand the rationale execution. Bring down the estimation of these parameters more effective is the outline. In [12] parameter called TRLIC had been proposed which is characterized as total of all cost measurements of the given configuration. The quantum expense is a parameter that critical ctly mirrors the deferral of the quantum circuit. Likewise lower TRLIC certainly implies bring down the quantum cost, subsequently low er is the deferral and the other way around. Other than soaking up the outline paradigm that fan-out must be created inside the circuit, th e proposed plans additionally decrease the TRLIC when contrasted with the beforehand proposed outline [12]. The further advancement of the circuit as far as the aggregate sensible expenses is under advancement and is taken as future work.

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REFERENCES

1. Swami BharatiKrsnaTirtha, Vedic Mathematics. Delhi: MotilalBanarsidass publishers 1965Vedic Mathematics: http://www.hinduism.co.za/vedic.html.

2. R. Landauer,"Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.

3. C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.

4. R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.

5. A. Peres, Reversible logic and quantum computers, Phys. Rev. A(1985) 3266–3276.

6. E. Fredkin and T. Toffoli,"Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982.

7. G Ganesh Kumarand V Charishma, Design of high speed vedic multiplier using vedic mathematics

techniques, Itn'l J. of Scientific and Research Publications, Vol. 2 Issue 3 March 2012

8. RakshithSaligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" VLSICS, Vol No (6), Dec-12

9. RakshithSaligram and Rakshith T.R. "Novel Code Converter Employing Reversible Logic", International Journal of Computer Applications (IJCA), August 2012.

10. H R Bhagyalakshmi and M K Venkatesha," Optimized multiplier using Reversible Multi-Control Input Toffoli Gates", VLSICS, Vol No (6), Dec.- 12

11. Rakshith T R and RakshithSaligram, Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach, Intl. Conf. on Circuit, Power and Computational Technologies.

12. H. R. Bhagyalakshmi, M. K. Venkatesha, "An Improved Design of a Multiplier using Reversible Logic Gates," IJEST, Vol. 2, No. 8, 2010.

13. FatemeNaderpour, Abbas Vafaei "Reversible Multipliers: Decreasing the Depth of the Circuit" ICECE 2008, 20-22 December 2008.

14. Maryam Ehsanpour , PaymanMoallem, Abbas Vafaei, "Design of a Novel Reversible multiplier Circuit Using Modified Full Adder", 2010 International Conference On Computer Design And Applications, 1389, (ICCDA 2010)

15. M. Haghparast, S. JafaraliJassbi, K. Navi and O. Hashemipour, "Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology", World Applied Science J.lVol. 3 No. 6, 2008.

16. M.S. Islam et al., "Low cost quantum realization of reversible multiplier circuit", Information technology journal, Vol.8, 2009

17. M. Shams, M. Haghparast and K. Navi, "Novel Reversible Multiplier Circuit in nanotechnology", World Applied Science Journal Vol. 3, No. 5, pp. 806-810, 2008.

18. NidhiSyal, Dr. H.P. Sinha, "Design of fault tolerant reversible multiplier", International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-6, January 2012.

19. H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 2006

20. SomayehBabazadeh and MajidHaghparast, "Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit", Journal of Basic and Applied Scientific Research.

21. Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005, A Reversible Version of 4×4 Bit Array Multiplier with Minimum Gates and Garbage Outputs, Int. Conf. Embedded System, Applications (ESA'05), Las Vegas, USA, pp: 106 114.

22. A. Khazamipur K. Radecka, "Adiabatic Implementation of Reversible Logic", Proc. Midwest Intl. Symposium on Circuits and Systems, pp. 291--294, 2005.

23. M. Nielsen, I. Chuang. Quantum computation and quantum information. Cambridge, UK: Cambridge University Press, 2000.

24. http://www.zettaflops.org/PES/5-Reversible-Frank.pdf

25. Michael P. Frank, "Reversible Computing," invited article, Developer 2.0 magazine, Jasubhai Digital Media, January 2004.

26. Md. Saiful Islam et.al" Synthesis of fault tolerant Reversible logic"IEEE 2009.