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Analysis, Design of Soft-Switching Current-Fed Push-Pull Dc/Dc Converter for Hybrid Vehicles

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Abstract:

The proposed converter has the following features: 1) zero current compensation (ZCC) and common voltage cinching (NVC) dispose of the requirement for dynamic clasp circuits or aloof snubbers required to ingest surge voltage in ordinary current-encouraged topologies; 2) Switching misfortunes are diminished altogether attributable to zero-current exchanging (ZCS) of essential side gadgets and zero-voltage exchanging (ZVS) of auxiliary side gadgets. Turn-on exchanging move loss of essential gadgets is additionally immaterial. 3) Soft-exchanging and NVC are inborn and load free. 4) The voltage crosswise over essential side gadget is free of obligation cycle with changing information voltage and yield control and clasped at rather low reflected yield voltage empowering the utilization of low voltage semiconductor gadgets. These benefits make the converter great possibility for interfacing low voltage dc transport with high voltage dc transport for higher current applications. Relentless state, examination, configuration, reenactment and trial results are displayed.

Index Terms:

Current-fed converter, DC/DC converter, Natural clamping, Soft-switching, Zero-current commutation.

I. Introduction:

Transportation charge has gotten noteworthy enthusiasm inferable from constrained supply of fossil powers and worry of worldwide environmental change [1-2].

Battery based Electric vehicles (EVs) and Fuel Cell Vehicles (FCVs) are developing as feasible answers for transportation zap with lower outflow, better vehicle execution and higher mileage. Contrasted and immaculate battery based EVs, FCVs are entirely engaging with the benefits of zero-outflow, fulfilled driving reach, short refueling time, high effectiveness, and high unwavering quality. An outline of a run of the mill FCV impetus framework is appeared in Fig.1 [3-5]. Bidirectional and unidirectional dc/dc converters are utilized to develop high voltage bus for the inverter. The energy storage system (ESS) is used to overcome the limitations of lacking energy storage capability and fastpower transient of FCVs.

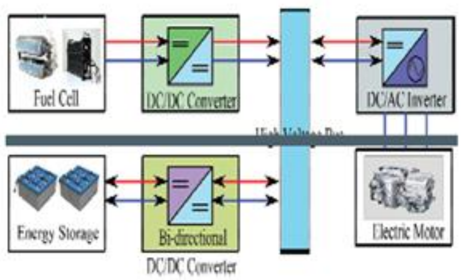

Fig. 1.Diagram of a FCV propulsion system.

Bidirectional converter with high support proportion and high productivity is required to interface the low voltage ESS and high voltage dc join transport. Contrasted and non-secluded topologies, high recurrence (HF) transformer disengaged converters are favored with benefits of high stride up proportion, galvanic seclusion and adaptability of framework setup [6].

HF transformer confined converters could be either voltage-encouraged [7-9] or current-sustained [10-20]. Points of interest and drawbacks of both sorts are thought about in [21-23]. The voltage-sustained converters have low switch voltage evaluations empowering the utilization of switches with low on-state resistance. This can essentially lessen conduction loss of essential side switches. Be that as it may, voltage-bolstered converters experience the ill effects of a few restrictions, i.e. high throbbing current at information, restricted delicate exchanging range, rectifier diode ringing, obligation cycle misfortune (if inductive yield channel), high circling current through gadgets and magnetics, and generally low proficiency for high voltage intensification and high information current applications.

Contrasted and voltage-nourished converters, current-bolstered converters exhibit littler information current swell, lower diode voltage rating, lower transformer turns-proportion, unimportant diode ringing, no obligation cycle misfortune, and simpler current control capacity. In addition, current-nourished converters can definitely control the charging and releasing current of ESS, which helps accomplishing higher charging/releasing productivity. In this manner current-bolstered converter is more possible for the use of ESS in FCVs. Three topologies of segregated current-nourished dc/dc converters, i.e. full-connect [10-12], L-sort half extension [13-15], and push-pull [16-17] have been examined. One downside of current-sustained converters is the high turn - off voltage spike over the gadgets.

Typically, dynamic - clip circuits [14-16, 24-25], RCD latent snubbers [11] or vitality recuperation snubbers [6] are utilized to assimilate the surge voltage and help delicate exchanging. In RCD snubbers, vitality consumed by the bracing capacitor is disseminated in the resistor bringing about low proficiency. Dynamic clip experiences high current anxiety (top) and higher circling current at light load. The spillage inductance and parasitic capacitance of the HF transformer were used to accomplish zero current exchanging (ZCS) in [17-19]. In any case, thunderous current is much higher than information current that builds the present anxiety of gadgets and magnetics requiring higher VA rating segments. Moreover, the variable recurrence regulation makes the control execution troublesome and complex [20]. Outer assistant circuits are used to accomplish ZCS and decrease the circling current in [26-28] yet intricate. Despite the fact that the caught energy can be reused, the assistant circuits still add to a lot of misfortune. In current-sustained bidirectional converter, dynamic delicate compensation method [11, 29-30] is proposed to redirect the change current to another change through transformer to accomplish common or zero current recompense accordingly decreasing or dispensing with the need of snubbers.

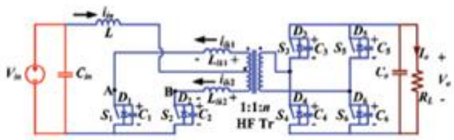

Fig.2. Proposed ZCS current-fed push-pull dc/dc converter.

In this paper, a novel auxiliary tweak based actually braced delicate exchanging bidirectional snubberless current-encouraged push-pull converter is proposed as appeared in Fig. 2. Normal voltage clipping (NVC) with ZCS of essential gadgets is accomplished by proposed auxiliary adjustment and along these lines stays away from the need of aloof snubbers or dynamic clasp making it snubberless. Exchanging misfortunes are diminished fundamentally attributable to ZCS of essential switches and ZVS of optional switches that licenses HF exchanging operation with littler magnetics. The goals of this paper are to clarify relentless state operation and investigation, represent plan, and exhibit test execution of the proposed converter. The targets are acknowledged and sketched out in different Sections as takes after: Steady-state operation of the converter is clarified and its scientific examination is accounted for in Section II. Nitty gritty converter outline methodology is shown in Section III.

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Investigation and configuration are confirmed by reenactment comes about utilizing PSIM 9.0.4 as a part of Section IV. Exploratory results on a research facility model of 250W are exhibited to approve and demonstrate the converter execution in Section IV.

II.OPERATION AND ANALYSIS OF THE CONVERTER

For effortlessness, the accompanying suppositions are made to concentrate on the operation and clarify the investigation of the converter: a) Boost inductor L is sufficiently huge to keep up consistent current through it. b) All the segments are perfect. c) Series inductors Llk1 and Llk2 incorporate the spillage inductances of the transformer. The aggregate estimation of Llk1 and Llk2 is spoken to as Llk_T.Llkrepresents the comparable arrangement inductor reflected tothe high voltage side. d) Magnetizing inductance of the transformer is infinitely large.

A. Boost mode (Discharging Mode) Operation:

In this part, consistent state operation and investigation with zero current substitution (ZCC) and NVC idea has been clarified. Before killing one of essential side switches (say S1), the other switch (say S 2) is turned-on. Reflected output voltage 2Vo/n shows up over the transformer essential. It occupies the current from one switch to the next one through transformer creating current through just activated switch to rise and the current through directing switch to tumble to zero normally bringing about ZCC. Later the body diode crosswise over switch begin directing and its gating sign is expelled prompting ZCSturn-off of the gadget. Commutated gadget capacitance begins accusing of NVC. The enduring state working waveforms of support mode are appeared in Fig. 3. The essential switches S1 and S2 are worked with indistinguishable gating signals stage - moved with each other by 180o with a cover. The cover differs with obligation cycle, and the obligation cycle ought to be kept above half. The consistent state operation of the converter amid various interims in a one half HF cycle is clarified utilizing the identical circuits appeared as a part of Fig. 4.

For the rest half cycle, the interims are rehashed in the same succession with other symmetrical gadgets leading to finish the full HF cycle.

Interval 1 (Fig. 4a; $t_o<t<t_1$):

In this interim, essential sideswitches S2 and against parallel body diodes D3 and D6 of optional side H-span switches are leading. Force is exchanged to the heap through HF transformer. The non-leading optional gadgets S4 and S5 are blocking yield voltage Vo and the non-directing essential gadgets S1 is blocking reflected yield voltage 2Vo/n. The estimations of current through different parts are: iS1 =0, iS2 =Iin, ilk1=0, ilk2= Iin, iD3 = iD6= Iin/n.Voltage over the switch S1: VS1 = 2Vo/n. Voltage over the switches S4 and S5: VS4 =VS5 = Vo.

Interval 2 (Fig. 4b; $t_1<t<t_2$):

Att=t_1, primary switchS_1isturned-on. The corresponding snubber capacitor C_1 discharges in a very short period of time.

Interval 3 (Fig. 4c; $t_2<t<t_3$):

Every one of the two essential switches are conducting. Reflected yield voltages show up crosswise over inductors Llk1and L lk2, occupying/exchanging the current through switch S2to S1. It causes current through already directing gadget S2to decrease straightly. It likewise brings about conduction of switch S1with zero current which helps lessening related turn-on misfortune. The streams through different segments are given by

$$i_{lk1}\; i_{S1} \quad \frac{2\,V_o}{n\,L_{lk\_T}}(t \quad t_2) \qquad (1)$$

$$i_{lk2}\; i_{S2} \quad I_{in} \quad \frac{2\,V_o}{n\,L_{lk\_T}}(t \quad t_2) \qquad (2)$$

$$i_{D3} \quad i_{D6} \quad \frac{I_i\,n}{n} \quad \frac{4\,V_o}{n^2\,L_{lk\_T}}(t \quad t_2) \qquad (3)$$

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Where $L_{lk\_T} = L_{lk1} + L_{lk2}$. Toward the end of this interim t=t3, the counter parallel body diode D3 and D6 are directing. In this manner S3and S6 can be gated on for ZVS turn-on. Toward the end of this interim, D3 and D6 commutates actually. Current through every single essential gadget achieves Iin/2. Last values are:
$i_{lk1} = i_{lk2} = I_{in}/2$, $i_{S1} = i_{S2} = I_{in}/2$, $i_{D3} = i_{D6} = 0$.

Interval 4 (Fig. 4d; $t_3 < t < t_4$): In this interim, secondary H-span gadgets S3 and S6 are turned-on with ZVS. Streams through all the exchanging gadgets keep expanding or diminishing with the same incline as interim 3. Toward the end of this interim, the essential gadget S2 commutates normally with ZCC and the particular current iS2 achieves zero getting ZCS. The full present, i.e. information current is assumed control by other gadget S1. Final values are: $i_{lk1} = i_{S1} = I_{in}$, $i_{lk2} = i_{S2} = 0$, $i_{S3} = i_{S6} = I_{in}/n$ .Interval 5 (Fig. 4e; $t_4 < t < t_5$): In this interval, the leakage inductance current ilk1 increments further with the same slant and hostile to parallel body diode D2 begins directing making extended zero voltage show up crosswise over commutated switch S2 to guarantee ZCS turn-off. Presently, the auxiliary gadgets S3 and S6 are killed. Toward the end of this interim, current through switch S1 achieves its pinnacle esteem. This interim ought to be short to restrict the pinnacle current however the transformer and switch lessening the present anxiety and kVA evaluations.

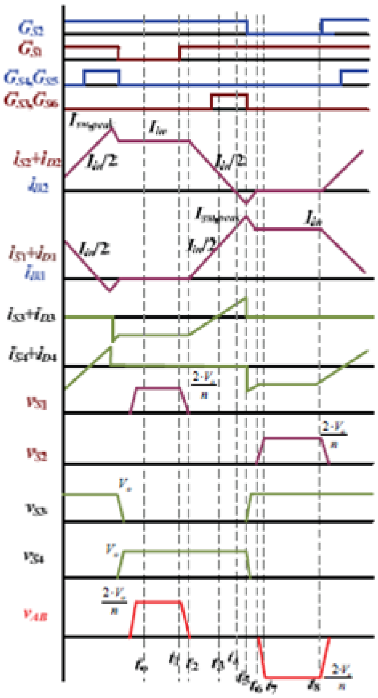
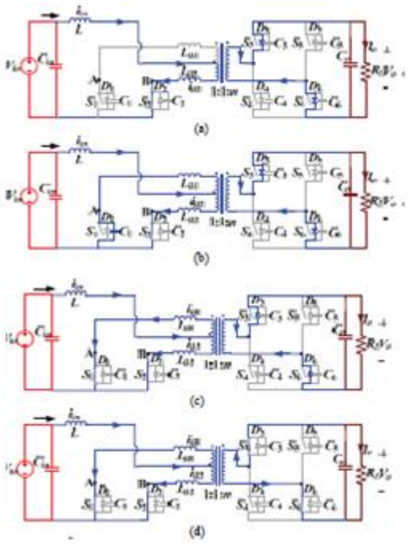


Fig. 3. Operating waveforms of proposed ZCS current-fed push-pull converter in the boost mode.



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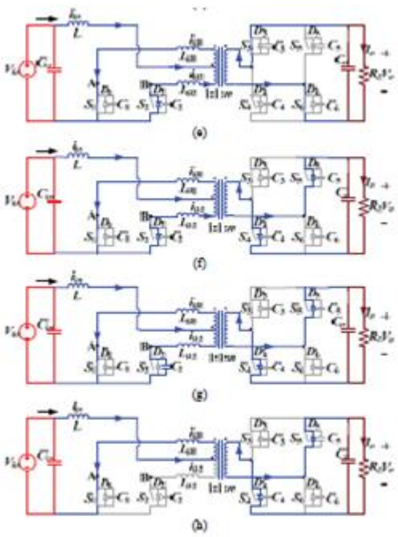

Fig. 4. Equivalent circuits during different intervals of the boost mode operation.

Interval 6 (Fig. 4f; $t_5<t<t_6$):

During this interval, secondary switches S_3 and S_6 are turned-off. Anti-parallel body diodes of switches S_4 and S_5 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch S_1 and body diodes D_2 also start decreasing. At the end of this interval, current through D_2 reduce to zero and is commutated naturally. Current through S_1 reaches I_{in}. Final values: $i_{lk1}= i_{S1}=I_{in}$, $i_{lk2}= i_{D2}=0$, $i_{D4}= i_{D5}= I_{in}/n$.

Interval 7 (Fig. 4g; $t_6<t<t_7$):

In this interval, snubber capacitorC_2 charges to $2V_o/n$ in a short period of time. Switch $S_2$is in forward blocking mode now.

Interval 8 (Fig. 4h; $t_7<t<t_8$):

In this interval, currents through$S_1$and transformer are constant at input currentI_{in}. Currentthrough anti-parallel body diodes of the secondary switches D_4 andD_5 is at I_{in}/n. The final values are: $i_{lk1}=i_{S1}=I_{in}$, $i_{lk2}=i_{S2}=0$, $i_{D4}= i_{D5}= I_{in}/n$. Voltage across the switch $S_2 V_{S2} = 2V_o/n$. In this half HF cycle, current has transferred from switch S_2 to S_1, and the transformer current has reversed its polarity.

B. Buck mode (Charging Mode) Operation:

In the reverse direction, the converter acts as a standard voltage-sustained full-connect focus tapped converter with inductive yield channel. The regenerative braking vitality can be nourished back and revive the low voltage stockpiling from high voltage transport, along these lines expanding general framework productivity. Standard stage - shift PWM control method is utilized to accomplish ZVS of high voltage side and ZCS of low voltage side. At low voltage side, gadgets need not be controlled on the grounds that body diodes of the gadgets can assume control as high-recurrence rectifier. The enduring state working waveforms of buck mode are appeared in Fig. 5. The optional side slanting switch sets S3-S6 and S4-S5 worked with indistinguishable gating signals stage moved with each other by 180o with a very much characterized dead time crevice. The unfaltering state operation of the converter amid various interims in a one half HF cycle is clarified utilizing the equal circuits appeared as a part of Fig. 6.

Interval 1 (Fig. 6a; $t_o<t<t_1$):

In this interval, secondary side switch pair S_3-S_6 and body diode D_2 of primary side switch are conducting. Power is transferred to the battery from high voltage dc-link bus through HF transformer. The values of current through various components are: $i_{D1}=0$, $i_{D2}=i_{battery}$,$i_{S3}= i_{S6}=i_{lk}=i_{battery}/n$. Voltage across the diode D_1: $V_{D1}= 2V_o/n$.Voltage across the switches S_4 and S_5: $V_{S4} =V_{S5} = V_o$.

Interval 2 (Fig. 6b; $t_1<t<t_2$):

Att=t_1, secondary side switchpair S_3- S_6 is turned-off. i_{lk} charge the snubber capacitor C_3 and $C_6$and discharges the snubber capacitor $C_4$and C_5in a shortperiod of time. Simultaneously, the capacitor C_1 discharges very fast. At the end of this interval t=t_2, the body diode D_4 and $D_5$are conducting. As long as the H-bridge devices $S_4$and $S_5$are turned on before i_{lk} changes its direction, ZVS turn-on canbe assured. Final values are: $i_{D4}= i_{D5}=i_{lk}=i_{battery}/n$, $i_{D1}=0$, $i_{D2}=i_{battery}$, $V_{D1}= 0$; $V_{S4}=V_{S5}= 0$, $V_{S3}=V_{S6}=V_o$;

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Interval 3 (Fig. 6c; $t_2<t<t_3$):

Now output voltage appearsacross inductors L_{lk}, causing current to reduce linearly. The currents through various components are given by

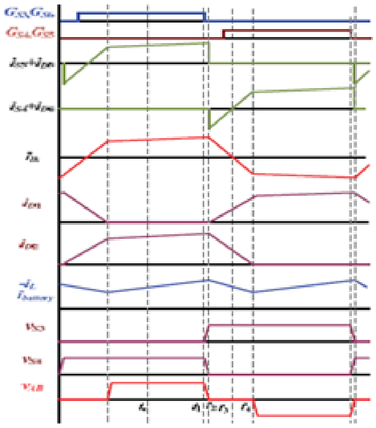

Fig. 5. Operating waveforms of proposed ZCS current-fed push-pull converter in the buck mode

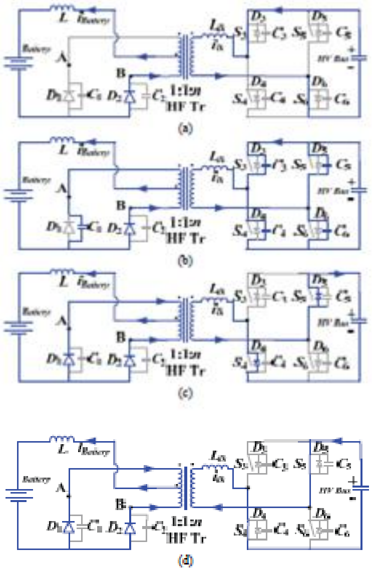

Fig. 6.Equivalent circuits during different intervals of the buck modeoperation.

Final values are: iD4 = iD5=ilk= 0, iD1= iD2 =ibattery/2.

Interval 4 (Fig. 6d; t3 <t <t4):

In this interval, S4 and S5 are turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3.

At the end of this interval, current flowing throughbody diode D2 decreases to zero obtaining ZCS. Final values are: ilk=-ibattery/n, iD1 = ibattery, iD2 =0.

III DESIGN OF THE CONVERTER:

In this Section, converter outline system is shown by a design case for the accompanying particulars: info voltage Vin= 12 V, yield voltage Vo = 150 to 300V, yield power Po =250W, exchanging recurrence fs= 100 kHz. The configuration equations are introduced to decide the segments' appraisals. It helps selection of the parts and in addition to anticipate the converter performance hypothetically. where is the obligation cycle of essential switches. This condition is derived on the condition that hostile to parallel diode conducti on time (e.g. interim 6) is entirely short and insignificant with the intention to guarantee ZCS of essential switches without significantly expanding the pinnacle current. In any case, at light load condition of converter, (power module stack is supplying the greater part of the power to drive framework and battery is supplying only auxiliary load), and the counter parallel diode conduction time is comparatively huge, (14) is not substantial any more.

Because of the existence of longer against parallel diode conduction period, the output voltage is helped to higher worth than that of nominal boost converter In this way, most extreme estimation of n = 12.5 for Vo, min=150V. Fig. 7(a) demonstrates variety of aggregate estimation of arrangement inductances Llk_T(H) as for force exchanging capacity P (W) for four estimations of turns-proportion. With the expansion of turns-proportion, the estimation of Llk_T abatements. It is hard to acknowledge low spillage inductance with high turns-proportion. Also, higher turns-proportion may prompt more transformer misfortune on account of higher copper misfortune, higher vortex current from vicinity impact and higher center misfortune because of bigger size. In any case, expanding the turns-proportion can decrease the most extreme voltage over the essential switches, which licenses utilization of low voltage gadgets with low

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on-state resistance (as appeared by Fig. 7(b). Hence conduction misfortunes in the essential side semiconductor gadgets can be fundamentally decreased. An ideal turns-proportion n =10, obligation proportion d = 0.8 are chosen to accomplish a worthy exchange off. Yield voltage can be controlled from 150 V to 300 V by balancing the obligation proportion from 0.6 to 0.8 including battery voltage variety because of its charging and releasing characteristics.(6) Leakage inductance Llk_T = 8.18 µH for the given qualities from (17). Here, arrangement inductors Llk1 and Llk2 are decided to beequal to half of Llk_T: Llk1= Llk2=4.09 µH. Estimation of support inductor is given by

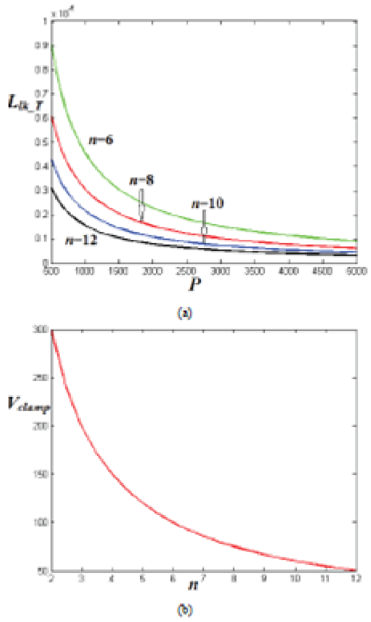

Fig. 7.Variation of (a) Total value of series inductances L_{lk_T} (H) with respect to power transferring ability P (W), and (b) Clamped voltage across primary switches V_{clamp} for various transformer turns-ratio n.

cycled=0.85 for dynamic cinched ZVS and 0.8 for proposed ZCS topology. It is clear from Table I that that pinnacle current anxiety through transformer and optional side switches of proposed ZCS converter is impressively lower. All the more critically, dynamic clipped current-bolstered ZVS topology has decreased support limit contrasted with proposed topology by 20% (not keeping up property of genuine help converter). What's more, the voltage over the essential switches of proposed topology is braced at lower voltage than dynamic clipped topology that diminished their conduction misfortunes inferable from low on-state resistance of low voltage gadgets. The proficiency of the proposed converter is higher because of lessened misfortunes connected with clasp circuit and fundamental essential switches.

IV.SIMULATION AND EXPERIMENTAL RESULTS:

Proposed converter has been mimicked utilizing programming PSIM 9.0.4. Reenactment comes about for information voltage Vin = 12 V, yield voltage Vo = 300 V, yield power Po = 250W, gadget exchanging recurrence fs = 100 kHz are shown in Fig. 8. Reproduction comes about agree intimately with hypothetically anticipated waveforms. It checks the unfaltering state operation and investigation of the converter displayed in Section II. Waveforms of current through the info inductor L and voltage VAB are appeared in Fig. 8 (a). The swell recurrence of info inductor current iL is 2x fs bringing about a lessening in size. Voltage waveform VAB demonstrates that voltage over the essential switches is actually clasped at low voltage i.e. 2Vo/n .Fig. 8(b) indicates current waveforms through essential switches S1 and S2 and auxiliary switches S3 and S4 including the streams moving through their particular body diodes, stage moved with each other by 180o (S1vsS2, S5vsS6). Essential switch streams (I(S1), I(S2)) are redirected from one switch (say S 1) to the next one (S2)causing one switch to ascend to Iin and the other one to tumble to zero. This unmistakably shows guaranteed ZCC of essential switches. The negative essential streams relate to conduction of body diodes before the switches are killed, which guarantees ZCS turn-off of the essential switches. As appeared in current waveforms of S3 and S4 in Fig. 8, the counter parallel diodes of changes behavior preceding the conduction of relating switches, which checks ZVS of the auxiliary side switches.

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Test model of the proposed push-pull converter, as appeared in Fig. 9, is worked for the details and outline given in Section III. Points of interest of the exploratory converter are given in Table II. Since the aggregate estimation of spillage inductance of HF transformer is lower than the coveted quality given in Section III, two outside little size arrangement inductors have been included, which can be stayed away from in functional modern converter if transformer is composed appropriately. Likewise, slight deviation in this quality ought not influence the execution excessively. Entryway signs are produced utilizing Xilinx Spartan-6 FPGA outline stage.

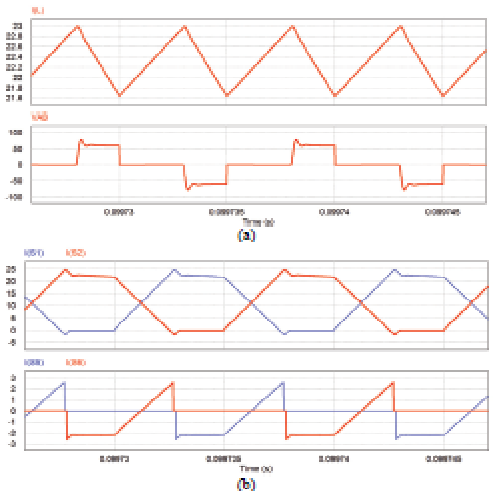
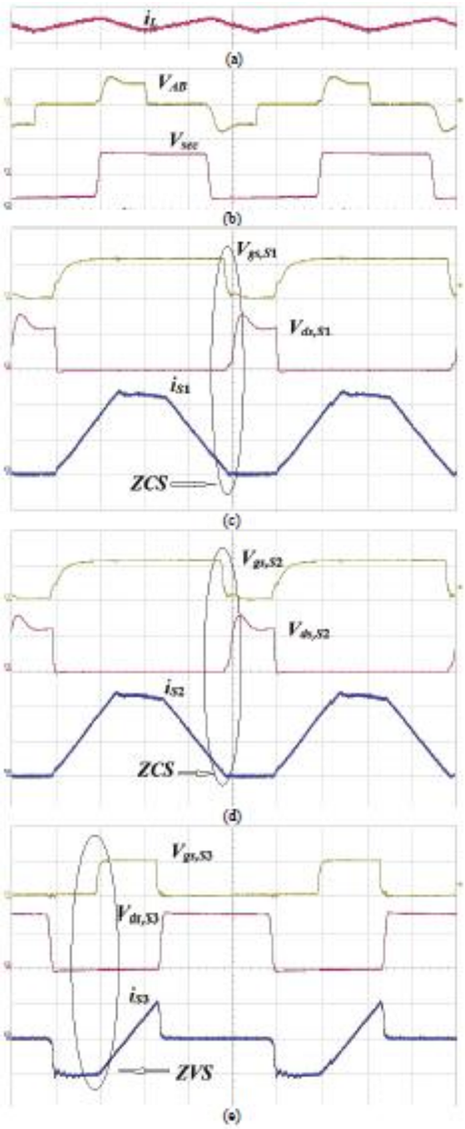


Fig. 8. Simulation results for output power of 250W at 300V. (a) Current through input inductor i_L and voltage V_{AB}. (b) Primary switches currents i_{S1} and $i_{S2}$and secondary switches currents$i_{S3}$and i_{S4}.

Fig.9. Photograph of the laboratory prototype.

TABLE: II.MAJOR COMPONENTS' PARAMETERS OF EXPERIMENTAL PROTOTYPE.

Components	Parameters
Primary switches $S_1 \sim S_2$	IRFB4110GPBF 100V, 180A. $R_{ds,on}$ = 3.7 mΩ
Secondary switches $S_3 \sim S_4$	IPP60R125CP 650V, 11A. $R_{ds,on}$ = 0.125Ω
HF transformer	3C95ETD49 ferrite core; Primary turns N_1=7, Secondary turns N_2=70 Leakage inductances reflected to primary, 264nH and 375nH respectively
External series inductors	TDK5901PC40Z core, 3.5μH and 3.4μH
Input boost inductor L	3C95ETD49 ferrite core, turns N = 12 L=22.5 μH
Input capacitors C_{in}	4.7 mF, 50V electrolytic 2.2μF high-frequency film capacitor
Output capacitors C_o	220uF, 450V electrolytic capacitor 0.68uF, 450V high frequency film capacitor



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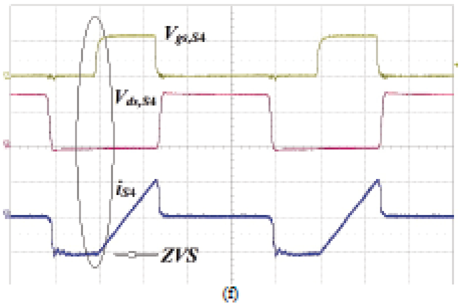
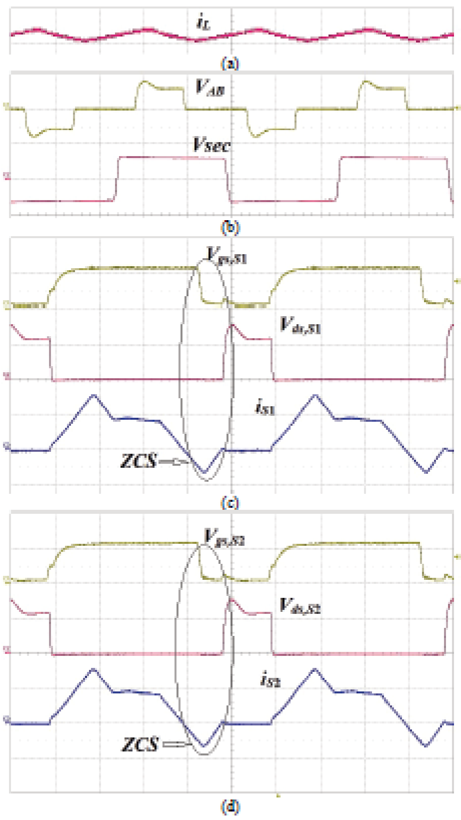


Fig. 10. Experimental results for output power of 250W at 300V(x-axis: 2μs/div): (a) Boost inductor current i_L (5A/div), (b) Voltage v_{AB} (100V/div) and voltage across secondary of transformer v_{sec} (500 V/div), (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (50V/div) across the primary side MOSFETs and currents through them (10A/div). (e-f) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across the secondary side MOSFETs and currents through them (2A/div)



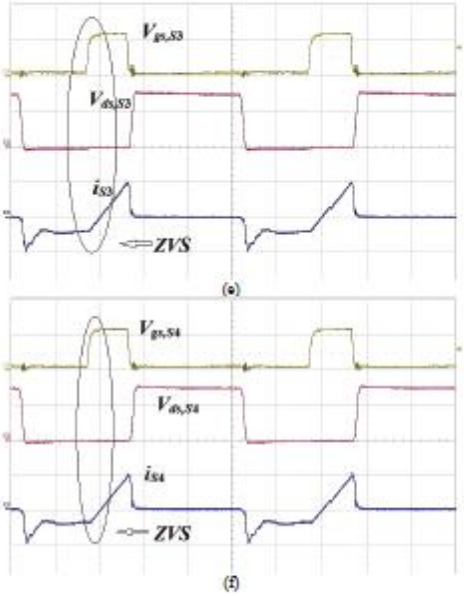


Fig. 11. Experimental results for output power of 100W at 300V(x-axis:2μs/div): (a) Boost inductor current i_L (5A/div), (b) Voltage v_{AB} (100V/div) and voltage across secondary of transformer v_{sec} (500 V/div), (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (50V/div) across the primary side MOSFETs and currents through them (10A/div). (e-f) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across the secondary side MOSFETs and currents through them (2A/div).

Trial comes about for yield force of 250W and 100W at 300V are appeared in Fig.10 and Fig. 11 respectably. Parts (c) and (d) of Figs. 10-11 show door to-source Vgsand channel to-source Vdsvoltage waveforms over the essential gadgets, and the gadget current waveform. This obviously affirms the ZCS of essential gadgets. Current through the change normally goes to zero and hostile to parallel body diode begins leading before expulsion of entryway sign. It can be plainly seen from the waveforms that door voltage Vgsfalls to zero and from there on, the switch voltage Vdsstarts rising. The augmented zero voltage over the gadget is brought about by hostile to parallel body diode conduction as is clear from switch current waveform. Parts (e) and (f) of Figs. 10-11 clearly demonstrate the ZVS turn-on of the auxiliary switches.

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Gating signs to auxiliary switches Vgs,S3 (Top switch S3) Vgs,S4 (Bottom switch S4) are connected when voltage crosswise over them Vds,S3 and Vds,S4, separately is zero as of now. Furthermore, its body diode conducts before switch conduction affirming ZVS of auxiliary gadgets. Likewise, the turn-on strategy of essential switches is additionally exhibited in waveforms appeared in Figs. 10 (c)- (d) and Fig. 11(c)- (d). Before turning on, the voltage crosswise over essential switch is braced at 2Vo/n=60V. At the point when the switch is gated on, the current through it is ascending at a consistent slant from zero.With this constrained di/dtthrough essential switch and low cinched voltage crosswise over it, the turn-on exchanging move misfortune (because of cover of switch voltage and current amid exchanging move time) can be viewed as immaterial. Considering ZCS turn-off of the primary switches and ZVS turn- on of the secondary side switches mentioned above, the total switching losses are reduced enormously.

Voltages across the primary winding of the HF transformer $V_{AB}$are illustrated in parts (b) of Figs. 10-11. Thehigh-frequency bipolar voltage waveform clearly states the clamped devices' voltage (less than 100V). Low on-state resistance can be used due to the naturally low clamped voltage across them resulting in lower conduction loss and higher efficiency. Parts (a) of Figs. 12-13 show the boost inductor current waveforms with 2x device switching frequency, which brings a reduction of size of the inductor. Fig. 12 demonstrates measured effectiveness for various burden for the proposed outline and the created research facility model. The pinnacle effectiveness of 93.6% for 200W and full load productivity 92.9% for 250W are gotten in forward bearing. Misfortune conveyance estimation from the misfortune model given in [31] is Fig. 13. It is anything but difficult to find that conduction misfortunes of essential gadgets are somewhat low due to the utilization of low voltage gadgets. Exchanging loss of both sides of HF transformer are decreased fundamentally because of delicate exchanging.

A significant piece of aggregate misfortune is from support inductor and HF transformer. The rate of this a player in misfortune can be lessened with the expansion of influence level and streamlined outline.

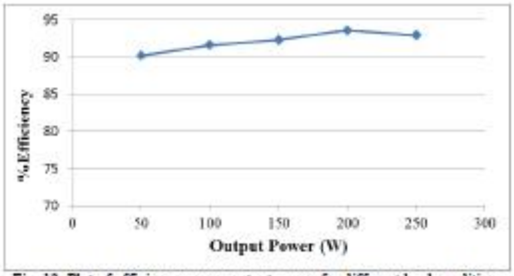

Fig. 12. Plot of efficiency versus output power for different load condition.

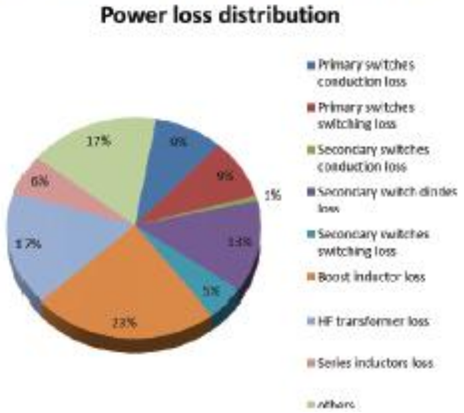

Fig. 13.Loss comparison of proposed converter at full load condition.

V.SUMMARY AND CONCLUSIONS:

This paper introduces a novel delicate exchanging snubberless bidirectional current-sustained detached push-pull dc/dc converter for utilization of the ESS in FCVs. A novel optional side balance strategy is proposed to wipe out the issue of voltage spike over the semiconductor gadgets at turn-off. The above asserted ZCC and NVC of essential gadgets with no snubber are shown and affirmed by the reenactment and trial comes about. ZCS of essential side gadgets and ZVS of optional side gadgets are accomplished, which lessens the exchanging misfortunes altogether. Delicate exchanging is innate and is kept up autonomous of burden. Once ZCC, NVC, and delicate changing are intended to be acquired at evaluated power, it is ensured to happen at diminished burden dissimilar to voltage-bolstered converters.

Turn-on exchanging move loss of essential gadgets is likewise appeared to be immaterial. Thus keeping up delicate exchanging of all gadgets considerably diminishes the exchanging misfortune and permits higher exchanging recurrence operation for the converter to accomplish a more conservative and higher influence thickness framework. Proposed auxiliary tweak accomplishes regular replacement of essential gadgets and clasps the voltage crosswise over them at low voltage (reflected yield voltage) autonomous of obligation cycle. It along these lines dispenses with prerequisite of dynamic cinch or aloof snubber. Use of low voltage gadgets brings about low conduction misfortunes in essential gadgets, which is huge because of higher streams on essential side. The proposed regulation strategy is straightforward and simple to execute.

These benefits make the converter promising for interfacing low voltage dc transport with high voltage dc transport for higher current applications, for example, FCVs, front-end dc/dc power transformation for renewable (power devices/PV) inverters, UPS, microgrid, V2G, and vitality stockpiling. The details are taken for FCV however the proposed regulation, outline, and the showed results are reasonable for any broad use of current-bolstered converter (high stride up). Comparative benefits and execution will be accomplished.

VI.REFERENCES:

[1]A. Khaligh and Z. Li, “Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art”, IEEE Trans. on Vehicular Technology, vol. 59, no. 6, pp. 2806- 2814, Oct. 2009.

[2]A. Emadi, and S. S. Williamson, “Fuel cell vehicles: opportunities and challenges,” in Proc. IEEE PES, 2004, pp. 1640-1645.

[3]K. Rajashekhara, “Power conversion and control strategies for fuel cell vehicles,” in Proc. IEEE IECON, 2003, pp. 2865-2870.

[4]A. Emadi, S. S. Williamson, and A. Khaligh, “Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems,” IEEE Trans. Power Electron., vol. 21, no. 3, pp. 567–577, May. 2006.

[5]A. Emadi, K. Rajashekara, S. S. Williamson, and S. M. Lukic, “Topological overview of hybrid electric and fuel cell vehicular power system architectures and configurations” IEEE Trans. on Vehicular Technology, vol. 54, no. 3, pp. 763–770, May. 2005.

[6]T.-F. Wu, Y.-C. Chen, J.-G. Yang, and C.-L. Kuo, “Isolated bidirectional full-bridge DC–DC converter with a flybacksnubber,” IEEE Trans.Power Electron., vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[7]Y. Kim; I. Lee; I.Cho; G. Moon, “Hybrid dual full-bridge DC–DC converter with reduced circulating current, output filter, and conduction loss of rectifier stage for RF power generator application," IEEE Trans.Power Electron., vol.29, no.3, pp.1069-1081, March 2014

[8]Corradini, L.,Seltzer, D., Bloomquist, D., Zane, R., Maksimović, D., Jacobson, B., "Minimum Current Operation of Bidirectional Dual-Bridge

[9]Series Resonant DC/DC Converters", IEEE Trans. Power Electron.,vol. 27, no.7, pp.3266-3276, July 2012.

[10]X. Li and A. K. S. Bhat, “Analysis and design of high-frequency isolated dual-bridge series resonant DC/DC converter,” IEEE Trans. PowerElectron., vol. 25, no. 4, pp. 850–862, Apr. 2010

[11]R.-J. Wai, C.-Y. Lin, and Y.-R. Chang, “High step-up bidirectional isolated converter with two input power sources,” IEEE Trans. Ind.Electron., vol. 56, no. 7, pp. 2629–2643, Jul. 2009.

[12]Lizhi Zhu, "A Novel Soft-Commutating Isolated Boost Full-bridge ZVS-PWM DC-DC Converter for Bi-directional High Power Applications," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 422–429, Mar. 2006.

[13]P. Xuewei and A. K. Rathore, "Novel Interleaved Bidirectional Snubberless Soft-switching Current-fed Full-bridge Voltage Doubler for Fuel Cell Vehicles," IEEE Transactions on Power Electronics, vol. 28, no. 12, Dec. 2013, pp. 5355-5546.

[14]A. K. Rathore and U. R. Prasanna, "Analysis, Design, and Experimental Results of Novel Snubberless Bidirectional Naturally Clamped ZCS/ZVS Current-fed Half-bridge Dc/Dc Converter for Fuel Cell Vehicles," IEEETrans. Ind. Electron., no.99, Aug. 2012.

[15]S. J. Jang, C. Y. Won, B. K. Lee and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," IEEETrans. on Energy Conversion, vol. 22, no.2, pp. 332-340, June 2007.

[16]S. Han, H. Yoon, G. Moon, M. Youn, Y. Kim, and K. Lee, "A new active clamping zero-voltage switching PWM current-fed half bridge converter," IEEE Trans. Power Electron., vol.20, no.6, pp 1271-1279, Nov.2006.

[17]Tsai-Fu Wu, Jin-Chyuan Hung, Jeng-Tsuen Tsai, Cheng-Tao Tsai, and Yaow-Ming Chen, "An active-clamp push-pull converter for battery sourcing application," IEEE Trans. Industry Application., vol.44, no.1, pp.196-204, Jan.2008.

[18]C.L. Chu and C.H. Li, "Analysis and design of a current-fed zero-voltage-switching and zero-current-switching CL-resonant push-pull dc-dc converter," IET Power Electron., vol. 2, no. 4, pp. 456–465, Jul. 2009.

[19]R. Y. Chen, R. L. Lin, T. J. Liang, J. F. Chen, and K. C. Tseng, "Current-fed full-bridge boost converter with zero current switching for high voltage applications," Fourtieth IAS Annual Meeting. ConferenceRecord of the 2005 Industry Applications Conference, 2005, pp.2000-2006.

[20]Stanislaw Jalbrzykowski and TadeuszCitko, "Current-Fed Resonant Full-Bridge Boost DC/AC/DC Converter," IEEE Trans. Ind. Electron., vol. 55, no.3 ,pp.1198-1205, March 2008.

[21]Tsorng-Juu Liang; Ren-Yi Chen; Jiann-Fuh Chen; Wei-Jin Tzeng; , "Buck-type current-fed push-pull converter with ZCS for high voltage applications," TENCON 2007 - 2007 IEEE Region 10 Conference, Oct. 30 2007-Nov. 2 2007, pp.1-4.

[22]F. Krismer, J. Biela, and J.W. Kolar, "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," Fourtieth IAS Annual Meeting in Industry ApplicationsConference, 2005, pp.599-606.

[23]M. Mohr and F.-W. Fuchs, "Voltage fed and current fed full bridge converter for the use in three phase grid connected fuel cell systems," in

[24]Proc. IEEE Int. Power Electron. Motion Control Conf., 2006, pp. 1–7.

[25]Akshay K Rathore and Prasanna UR, "Comparison of soft-switching voltage-fed and current-fed bi-directional isolated Dc/Dc converters for fuel cell vehicles," in Proc. IEEE ISIE, May 2012, pp. 252-257.

[26]Kunrong Wang, Fred C. Lee, and Jason Lai, "Operation Principles of Bi-directional Full-bridge DC/DC Converter with Unified Soft switching Scheme and Soft-starting Capability," in Proc. IEEE APEC, 2000. pp.111-118.

[27]G. Chen. Y. Lee, S. Hui. D. Xu, and Y. Wang, "Actively clamped bi-directional flyback convener," IEEE Trans Ind. Electron., vol. 47, no. 4, pp. 770-779, Aug. 2000

[28]Ahmad Mousavi, Pritam Das, and Gerry Moschopoulos, " A comparative study of a new ZCS DC–DC full-bridge boost converter with a ZVS active-clamp converter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1347–1358, Mar. 2012.

[29]A. Averberg, K. R. Meyer, and A. Mertens, "Current-fed full bridge converter for fuel cell systems," in Proc. IEEE Power Electron. Spec.Conf. (PESC), 2008, pp. 866–872.

[30]T. Reimann, S. Szeponik, G. Berger, and J. Petzoldt, "A novel control principle of bidirectional dc–dc power conversion," in Proc. IEEEPESC'97 Conf., 1997, pp. 978–984.

[31]Udupi R. Prasanna, Akshay K. Rathore, and Sudip K. Mazumder, "Novel Zero-Current-Switching Current-Fed Half-Bridge Isolated DC/DC Converter for Fuel-Cell-Based Applications," IEEE Trans. Industry Application., vol.49, no.4, pp.1658-1668, July, 2013

[32]Z.Wang and H. Li, "A soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wside input voltage range," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 669–684, Feb. 2012.

[33]S. W. Leung, H. S. H. Chung, and T. Chan, "A ZCS isolated full-bridge boost converter with multiple inputs," in Proc. IEEE Power Electron.Spec. Conf. (PESC), 2007, pp. 2542–2548.