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A New MIC Control for the Three Level Switch Mode Rectifier


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Abstract:
Multiloop Interleaved Control (MIC) is proposed, and it is combined with Solar PV integrated Battery and the interleaved pulse width modulation scheme. The average behaviour of the interleaved three-level switch-mode rectifier (SMR) behaves similar to the conventional boost-type SMR even though two capacitor voltages are imbalanced. It implies that conventional multiloop control can be applied to the interleaved three-level SMRs to achieve the desired power factor correction function.

Index Terms:
Interleaved control, Lithium- Ion Battery, three-level boost switch mode rectifier (SMR).

I. INTRODUCTION:

THE QUALIFIED ac/dc conversion must meet the functions of input current shaping and output voltage regulation. The boost-type switch-mode rectifier (SMR), including a diode rectifier and a boost converter, is often used to perform the qualified ac/dc conversion [1]–[3]. In addition, the multiloop control with the inner current loop and the outer voltage loop is often used to generate a switching signal in boost-type SMR. However, multiloop control needs to sense three signals: current signal and input and output voltage signals. Recently, to reduce the number of feedback signals, many voltage sensor less controls (VSCs) [4]–[7] and current sensor less controls (CSCs) [8]–[10] for boost-type SMR have been proposed in the literature.

The summary of feedback signals for sensor less controls is tabulated in Table I. It is clear that fewerfeedback signals were used in sensor less control except the on in due to the additional dc load current sensing.

II. PROPOSED TOPOLOGY:

The three-level boost converter is shown in Fig. 1 where two capacitors are connected across the switches, respectively Thus, each switch needs to withstand only a half output voltage. In addition, the inductor voltage in the three-level boost converter has three levels, but the inductor voltage in the conventional boost converter has only two levels. Therefore, the three-level boost converter is able to yield smaller inductor current ripple than the conventional boost converter.

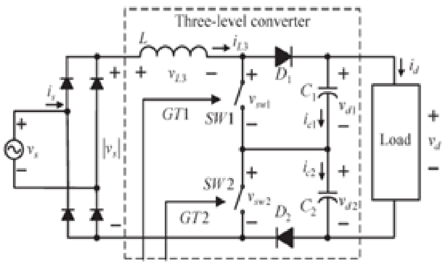

Fig. 1. Three-level SMR

It follows that three-level converters are often used in the applications, such as the high-voltage–ratio dc/dc conversion and the wide input voltage range, particularly in the fuel cell applications and the grid-connected applications.

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Additionally, the high-with standing-voltage semiconductor switches often have larger drain–source resistances than the low-withstanding-voltage ones. Thus, the three-level converter has the advantages of low voltage stress, small inductor current ripple, and low switching loss .In Fig. 1, the three-level SMR was obtained by connecting the diode rectifier with the three-level converter. In the three single-phase three-level SMRs are in Delta connection to achieve the three-phase PFC function with the ability of redundancy. The control methods for the three-level SMR (ac/dc application)can be found in where gate signals GT1 andGT2 are generated from the lookup table with inputs H1, H2,and H3. In this paper, the average behavior of a three-level SMR under the interleaved pulse width modulation (PWM) scheme (i.e., interleaved three-level SMR) is derived.

The interesting result shows that the interleaved three-level SMR be haves similar to a conventional boost-type SMR even when thetwo capacitor voltages are imbalanced. It means that the multiloop control and the interleaved PWM scheme can be integrated to achieve the desired PFC function without an additional voltage balancing loop. Thus, the proposed multiloop interleaved control (MIC) is simpler than the control method in Fig. 1. From the provided simulation and experimental results, the proposed MIC is able to achieve PFC functions, and in particular, the three-level SMR in ac/dc application is able to take several seconds to balance the capacitor voltages without the voltage balancing control loop. However, because the time taken to balance the voltages is long, the voltage balancing loop is sometimes required.

III.CONTROL STRATEGY

The proposed MIC shown in Fig. 2 combines the conventional multiloop control, the feed forward loop, and the interleaved PWM scheme. Both the voltage controller and the current controller are proportional–integral-type controllers. Two gate signals GT1 and GT2 are generated from the comparisons of control signal vcont3 and two unit saw tooth signals vtri1 and vtri2, respectively. It is noted that the two saw tooth signals have unit amplitude and identical period Ts; however, there is a 180◦phase difference between them. Both duty ratios of switchesSW1 and SW2 are equal to the MIC control signal vcont3.

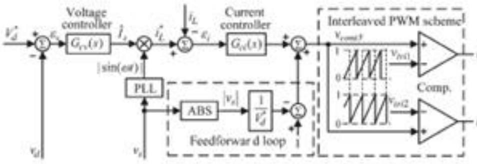

Fig. 2. Proposed MIC for three-level SMR.

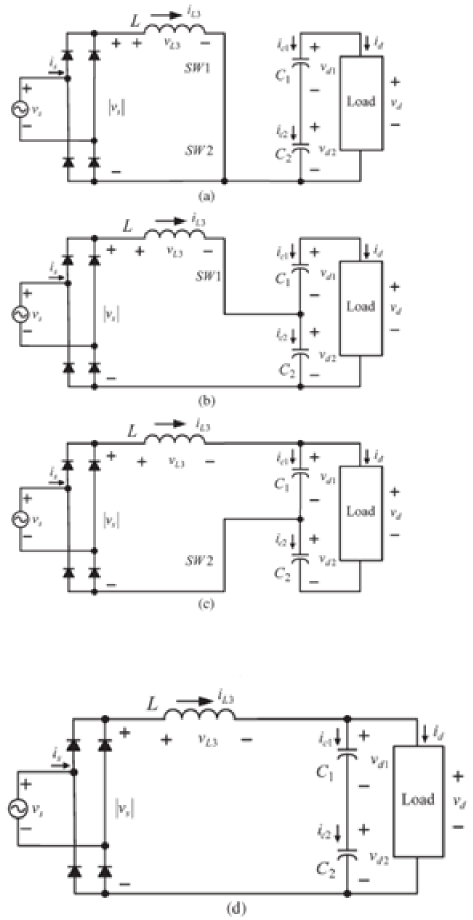

Fig. 3. Possible switching states in the interleaved three-level SMR. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

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IV.SIMULATION RESULTS

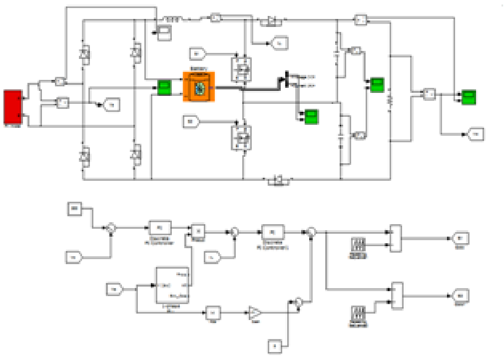

Fig 4. Simulation Circuit with PV+battery

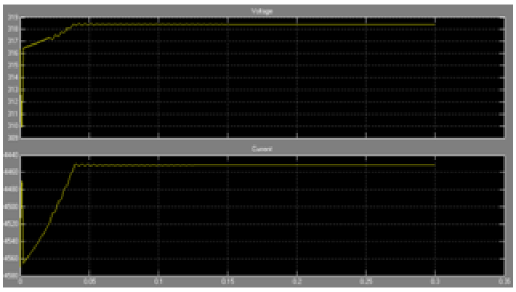

Fig 5. Battery voltage & current

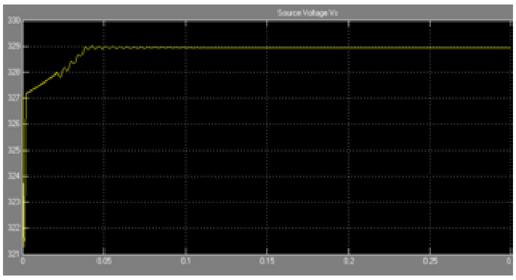

Fig 6. Source PV Voltage

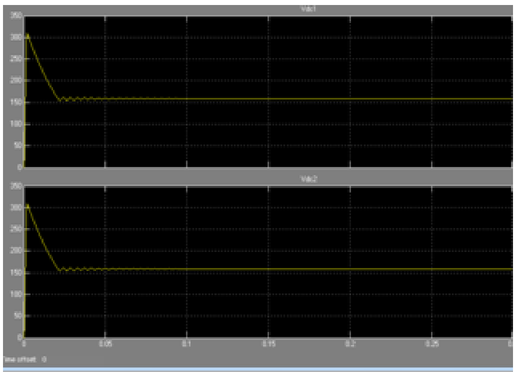

Fig 7. Vdc1 & Vdc2 Capacitor Voltages

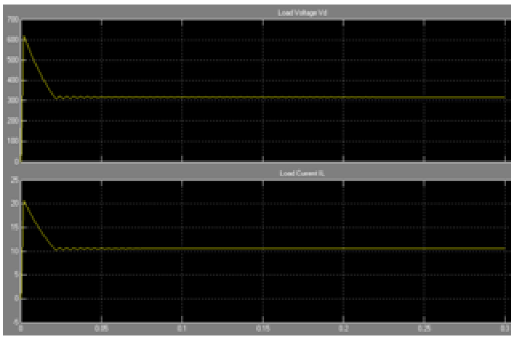

Fig 8. Load Voltage & Current

V.CONCLUSION:

In this paper, the results show that the interleaved PV+Battery based three-level SMR with the interleaved PWM scheme behaves similar to a conventional boost-type SMR. Its performance of the current shaping function does not degrade even when the two capacitor voltages are imbalanced. The MIC for the three-level SMR in ac/dc applications has been proposed simulation results have been proved.

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