ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

# Implemetation of Low Delay and Low Power Consumption Carry Skip Adder

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**Abstract:**
A carry skip adder (CSKA) structure has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrimination schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power and energy parameters with those of other adders using a 45-nm static CMOS technology for a wide range of supply voltages. The results that are obtained using HSPICE simulations reveal, on average, 44% and 38% improvements in the delay and energy, respectively, compared with those of the Conv-CSKA. In addition, the power–delay product was the lowest among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.

**Keywords:**
CSKA, Energy, Performance, VSS Hybrid-adders, voltage.

## I. INTRODUCTION:

There are many works on the subject of optimizing the speed and power of these units, which have been reported in[2]–[9]. Obviously, it is highly desirable to achieve higher speeds at low-power / energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component tin OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect [10].Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are(potentially)subject to process and environmental variations in the nanoscale technologies. The variations increase uncertainties in the a fore said performance parameters .In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region [10]. Recently, the near-threshold region has been considered as a region that provides a more desirable

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trade off point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowers switching and leakage powers compared with the super threshold region. In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors [11], suffers considerably less from the process and environmental variations compared with the sub threshold region. The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency)of the circuit based on the work load requirement[12]. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors. In addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays ,power consumption.

## II. RELATED WORK:

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The concentration on the static CMOS originates from the desire to have are liably operating circuit under a wide range of supply voltages in highly scaled technologies [10].The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of(hybrid) variable latency CSKA structures have been reported in the literature. Hence, the contributions of this paper can be summarized as follows. 1) Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer. 2) Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay.3) Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure(from the nominal supply voltage to the near-threshold voltage). 4)Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper. There is to this paper is organized as follows. Section II discusses related work on modifying the CSKA structure for improving the speed as well as prior work that use variable latency structures for increasing the efficiency of adders at low supply voltages. In Section III, the Conv-CSKA with fixed stage size (FSS) and variable stage size(VSS)is explained, while Section IV describes the proposed static CSKA structure. The hybrid variable latency CSKA structure is suggested.

## III. EXISTING CONCEPT:

Adders are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in [2]–[9]. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the

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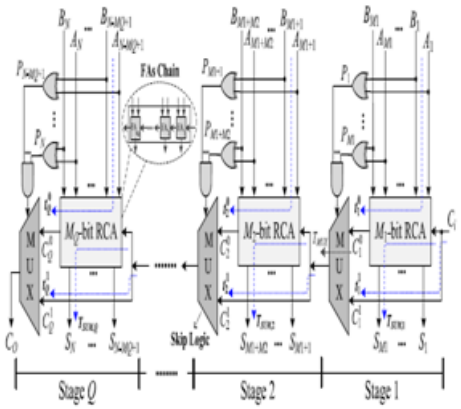


**Figure 1: Conventional Carry Skip Adder**

## DRAWBACKS:

- More area overhead system
- More power consumption
- Low speed architecture

## IV. PROPOSED METHOD:

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic.

The concentration on the static CMOS originates from the desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies [10]. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the superthreshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature. Hence, the contributions of this paper can be summarized as follows.

1) Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.

2) Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay.

3) Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure (from the nominal supply voltage to the near-threshold voltage).

4) Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper.

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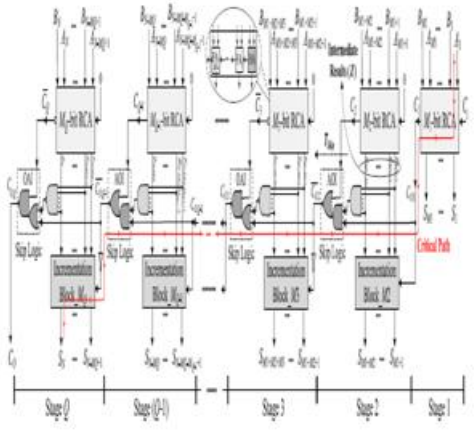

**Figure 2 : Proposed CI-CSKA Structure**

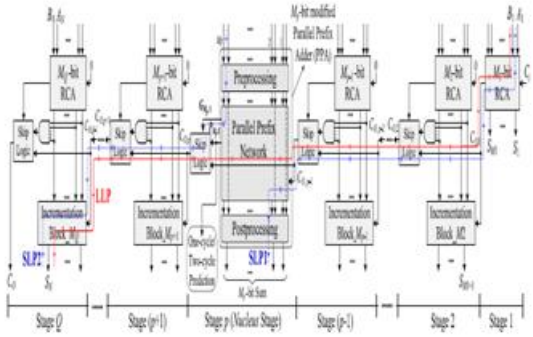

**Figure 3: Proposed Hybrid Variable Latency CSKA Structure**

## CARRY SKIP ADDER:

Modifying CSKAs for Improving Speed. The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and2:1multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1multiplexers, which can be placed in to one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder [23]. Many methods have been suggested for finding the optimum number of the FAs [18]–[26]. The techniques presented in[19]–[24]make use of VSSs to minimize the delay of adders based on a single- level carry skip logic. In[25],some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power increase considerably and less regular layout.

The design of a static CMOS CSKA where the stages of the CSKA have a variable sizes was suggested in[18].In addition, to lower the propagation delay of the adder ,in each stage, the carry look-ahead logics were utilized. Again, in that complex layout as well as large power consumption and area usage. In addition, the design approach,which was presentedonlyforthe32-bitadder, was not general to be applied for structures with different bits lengths.

## RIPPLE CARRY ADDER:

The ripple carry adder structure is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the adding of the two binary digits at different stage of the ripple carry [9]. The carry out of one stage is fed directly to the carry-input to the next stage. A number of full adders circuits may be added to the ripple carry adder or ripple carry adders of the different sizes may be cascaded in the order which accommodate binary vector strings of larger sizes [7]. For an n-bit parallel adder, it requires n number of computational elements (FA). The worst-case delay of the RCA is when a carry signal propagates ripples through all the stages of adder chain from the LSB to the MSB, which is approximated by: T = (n-1) tc+ ts where the tc is the delay through the carry stage of a different full adder, and ts is the delay used to compute the sum of the last stage.

## SKIP LOGIC:

The skip logic contains the AOI (AND OR Invert) and OAI (OR AND Invert) compound gates for skip logic. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer [7]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the exisiting one. Note that while the power consumed by the AOI (or OAI) gate are smaller than that of the multiplexer, hence the power consumption of the proposed CI-CSKA is a little more than that of the conventional carry skip adder structure [8]-[9]-[10].

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## INCREMENTATION SCHEMES:

The internal structure of the incrimination block, which contains a chain of half-adders (HAs), is shown in Figure. In addition, note that, to reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrimination block is not used. The incrimination contains AND gate and EX-OR gate. The carry input is fed into the structure and it performs the operation like the half adder.

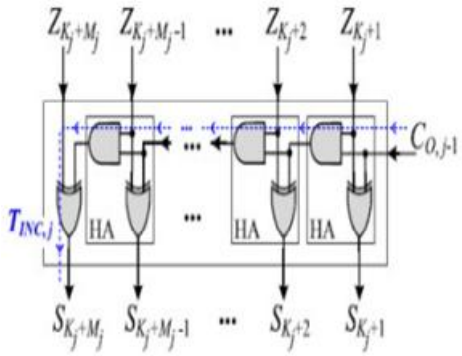
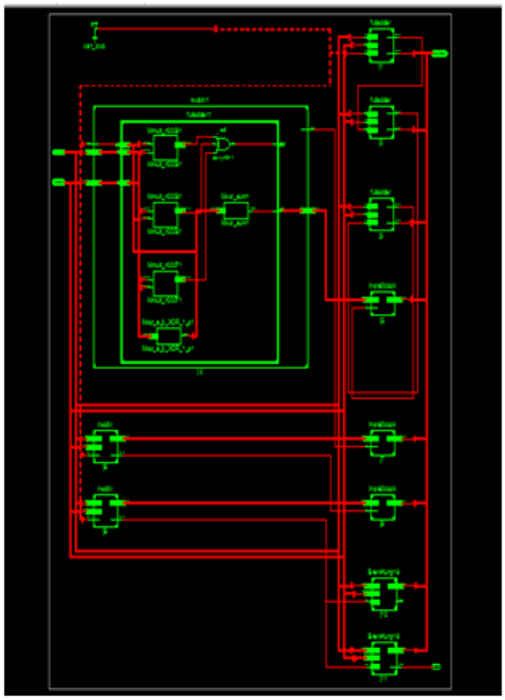



**Figure 4 : Incrementation Block**

## V. RESULTS:

### RTL schematic Result:



### Simulation Result:

## VI. ADVANTAGES:

- Low power,
- High speed

## VII. APPLICATIONS:

1. Arithmetic Logic Units.
2. Digital Signal Processing.
3. Image Processing….etc..

## VIII. FUTURE ENHANCEMENT:

We will design existing and proposed system 128 bit. This two system compare proposed system is better because proposed system is takes less area and delay. So, our modification proposed system same concept but increase the bit size.

## IX. CONCLUSION:

In this paper, Carry Skip Adder (CSKA) structure was proposed, which exhibits a higher speed and lower energy consumption compared with the conventional structure. The speed is through the concatenation and efficiency by the incrimination techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied. The results also suggested that the CSKA structure is a very good adder for the applications where both the speed and energy consumption are critical.

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In addition, a hybrid variable latency extension of the structure was proposed which reduces the power without affecting the speed of the structures.

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