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Photo Voltaic Systems Power Optimization under Cascaded Inverter Environment

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Abstract:
The proposed system is under expirimentation for achieving the systematic pattern behavioral approach under optimized multicarrier pulse width modulation technique, the proposed scheme is experimented on the five level inverter circuit to reduce the leakage current. Hence the system also incorporates the transformer less PV based infrastructure which improves the ratio of performance and also the efficiency in analyzing the leakage current losses. Under this O-MCPWM the infrastructure is aided under multilevel inverter circuit configurations. The outcome is analyzed and projected in this thesis for detailed understanding. The power optimization of the solar panels is carried out by implementing a multilevel inverter using a special optimum multicarrier PWM. Which makes use of only two carrier signals and due to which the calculations of the system are reduced and are implemented

1. INTRODUCTION:

Solar power is the solution for modern day power needs and the fact that, the solar power is a clean and less polluting and the simplicity of the process involved well suited for producing electricity. Solar panel is made to collect the sun rays as source of energy for producing electricity To improve the performance of the solar panels or cells, power electronics has good impact. Where power electronics switches can be used to charge a battery, when electric current is generated from the solar power module and while at utilization of the stored energy power semiconductor devices are used to convert the power from DC to AC.

An inverter is used to convert the DC to AC using power semiconductor devices which can handle power voltages. Simply the inverter inverts the supply from Dc to AC, Where as the inverter can give the output voltage at three levels of positive, zero and negative of the supply voltage. The Multilevel inverter has got a significance of improving the shape of the alternating voltage by using different levels of supply voltage, such that the overall outcome of the circuit resembles the sinusoidal waveform required for the better operation of the loads which work on the AC supply.
The different types of multilevel inverters are
A) FC (flying capacitor) multilevel inverter
B) DC (diode clamped) multilevel inverter
C) cascaded (H-bridge) multilevel inverter

Whereas the cascaded multilevel inverter is the advantageous multilevel inverter than diode clamped and flying capacitor multilevel inverters because of the requirement of less number of components in each level. This topology consists of series of power conversion cells and switches. And power can be scaled easily, the combination of capacitors and switches is called H-bridge and gives the separate input DC voltage for each bridge considered. There are many PWM techniques such as sin PWM, bipolar PWM, monopolar PWM, for single stage inverter and for multilevel inverter we have sin PWM, phase disposition (PD) PWM, Phase opposition disposition (POD) PWM and Alternate phase opposition disposition (APOD) PWM. Over all these PWM techniques the O-MCPWM (optimized – multicarrier PWM) is advantageous in reducing the leakage current and improving performance of the multilevel inverter.

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Where it uses only two carrier signals and hence reducing the mathematical calculations. By reducing the variation of the CMV (common mode voltages) the reduction in the leakage current in a isolation less PV systems. The PWM technique discussed is useful in reducing the leakage current and constraining the common mode voltage. The overall power generation of the solar power systems is comparatively small when compared to other power generation methods. Reducing the cost of solar power systems has got greater importance on the other hand increasing the efficiency of the solar panels has higher significance recent days. A high performance PWM algorithm with reduced common mode voltage and overall performance is proposed for three Phase PWM inverter drives. The algorithm combines the near state PWM method which has superior overall performance characteristics at high modulation index and another method, which is suitable for low modulation index range of operation [8].

Multilevel voltage source inverters synthesize the AC output terminal voltage from several levels of voltages, stepped waveforms can be produced which approach the reference waveform with low harmonic distortion thus reducing filter requirements. The need of several sources on the DC side of the converter makes multilevel topology attractive for photovoltaic and fuel cells applications. For low power grid connected applications a single phase converter can be used and it is possible to remove the transformer in the inverter in order to reduce losses, cost and size, galvanic connection of the grid and the DC sources in transformer less systems can introduce additional leakage currents due to the earth capacitance. This currents increase conducted and radiated electromagnetic emissions, harmonics injected in the utility grid losses, Amplitude and spectrum of leakage currents depends not only on converter topology, it depends not only on converter topology, it depends also on switching strategy and resonant circuit formed by ground capacitance.

Several voltage source topologies without transformer suitable for grid connection low power systems has been and ground voltage and leakage current was studied comparing the traditional full bridge topology with the multilevel half bridge neutral point clamped and cascaded full bridge topology and modulation strategy have a great influence in leakage current reduction [9]. A hybrid phase disposition pulse width modulation technique suitable for cascaded multilevel inverter, A hybrid PDPWM is developed based on low frequency sinusoidal PWM an optimized sequential switching scheme introduced in this proposed method to equalize electrostatic and electromagnetic stress among the power devices. It is confirmed that the proposed technique offers significantly lower switching losses and switching transitions furthermore, the proposed hybrid PDPWM offers better harmonic performance compared to its conventional PWM [10].

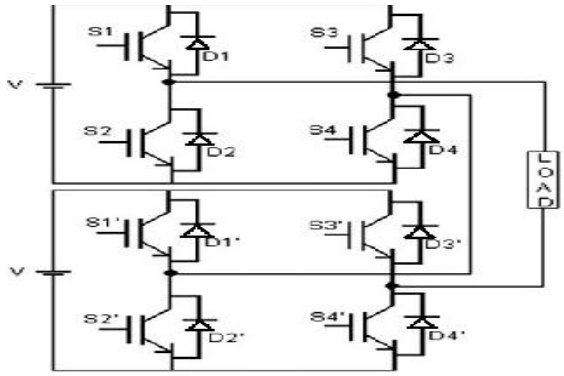

Fig 2: cascaded multilevel inverter

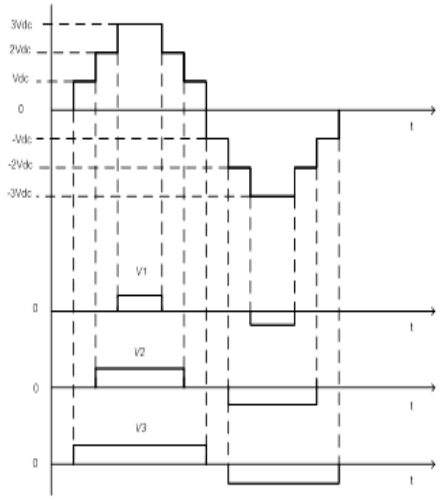

Fig1: The sample outcome of the above used inverters for seven level output

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2.OPTIMIZED-MULTICARRIER PULSE WIDTH MODULATION TECHNIQUE:

The proposed multicarrier PWM is the Optimized-Multicarrier Pulse Width Modulation technique which uses only two carrier signals to implement the switching pattern. Hence the computational burden on the designer is reduced for a better extent and the control signal generating circuit design is also simplified. In the below method of generation of the pulse width modulation only two carrier signals are used and a rectified sin signal is utilized as the modulating signal, then the carrier signals are in phase until the first half cycle and then they are phase sifted by 180 degrees along the axis as shown in the below diagram.

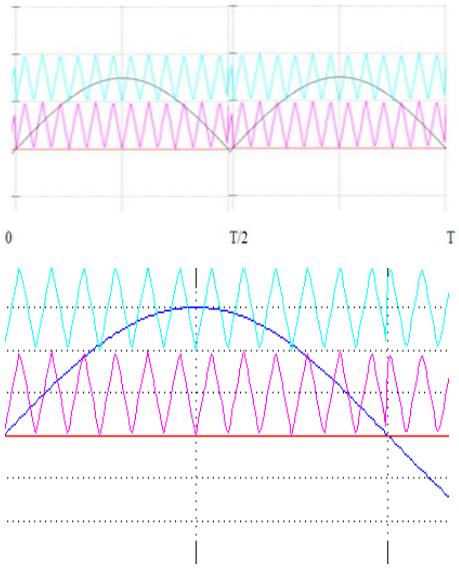

Fig 3: O-MCPWM

3. CIRCUIT OPERATION:

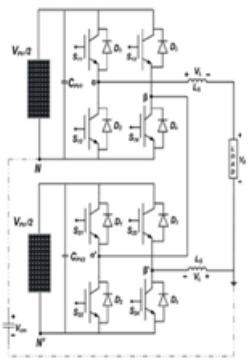

Fig 4:proposed circuit topology

Discussed and designed system under isolation less operation is encouraged and monitored under this section for development. The system is been designed and developed under the theoretical modeling of the mathematics. The proposed protocol circuit diagram is as shown below The fell H-Bridge edge multilevel inverter has the upsides of less spillage current when contrasted with the conventional uncoupled H-Bridge inverter in view of diminished cost of dc-hyperlink voltage as indicated by Bridge. The not strange multicarrier adjustment methodologies utilized in the transformer less fell H-Bridge multilevel PV inverter topologies present basic mode voltage.

This contraption proposes a cross breed multicarrier Pulse width balance (H-MCPWM) technique to reduce spillage present day in transformer less fell H-Bridge multilevel inverter for PV structures. whilst the basic mode voltage changes in a huge step value, it impels high spillage advanced inside the PV machine by means of the parasitic capacitance among the PV module and the ground. The lessened voltage move inside the normal mode voltage lessens the spillage advanced. It is easy to actualize the proposed adjustment strategy without parcels multifaceted nature and require half of the quantity of suppliers as required inside the customary MCPWM methods.

The circuit above is a single phase cascaded H-bridge inverter where two H-bridges are used in series providing a common output, All the switches put together provides a five level stepped variation of the output voltage at the final stage The voltage levels are given as $V_{PV,}$ V_{PV} /2, 0, $V_{PV,}$ V_{PV} /2 and by making a crude assumption that the common mode voltage variation is not contribute to the overall leakage current under the discussed scenario of implementation of the studied and proposed methodology. The circuit design and the firing pulse train design have prominent effect on the leakage current reduction. Therefore the complete circuit is connected to a resistive load and even a small inductive load can also be used for analysis of the circuit behavior and the design behavior under testing.

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Generally the leakage current is existing between the PV module and the ground, where the common mode voltage is also formed at the same place as shown in the schematic above. " The common mode voltage of any electrical circuit is the mean of the voltage between the outputs and a common reference" The parasitic capacitance formed for the lower and upper H-bridge is assumed to be same, as the two bridges are given Supply from similar power rated PV cells, the common mode voltage and leakage current in both the circuit topologies also considered same. The common mode voltage for the upper H-bridge is given by the equation below equation.

$$V_{cm} = \frac{V_{\alpha N} + V_{\beta N}}{2} \quad \text{---------- (1)}$$

Whereas the two terms of the numerator equation are the voltages between the upper H-bridge and the lower H-bridge inverter legs to the negative port terminal of the input side, $V\alpha'\beta'$ is the voltage between the midpoints of the pair of legs of lower H-bridge inverter, and let 'v_o' is the output voltage across the load. The leakage current mainly depends upon the magnitude of the inverter common mode voltage. In cascaded multilevel inverter. The fallowing equations can be written as

$$V_{CM} = V_o + V_L - V_{\alpha N} \quad \text{---------- (2)}$$

$$V_{CM} = V_{o'\beta'} - V_L - V_{\beta N} \quad \text{---------- (3)}$$

In the above equations (2) & (3) V_o (output voltage) and V_L (inductor voltage) are not considered for the further calculations as they have less no greater impact on the on the common mode voltage considered

Then by adding above equations we get

$$2V_{CM} = V_{\alpha'\beta'} - V_{\alpha N} - V_{\beta N} \quad \text{---------- (4)}$$

Now considering the leakage front current which can be mentioned as leakage current will flow through the parasitic capacitance, the procure option available is to restrict the voltage pressure variation of the common mode voltage. During the switching transitions of the switches, the minimized adjustment value for common mode reference voltage is given by $V_{PV}/(n-1)$ in the modulation technique called as multicarrier pulse width modulation. Simply for a phase disposition multicarrier pulse width modulation the common mode pressure voltage dose varies in the band range of +/-($V_{PV}/2$). In the method persuaded total (n-1) count of carrier signals are used, where n is considered form the level of the inverter considered for the analytical studies. The persuaded method of pulse width modulation is a improvised version of the POD (phase opposition disposition PWM), the complication is that it requires 4 carrier signals But whereas in the new technique proposed it requires only 2 carrier signals and hence it is called as the improved or advanced version of the POD or phase disposition pulse width modulation In the discussed optimized multicarrier pulse width modulation the number of the carrier signals used is (n-1)/2.as the number of signals required to compare with the modulating signal is less. The computational burden and the design complexity regarding the designing aspect of the pulse width m0dulating circuit is less. And the carrier signals are shifted by 180^0 whereas prior to the shifting and after the shifting the carrier signals are maintained such that they are in phase

Table1: switching transitions of O-MCPWM

Logic conditions	*Switches on upper H-bridge*				*Switches on lower H-bridge*				*Common mode voltage*
Mode 1(0 to T/2)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	$V_{CM'}$
$V_{c1} > V_{ref} < V_{c2}$	1	1	0	0	0	0	1	1	$V_{pv}/2$
$V_{c1} > V_{ref} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{pv}/4$
$V_{c1} < V_{ref} > V_{c2}$	0	0	1	1	0	0	1	1	$V_{pv}/2$
Mode 2 (T/2 to T)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	---
$V_{c2} > V_{ref} < V_{c1}$	1	1	0	0	0	0	1	1	$V_{pv}/2$
$V_{c2} > V_{ref} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{pv}/4$
$V_{c1} < V_{ref} > V_{c1}$	1	1	0	0	1	1	0	0	0

The switching design of the deduced method which is named after as optimized multicarrier pulse width modulation is as shown in the figure above. The operational details of the derived systematic approach is explained in two parts, Stage 1 and stage 2

Stage 1 (0 to T/2):

In this stage all the carrying signals or waves are in same phase and they are no different in terms of phase, the triple voltage formations are $-V_{PV}/2$, $-V_{PV}$, 0 formed as described below

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1) When the signal of reference is lower than the carrying signals V_{C1} and $V_{C2.}$ The Switches S_{11}, S_{14}, S_{22}, S_{23} are fired on and the other switches are namely S_{13}, S_{12}, S_{21}, and S_{24}. The trolling an output voltage of $+V_{PV}$.

2) when the signal of reference is greater than the carrier signal $V_{C2,}$ And lesser than carrier signal V_{C1} then the switches S_{14}, S_{12}, S_{23}, S_{22} are fired and the switches S_{11}, S_{13}, S_{21}, S_{24} are mot fired. At this instant the output voltage is '0'

3) When the signal of reference is greater than both the carrying signals then switches S_{13}, S_{12}, S_{23} and S_{22} are fired and the complimented switches in the circuit are kept in non conducting state and the output voltage is given by $+V_{PV}/2$

Stage 2 (T/2 to T):

In this stage all phases of the carrier signals are phase shifted by 180^0, the triple voltage formations are $+V_{PV}/2$, $+V_{PV}$, 0

1) When the carrying signals are greater than the reference signals of modulation then the switches S_{11}, S_{14}, S_{23} and S_{22} are fired on and the compliments of each above namely S_{13}, S_{12}, S_{21} and S_{24} are kept not conducting. Then the voltage synthesized is $-V_{PV}$.

2) When the reference signal of modulation is greater than the carrier signal V_{C1} and smaller than the carrier signals V_{C2}, Then the switches S_{11}, S_{14}, S_{21} and S_{23} are fired to on condition and the switches S_{13}, S_{12}, S_{22} and S_{24} are kept not conducting and the synthesized voltage output is '0'.

3) When both carrier signals are smaller than that of the reference signal of modulation, then the switches S_{11}, S_{14}, S_{21} and S_{24} are fired to on condition and the switches S_{13}, S_{12}, S_{23} and S_{22} are kept not conducting and the voltage synthesized is $-V_{PV}/2$.

4. SIMULATION AND IMPLEMENTATION OF THE CIRCUIT DESIGN

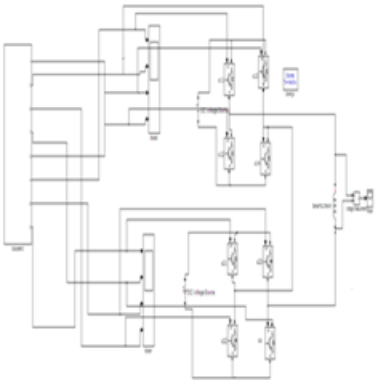

Fig 5: circuit diagram for inductive load

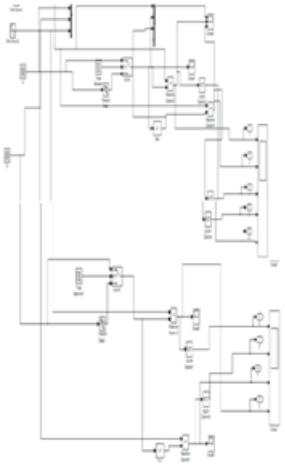

Fig 6: Circuit for optimized PWM signals

5. RESULT AND DISCUSSION:

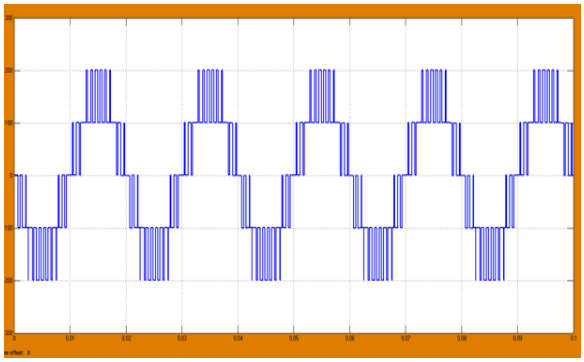

Fig 7: Five level H-bridge multilevel inverter Output waveform using O-MCPWM technique

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The above figure depicts the output waveform for a cascaded H-bridge multilevel inverter where it has five levels of the voltage variation or stages of output voltage namely V_{PV}, $V_{PV}/2$, 0, $-V_{PV}/2$, V_{PV}. By using 8 switches and an inductive load and of rating 10 milli Henry as previously shown in the figure of the H-bridge inverter drawn using simulink.

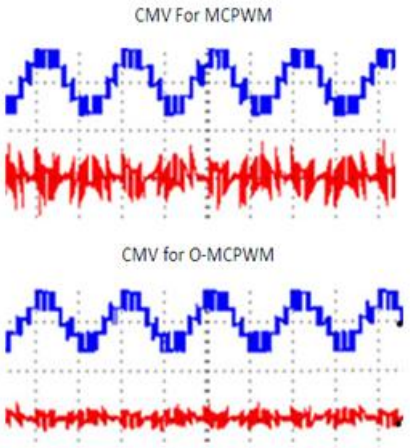

Fig 8: the common mode voltage reduction depicted by using the O-MCPWM

As already discussed the common mode voltage reduction dose not only depends on the circuit design methodology, but the common mode voltage can also be reduced by implementing the useful PWM technique. whereas the Optimized-multicarrier pulse width modulation technique can achieve a common mode voltage reduction and because of reducing the common mode voltage or restricting the common mode voltage the leakage current is reduced by a noticeable amount and hence the overall power output of the PV cells is improvised and hence the above technique of PWM can be called suitable for PVS power optimization under multilevel inverter environment. The above figure shows the reduction amount of the common mode

Table 2: compression of MCPWM and O-MCPWM

Content	MCPWM	O-MCPWM
Total harmonic distortion% (voltage)	30.29%	27.41%
Total harmonic distortion% (current)	4.71%	4.25%
Common mode voltage	High	Low
Leakage current (peak)	0.3 A	0.24 A
Leakage current (rms)	0.098 A	0.070 A
Number of carrier required	4	2

6. HARDWARE PROTOCOL DESIGN:

The designed and above discussed transformer less circuit is implemented under 5 level in vertor approach. The system is more reliable and has higher value of data acquiring and modeling. The design model is shown in below diagram.

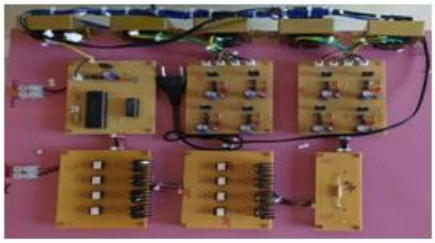

Fig 9: Hardware designed Kit for the Transformer less circuit analysis

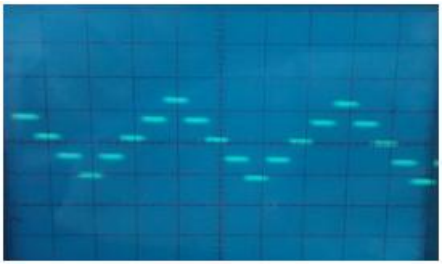

Fig10: output waveform of hardware design

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Typically the circuit consists of the MOSFITS and the 5 level inverters' for acquiring the input voltage and processing. The designed system model is highly efficient and thus retrieves the power supply by the PV cells for high gained PWM. The system is also programmed to connect the system behavioral approach of processing and trapping the incoming signals and reducing the overall leakage current.

CONCLUSION:

This postulation proposes O-MCPWM approach utilized in transformer less fell multilevel inverter for the PV frameworks. The proposed balance strategy accomplishes diminished regular mode voltage with straightforwardness in execution of the adjustment method. it's been delineated that the proposed adjustment approach has significantly less spillage present day when contrasted with the two and 3-degree inverters. it's additionally found that the proposed O-MCPWM offers substantially less aggregate symphonious bending in examination to the traditional tweak systems. It makes utilization of handiest supplier markers to produce the five-level inverter yield which in whatever other case is four in other multicarrier regulation systems.

REFERENCES:

[1] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," IEEE Trans. Power Electron., vol. 22, no. 2, pp. 693–697, Mar. 2007.

[2]Y. Zhou, W. Huang, P. Zhao, and J. Zhao, "A transformerless gridconnected photovoltaic system based on the coupled inductor single-stage boost three-phase inverter," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1041–1046, Mar. 2014.

[3]T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 184–191, Jan. 2011.

[4]E. Koutroulis and F. Blaabjerg, "Design optimization of transformerless grid-connected PV inverters including reliability," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 325–335, Jan. 2013.

[5]L. June-Seok and L. Kyo-Beum, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1720–1732, Apr. 2014.

[6]Z. Li, S. Kai Sun, F. Lanlan,W. Hongfei, and X. Yan, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic gridtied inverters," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 730–739, Feb. 2013.

[7] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1598–1607, Jul. 2008.

[8] A. M. Hava and E. Un, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," IEEE Trans. Power Electron., vol. 26, no. 7, pp. 1998–2008, Jul. 2011.

[9]O. Lopez, R. Teodorescu, and J. Doval-Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," in Proc. 32nd Annual. Conf. IEEE Ind. Electron., Nov. 2006, pp. 5191–5196.