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Implementation of Hybrid Switch Based Soft-Switching Inverter for UHE Traction Motor Drives

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Abstract:
This project presents a hybrid switch that parallels a power MOSFET and an IGBT as the main switch of a zero-voltage switching inverter. The combination features the MOSFET conducting in the low current region and the IGBT conducting in the high current region, and the soft switching avoids the reverse recovery problem during the device turn-on. A custom hybrid switch module has been developed for a variable-timing controlled coupled-magnetic type ZVS inverter with a nominal input voltage of 325 V and the continuous output power of 30-kW for a traction motor drive. Experimental results of the hybrid-switch based inverter with the total loss projected by temperature indicate that the inverter achieves 93% efficiency at the nominal condition and demonstrate ultrahigh efficiency operation over a wide load range. At 375-V input, the maximum measured efficiency through temperature projection and loss separation analysis is 92.3%.

Introduction:
A soft-switching inverter allows elimination of switching loss, but its conduction loss remains as the major part of the overall loss. If the switching device is a power MOSFET, it is possible to parallel a large number of power MOSFETs to reduce the conduction voltage drop. The problems with excessive number of paralleled MOSFETs are high cost and increased voltage drop at high temperatures. Thus, most high-power inverters have been using the insulated-gate bipolar-transistor (IGBT). In high power dc-dc converter applications, using IGBT as the main switch and MOSFET as the auxiliary switch whether series- or parallel-connected was suggested for efficiency improvement.

Hybrid Switch Configuration for a Soft Switching Inverter:
The only concern is during the turn-on process, during which a majority of the load current may flow through the power MOSFET and result in transient over-current and turn-on delay only, (2) turn-off delay only, and (3) both turn-on and -off delays. If the MOSFET die area is large enough, it is also possible to delay the MOSFET turn-off so the IGBT turn-off tail current induced loss is minimized. The circuit here is a generic soft-switching leg that can employ different auxiliary circuits to achieve zero-voltage switching.

The upper switch consists of *M*1, *Q*1, and *D*1. In a conventional hard-switching inverter, only IGBT *Q*1 and diode *D*1 are used. IGBT *Q*1 is to conduct the positive current, while diode *D*1 is to conduct the negative freewheeling current. With added *M*1, the positive load current *IL* can be shared between *M*1 and *Q*1, and the negative freewheeling current can be shared between the body diode of *M*1 and *D*1. The lower switch consists of *M*2, *Q*2, and *D*2. IGBT *Q*2 is to conduct the negative current, while diode *D*2 is to conduct the positive freewheeling current. With added *M*2, the positive load current can be shared between *M*2 and *Q*2, and the positive freewheeling current can be shared between the body diode of *M*2 and *D*2.

Only one gate signal is required for each hybrid switch pair. *G*1 controls both *M*1 and *Q*1, and *G*2 controls both *M*2 and *Q*2. The auxiliary resonant current *ILr* can be created by an auxiliary circuit or the other phase switches. Resonant capacitors *C*1 and *C*2 are connected across the hybrid switches to slow down the device voltage slew rate and to reduce the turn-off loss. If MOSFET die size is large enough, then *D*1 and *D*2 can be eliminated to save the cost.

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Use of Hybrid Switch in Coupled-Magnetic Type Soft-Switching Inverters:

Note that the conventional IGBT's antiparallel diode has been eliminated in this case because the MOSFET die size is large enough to handle the continuous reverse current. In this case, the total number of the main devices in the hybrid soft switch is the same as that in the conventional IGBT modules. Fig. 2(b) shows the forward conduction characteristic of a recently developed hybrid switch.

Temperature Characteristic:

The first generation adopted an internal bus bar structure to reduce the substrate resistance loss with the major penalty on parasitic inductance. The second generation adopted a low-profile module housing to reduce the parasitic inductance, but the substrate path causes significant conducting path resistance penalty.

The Hybrid Switch In A Phase Leg Of Inverter:

For the hybrid switch, the MOSFET turn-on delay circuit can be implemented with a resistor. *Q*1 is the upper main switch, *Q*2 is the lower main switch, *D*1 is the upper freewheeling diode, and *D*2 is the lower freewheeling diode. *Qx*1 and *Qx*2 are the auxiliary switches to produce the resonant current, *ILr*. The gate-to-emitter voltage of *Q*1, *VGE*-*Q*1, is to control *Q*1 on and off. The gate-to-source voltage of *M*1, *VGS*-*M*1, is to control *M*1 on and off.

A Variable Timing Controlled Soft Switching Inverter Using Hybrid Switches:

The copper weight and the number of layers of the printed circuit board (PCB) depend on the power requirement. In this specific design case, rather than using a heavy copper board or multilayer board with a typical 1-oz copper, multiple 4-layer standard copper boards were stacked to allow sufficient current handling capability.

Voltage turned on at zero voltage:

As compared to the waveforms obtained from the early generation modules, however, the waveform obtained in this latest generation is considerably cleaner because of significant reduction on parasitic inductances for both power traces and gate signal connections.

With the zero-voltage switching verified in the complete load range, a complete three-phase soft-switching inverter was constructed for a traction motor drive with 325-V nominal input and 55-kW peak power.

INVERTER TOPOLOGIES:

Cascaded H-Bridge Converter:

A cascade H-bridge inverter is a series connection of several H-bridges. This topology is the most obvious way of achieving a multilevel waveform. As stated earlier, the H-bridge inverter can produce voltage waveform with three discrete levels; $+V_{dc}$, 0 and $-V_{dc}$ where V_{dc} is voltage of its DC source. Therefore, a combination of a number of H-bridge inverters should be able to produce more than three level voltage output. Based on this concept the cascade H-bridge inverter is constructed. A single-phase structure of an m-level cascaded inverter is illustrated in Fig 1.1. Each separate DC source is connected to a single-phase H-bridge inverter.

Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches,S1, S2, S3, and S4. To obtain $+V_{dc}$, switches S1 and S4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by $m = 2s + 1$, where s is the number of separate DC sources.

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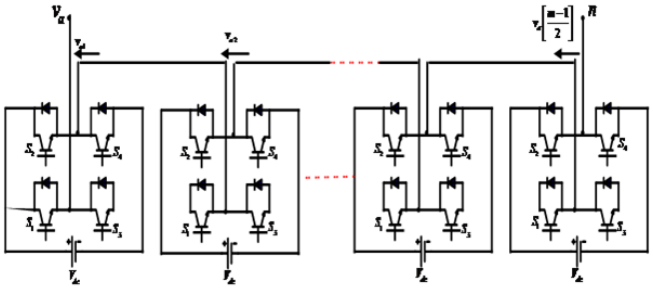

Fig 1: Single phase structure of a multilevel cascaded H-bridge inverter

For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration. For example, a wye-configured five-level inverter using cascaded-inverters with two separated capacitors is illustrated in Fig 1.2. The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng and Joos have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate DC sources, which is the case in applications such as photovoltaic or fuel cells.

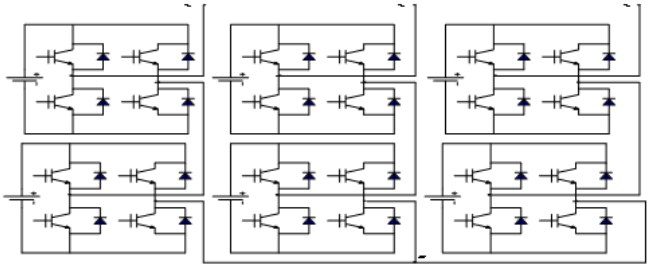

Fig 2: A five-level three-phase Wye-configuration cascaded H-bridge inverter Cascaded

Inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra capacitors are well suited to serve as separate DC sources. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply.

For simplicity, the switching devices along with anti-parallel diodes are represented by correspondingly placed two-way switches. As can be analyzed from this figure that a current flowing from positive terminal of the upper DC-link capacitor to b1, a2, a12, b11 and then to negative terminal of the same capacitor will cause short-circuit in the circuit.Therefore, by nature of this topology, it is impossible to apply it in the applications such as UPFC, UPQC, etc.

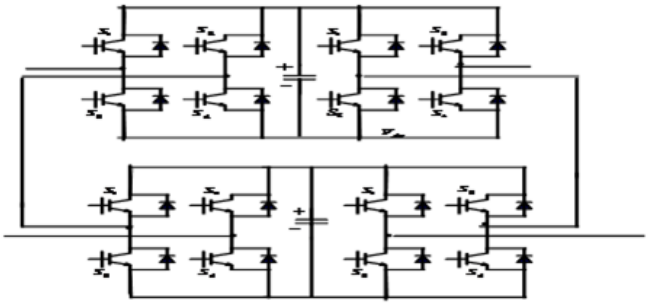

Fig 3: A back-to-back connected cascaded H-bridge inverter arrangement.

Diode Clamped Multilevel Inverter:

The first practical (and still widely studied) multilevel topology is the neutral-point-clamped (NPC) PWM topology first introduced by Nabae, et al., in 1981. This is essentially a three-level diode-clamped inverter also called three-phase NPC topology.The NPC consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the main DC voltage into smaller voltages.

In this the main DC voltage is divided into two. If the point 'n' is taken as the ground reference, the three possible phase voltage outputs are $-V_{dc}/2$, 0, or $V_{dc}/2$. The line-line voltages of two legs with the common DC capacitors are: V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$ or $-V_{dc}$. Similar switch states exist in all the three phases to produce corresponding three-level voltage outputs.

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The key components that distinguish this circuit from a conventional two-level inverter are D_{11}, D_{12}. These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both S_{a1}, S_{a2} turn on, the voltage across a Van is $V_{dc}/2$, i.e., Van = $V_{dc}/2$.

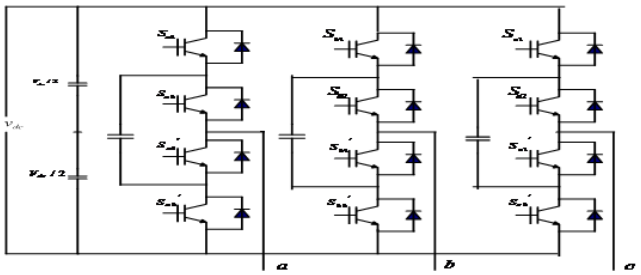

Fig 4: Three-phase three-level structure of a diode-clamped multilevel inverter

(Table 1.1) In this case, D_{12} balances out the voltage sharing between (S_{a2}, S_{a2}') with S_{a1}' blocking the voltage across C1 and S_{a2}' blocking the voltage across C2.

Table 1.1 Switch states and the output voltages for three-level diode-clamped inverter.

S_{a1}	S_{a2}	S_{a1}'	S_{a2}'	V_{an}
1	1	0	0	$V_{dc}/2$
1	0	0	1	0
0	0	1	1	$-V_{dc}/2$

Flying Capacitor Multilevel Inverter:

Meynard and Foch introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The three-level flying capacitor topology, shown in Fig. 5, can be considered a good alternative to overcome some of the NPC topology drawbacks. In this topology, additional levels and voltage clamping are achieved by means of capacitors that 'float' with respect to the DC source reference.These floating capacitors are commonly called as 'flying capacitors' and due this arrangement this topology is named as flying capacitor topology.

In the three-level flying capacitor topology shown in Fig. 5, the capacitors C_a, C_b and C_c are flying capacitors of the three individual phase legs and C1, C2 constitute the DC-link. In the three-level converter of Fig. 1.5, all the capacitors shown are regulated at a voltage of $V_{dc}/2$. Depending of the modulation scheme used, the three-level inverter is switched in such a way to maintain the flying capacitors voltage at $V_{dc}/2$. By doing so, the voltage stress across inverter devices keeps limited to $V_{dc}/2$.

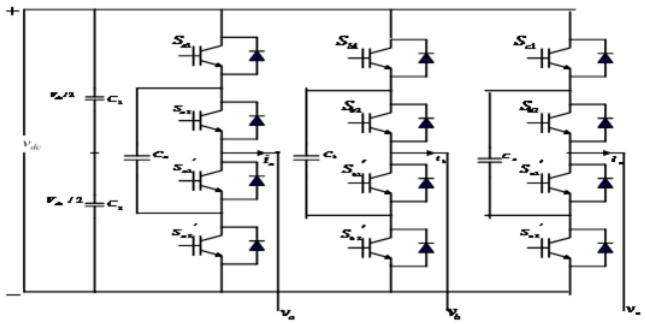

Fig 5: Three-phase three-level structure of a flying capacitor multilevel inverter

S_{a1}	S_{a2}	V_{an}	C_a
On	On	$+V_{dc}/2$	No change (NC)
On	Off	0	Charging (+)
Off	On	0	Discharging (-)
Off	Off	$-V_{dc}/2$	No change (NC)

Table 2: Switch states and the output voltages for three-level flying capacitor inverter

RESULTS:

The inverter operates under discontinuous PWM mode with10-kHz switching frequency. It was tested with three voltage levels: 275, 325, and 375 V with a 4-pole, 90-kW induction motor for electric vehicle traction drives. Fig. 11(a) shows the output phase current waveforms at 1030-rpm, 225-Nm load condition. The inverter output current is 146 A rms, and the output power is 27 kW under this load condition. Fig. 11(b) shows the inverter output current waveforms at 3030-rpm, 110- Nm load condition at 275-V input. In this case, the inverter output current is 150 A rms, and the output power is 39 kW. Fig. 11(c) shows the inverter output current waveforms at 2980 rpm, 110 Nm motoring load under 375-V dc input

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voltage condition. In this case, the inverter output current is about 100 A rms, and the output power is 38 kW. Higher input voltage tends to have lower output current at the high speed region because the control loop adapts the maximum torque per ampere (MTPA) control to minimize the motor current with the available input voltage. Note that the continuous testing power level far exceeds the continuous rated power because the heat sink and chassis used in the existing vehicle chassis have sufficient thermal capacity margin. The peak power was not tested with the dynamometer, but it was tested on the vehicle during startup and short-term acceleration conditions.

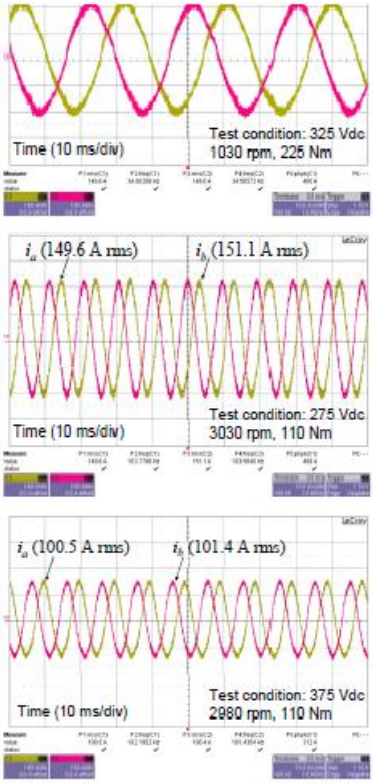

Fig 6: inverter output current waveforms

In this measurement, the auxiliary power and fan losses are included as a part of total losses. With hybrid switch and adaptive timing soft-switching operation, the efficiency at 325-V input exceeds 99% at 30-kW nominal load condition. At 375-V input, 38-kW output, the efficiency reaches 99.3%. Such high efficiencies cannot be measured accurately with a power meter that measures the dc input and PWM ac output. Some operating points, however, were verified with a differential calorimeter in the first generation inverter, which had a peak efficiency of 99.1%. To verify the efficiency numbers for this version, the approach is to measure the module case temperature and couple magnetic winding temperature over a long period and use them to estimate the efficiency.The 325-V condition was started at a temperature that is considered steady state, so over the 12-minuteinterval there was not any appreciable temperature rise.At the 20°C room temperature test condition, the entire inverter was only cooled by a 3-W fan, and the monitored module which is far away from the fan has a case temperature of 47°C under steady state 325-V input, 38-kW output condition

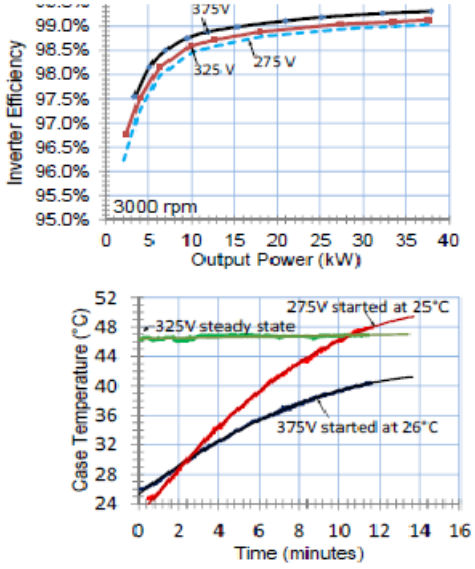

Fig 7: Measuring Efficiency, module

At 375-V dc input voltage and 37.59-kW output power condition, the inverter output was measured with phase-to neutral voltage 143 Vrms, peak current 144 A, power facto 0.862, and input power 37.86 kW. The individual loss components under this condition are listed in Table 1. It should be noticed that the main power devices are responsible for the dominant loss component. With soft switching, the achieved ultrahigh efficiency is mainly attributed to the conduction voltage drop reduction by the hybrid switch. With near zero switching loss in both main and auxiliary switches, the next major loss item is the

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magnetic component, which accounts for 11% of the total loss in this specific case. The third major loss item is the auxiliary power supply which supplies power to the gate drives, controller, conditioning circuit, and fan with a total of 19 W, or 7.0% of the total loss. The dc bus capacitors, power bus, and other parasitic losses attribute another small percentage. With continuing improvement of super-junction power MOSFET technologies, the room for efficiency improvement can be anticipated in a near future. Fig. 12(a) shows the test vehicle that was equipped with the soft-switching inverter. The soft-switching inverter replaces the existing vehicle inverter for on-the-road test. The inverter and motor operating conditions are monitored through the entire test cycle. The 4-minute drive cycle data including the motor speed, peaking at 1100 rpm and inverter output current, which peaks at 360-A. The inverter performed very well with unnoticeable temperature rise after 15-minute driving around a city block near Boston, Massachusetts.

CONCLUSION:

A hybrid switch has been proposed as the main switch of soft-switching inverters. The switch consists of the power MOSFET to conduct the low-current portion and the IGBT to conduct the high-current portion. The use of the proposed hybrid switch in a soft switching circuit avoids the reverse recovery problem of the power MOSFET while taking advantage of the low voltage-drop body diode with synchronous rectification. This combination not only eliminates the switching loss, but also reduces the conduction loss substantially. Using the custom hybrid switch module in a variable-timing controlled coupled magnetic type ZVS inverter demonstrated an ultrahigh efficiency operation over a wide load range. Experimental results with the total loss projected by the temperature rise and loss separation analysis indicate that at the nominal 325-V input, 30-kW output, the efficiency is 99%, and at a 375-V input and 38-kW output, the efficiency exceeds 99.3%.

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