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An Efficient Design of Reversible Binary and BCD Adder Using VERILOG HDL

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Abstract

Reversible logic has emerged as a possible low cost alternative to conventional logic in terms of speed, power consumption and computing capability. An adder block is a very basic and essential component for any processor and optimized design of these adders' results in efficient processors. In this work we propose optimized Binary adders and BCD adders. The adders designed in this work are optimized for Quantum cost, Delay and Area. A modified BCD adder is also proposed which removes redundancy in the circuit and acts as most efficient BCD adder. Here we explore the use of Negative control lines for detecting overflow logic of BCD adder which considerably reduces Quantum cost, delay and gate count which result in high speed BCD adder with optimized area which give way to lot of scope in the field of reversible computing in near future.

I-BIT REVERSIBLE FULL ADDER:

There are various variants of Toffoli gate. 2*2 Toffoli gate is generally called CNOT gate / Feynman gate. A I-bit reversible full adder has been designed using only n*n positive controlled Toffoli gates as shown in Fig 3. The proposed design is simple and has a gate count of 4 with 0 garbage output. The proposed 1-bit reversible full adder is shown in below figure 1

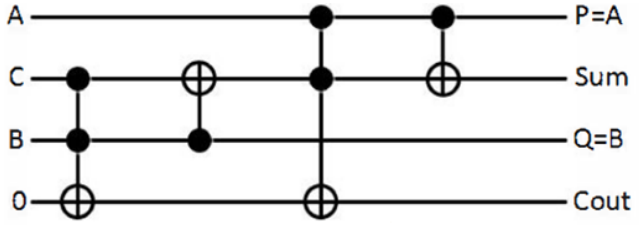

FIGURE 1: PROPOSED I-BIT REVERSIBLE FULL ADDER

4-BIT REVERSIBLE FULL ADDER:

Proposed reversible 4-bit ripple carry adder has been designed using four I-bit reversible adders as shown in Fig 4. It is characterized by a quantum cost of 48 and a delay of 40t:J.. For each stage of input, I ancilla input is required producing no garbage output. The proposed design performs better in terms of quantum cost and delay when compared to previous works. When compared to [15, 19], the quantum cost has been reduced by 18.75% for an 8-bit adder. In rest of the paper proposed reversible 4-bit full adder will be called by the name 'NAFA'. The proposed 4 bit reversible full adder design (NAFA) is shown in figure 2.

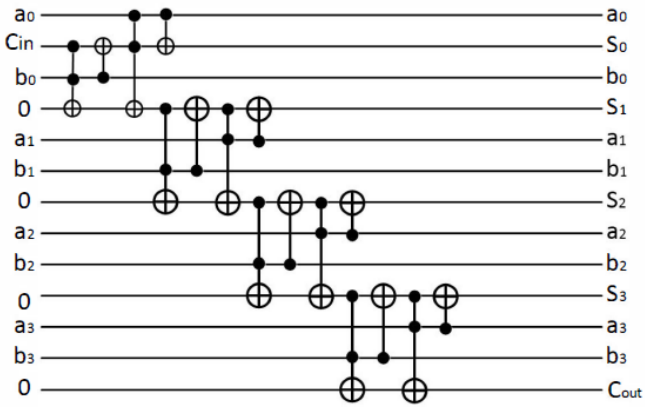

FIGURE 2: PROPOSED 4-BIT REVERSIBLE FULL ADDER DESIGN (NAF A)

4-BIT REVERSIBLE BCD ADDER DESIGN (DESIGN 1):

BCD codes makes calculation and analysis more simple in processor design. A BCD adder plays a major role in these designs. A conventional BCD adders are constructed using Full Adder circuit with an overflowing detector circuit. In this design we have

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proposed a 4-bit reversible BCD adder using proposed reversible full adder circuit (NAF A) and an overflow detector circuit as shown in Fig 5. The overflowing detector circuit has been designed using two 3 *3 negative controlled Toffoli gates and a positive controlled Toffoli gate. The use of negative logic reduces the gate count and hence aids the requirement. In this design two reversible 4-bit full adders (NAF A) are used to realize the reversible BCD adder. The proposed 4-bit reversible Bcd adder design is shown in figure 3.

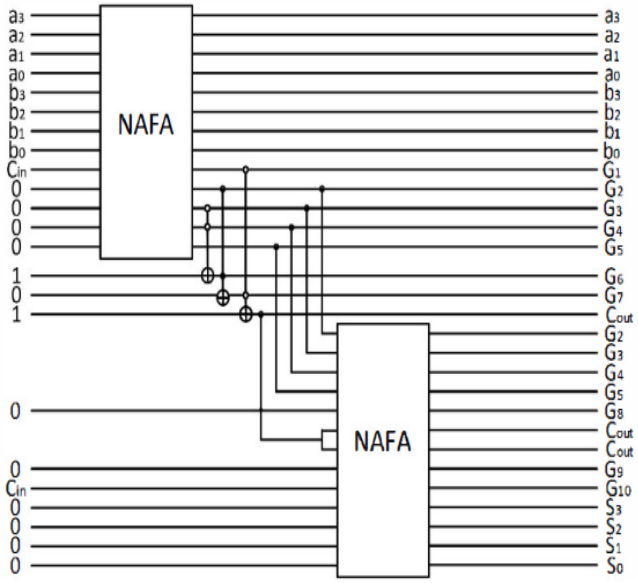

FIGURE 3: PROPOSED 4-BIT REVERSIBLE BCD ADDER DESIGN

MODIFIED 4-BIT REVERSIBLE BCD ADDER DESIGN (DESIGN 2):

A BCD code consists of numbers from 0 to 9 and any value greater than the range is corrected by adding 6 (0 I 10) to the resulting value. There is a need to detect this overflow of the resulting value. Hence we have designed overflow logic using negative controlled Toffoli gate followed by a 4-bit reversible full adder to add 6 to the resulting value. But we need to add l's only for 2nd and 3rd bits. Hence we need only two I-bit adders to perform the same instead of 4-bit full adder as discussed in previous section. Hence we modified the previously proposed BCD adder design with the one as shown in Figure 4.

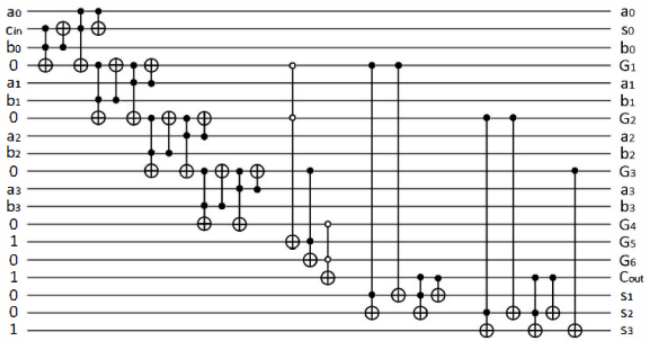

FIGURE 4: PROPOSED 4-BIT MODIFIED REVERSIBLE BCD ADDER DESIGN

METHODOLOGY

A. REVERSIBLE BINARY FULL ADDER:

The methodology adapted is to ripple the carry through each stage of full adder circuit. Thus the proposed 4-bit reversible full adder is the cascade of four I-bit full adders with a Quantum cost of 48 and delay of 40LL The delay calculation process has been shown diagrammatically in Fig 7. According to the design, for each group of 2*2 and 3*3 Toffoli gate, delay is found to be

$$\Delta = \max(1\Delta, 5\Delta) = 5\Delta$$

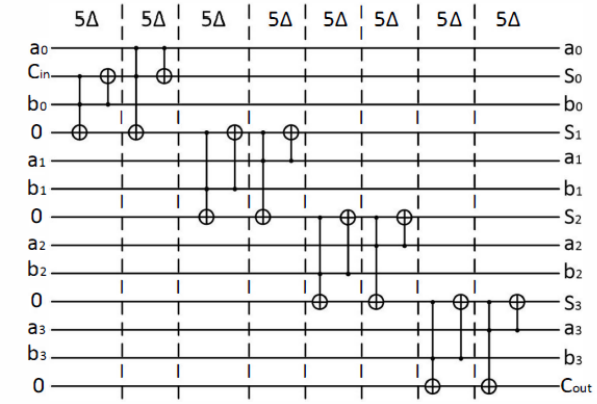

FIGURE 5: DELAY CALCULATION IN 4-BIT REVERSIBLE FULL ADDER DESIGN

Since there are 8 such pairs, the total delay for a 4-bit reversible full adder is found to be 40Δ. the general expression to find delay for an n-bit reversible binary adder is as shown below:

$$\Delta_{total} = \sum_{i=1}^{2n} \max(1\Delta, 5\Delta)$$

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Reversible BCD Adder:

A binary coded decimal is a form of number system in which every four bits of a number is represented by its equivalent value. For example, a decimal number 45 is represented as 0100 0101 in BCD system. This makes things simple and facilitates the logic designer to understand the logic. While designing a combinational circuit using BCD logic, we may need to perform different operations on it such as addition, subtraction, etc. While performing any operation, there may be chances of overflowing the range of the number system. In such a case, a detector and corrector circuit needs to be present. During BCD addition if there is any overflow, the logic to correct is to add 6 (0 I I 0) to the resulting data.

The design methodology involves detecting overflow of the resulting sum from 4-bit reversible full adder and then adding 6 to it using another 4-bit reversible full adder. In this proposed design, we have used cascade of two negative controlled Toffoli and a positive controlled Toffoli gate to detect the overflow and have used nother 4-bit reversible binary adder to correct it by adding 6 (0110) to the output of first full adder. By this the quantum cost has been found to be 113 with gate count of 35 and delay of 97LL In case of modified full adder (Design 2), we have removed the redundancy present in the reversible BCD adder proposed (Design I) as we need only two I-bit full adder instead of 4-bit full adder. This will reduce the delay as well as area.

COMPARISION

Reversible Binary Full Adder:

n-bit reversible binary full adder proposed is characterized by the quantum cost of 12n, delay of IOn, 4n ancilla inputs and 0 garbage outputs. When compared to [15, 19], the quantum cost of the proposed design has been reduced by 18.75% for an 8-bit adder. The delay has been improved by 7.5% when compared to [18]. Table I gives the comparison of n-bit full reversible binary full adder. Table II gives the percentage improvement in quantum cost for different bits.

TABLE 1. COMPARISON OF N-BIT REVERSIBLE FULL ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[18]	0	0	17n-6	10n+6
[19]	0	0	17n-22	15n-6
[15]	0	0	15n-6	9n+1
Proposed	4n	0	12n	10n

TABLE 2: QUANTUM COST COMPARISON OF N-BIT REVERSIBLE FULL ADDER

Bits	*[19]*	*[15]*	*Proposed*	*% Improvement w.r.t [19]*	*%Improvement w.r.t [15]*
8	114	114	96	18.75	18.75
16	250	234	192	30.20	21.87
32	522	474	384	35.93	23.43
64	1066	954	768	38.80	24.21
128	2154	1914	1536	40.23	24.61
256	4330	3834	3072	40.95	24.80
512	8682	7674	6144	41.30	24.90

REVERSIBLE BCD ADDER:

TABLE 3. COMPARISON OF 4-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[10]	68	72	440	Not Mentioned
[11]	28	24	220	Not Mentioned
[12]	16	16	676	Not Mentioned
[13]	56	64	336	Not Mentioned
[14] (Design 3*)	8	24	412	Not Mentioned
[15] (Work 3*)	4	3	280	228
[16]	6	10	Not Mentioned	Not Mentioned
[17]	17	22	Not Mentioned	Not Mentioned
Proposed (Design 1)	13	10	113	97
Proposed (Design 2))	10	6	90	80

In [14] 6 designs and in [15],4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

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TABLE 4: QUANTUM COST COMPARISON OF N-BIT REVERSIBLE BCD ADDER

Bits	*[11]*	*Proposed Design 1*	*Proposed Design 2*	*% Improvement of Design 1 w.r.t [11]*	*% Improvement of Design 2 w.r.t [11]*	*% Improvement of Design 2 w.r.t Design 1*
8	440	226	180	94.69	144.44	25.55
16	880	452	360	94.69	144.44	25.55
32	1760	904	720	94.69	144.44	25.55
64	3520	1808	1440	94.69	144.44	25.55
128	7040	3616	2880	94.69	144.44	25.55

When compared to the previous works, the proposed BCD adder using reversible binary full adder has better quantum cost. The results of all the previous works and our proposed design have been summarized in table iii. The percentage improvement in quantum cost when compared to [11] is 94.69% and delay improvement is 135.05% compared to [15]. Though the ancilla inputs and garbage outputs are more compared to [15], the quantum cost and delay has been optimized to a greater extent.

The quantum cost comparison of n-bit reversible BCD adder is as shown in table (iv). The modified BCD adder designed is much more efficient than proposed BCD adder (design 1). For a 4-bit adder, the percentage improvement in quantum cost when compared to design is 25.5% and also 21.25% improvement in delay. Hence it is much more efficient than the proposed design 1. Table v gives the comparison of n-bit reversible BCD adder.

TABLE 5. COMPARISON OF N-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[10]	17n	18n	110n	Not Mentioned
[11]	7n	6n	55n	Not Mentioned
[12]	4n	4n	169n	Not Mentioned
[13]	14n	16n	84n	Not Mentioned
[14] (Design 3*)	2n	6n	103n	Not Mentioned
[15] (Work 3*)	n	n-1	70n	57n
Proposed (Design 1)	$3n+\frac{n}{4}$	$2n+\frac{n}{2}$	$28n+\frac{n}{4}$	$24n+\frac{n}{4}$
Proposed (Design 2)	$2n+\frac{n}{2}$	$\frac{3n}{2}$	$22n+\frac{n}{2}$	20n

In [14] 6 designs and in [15], 4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here

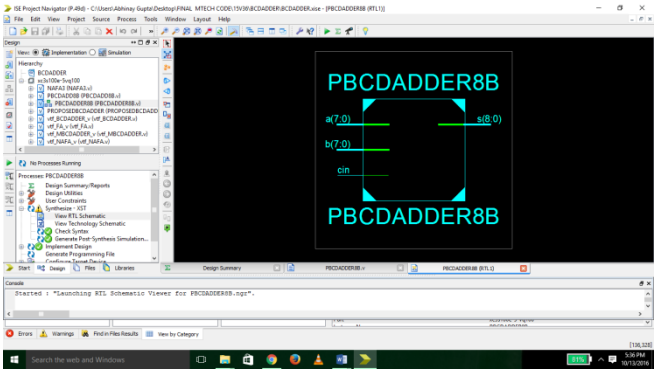


FIGURE 6: RTL SCHEMATIC OF TOP-LEVEL OF MODIFIED BCD ADDER

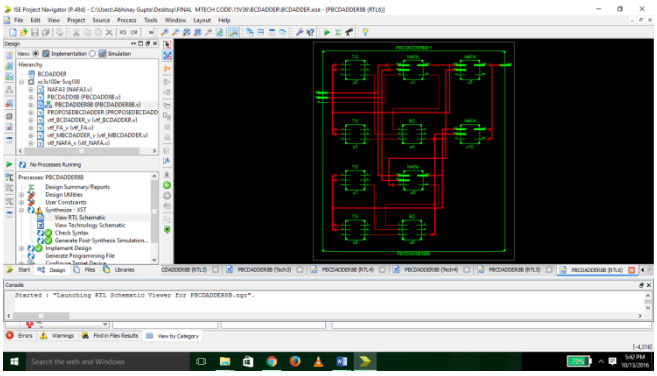
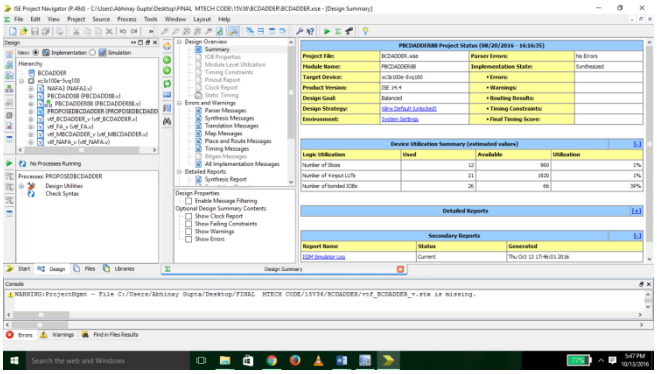


FIGURE 7: TECHNOLOGY SCHEMATIC OF INTERNAL BLOCK OF PROPOSED SQUARER



SYNTHESIS REPORT OF MODIFIED BCD ADDER

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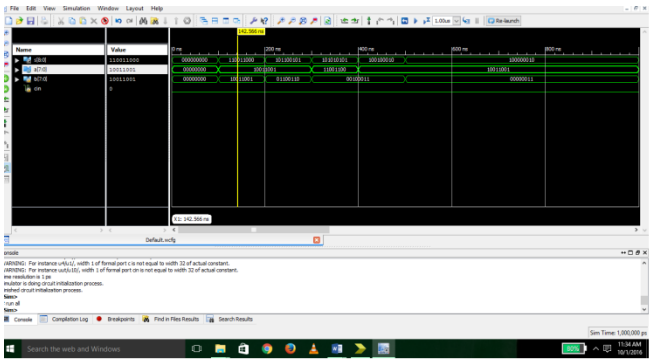

FIGURE 8: SIMULATED OUTPUTS FOR PROPOSED MODIFIED BCD ADDER

CONCLUSION AND FUTURE WORK

In this work, we have proposed a reversible binary adder design with optimized quantum cost and delay compared to previous work in literature and using this adder, an optimized reversible BCD adder in terms of Quantum cost, delay and garbage outputs have been designed. All the designs are functionally verified using Xilinx ISE tool. The use of negative control lines in the design for detecting overflow logic of BCD adder has considerably reduced delay and gate count which result in high speed BCD adder with optimized area. Thus we conclude that the use of Negative control lines reduces the gate count and hence area, for specific signal processing which gave way to lot of scope in the field of reversible computing in near future.

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