

Design of Wi-Fi MAC Layer for Transmitter using Verilog HDL

Moodu Balaji

M.Tech,

(VLSI & Embedded System),

Siddhartha Institute of

Engineering and Technology.

T.A.Ashok Babu

Assistant Professor,

Department of ECE,

Siddhartha Institute of

Engineering and Technology.

Dr.Dasari Subba Rao, Ph.D

HOD,

Department of ECE,

Siddhartha Institute of

Engineering and Technology.

Abstract:

The main purpose of the IEEE 802.11 standard is to provide wireless connectivity to devices that require a faster installation, such as Laptops, PDA's or generally mobile devices inside a WLAN. MAC procedures are defined here for accessing the physical medium, which can be infrared or radio frequency. The main objective is to design and implementation WIFI MAC Transmitter using Verilog HDL. For the wireless communication in RF range IEEE 802.11 is one of the many standards available. IEEE 802.11b defines the Medium Access Control Layer for wireless local area networks. Wi-Fi MAC transmitter module is divided into 5 blocks i.e.. data unit interface block, controller block, payload data storage block, MAC header register block, data processing block. In this project, we are considering only two blocks i.e. payload data storage block, data processing block. All the synthesis and simulations are done using verilog HDL on Xilinx 14.4 ISE.

Keywords:

Wi-Fi MAC layer, IEEE 802.11b, FIFO, DLC, HEC, CRC.

I. INTRODUCTION TO WIFI:

Wireless Technology is an alternative to Wired Technology, which is commonly used, for connecting devices in wireless mode. Wi-Fi (Wireless Fidelity) is a generic term that refers to the IEEE 802.11 communications standard for Wireless Local Area Networks (WLANs). Wi-Fi Network connect computers to each other, to the internet and to the wired network. The WLAN (Wireless Local Area Network) protocol, IEEE 802.11, allows wireless and mobile network access to a network infrastructure.

Before the 802.11b protocol (which was coined Wi-Fi) was widely adopted in the early 2000s, to get high speed network access to your LAN you had to be physically connected via a cable. The family of 802.11 protocols are made up of an arrangement of over-the-air modulation techniques that use the same basic principles. The most widely used protocols are the 802.11b, 802.11g and 802.11n for 2.4GHz networks and the 802.11a, 802.11n and 802.11ac for 5GHz networks.

II. OVERVIEW OF MAC LAYER:

Before transmitting frames, a station must first gain access to the medium, which is a radio channel that stations share. The 802.11 standard defines two forms of medium access, distributed coordination function (DCF) and point coordination function (PCF). DCF is mandatory and based on the CSMA/CA (carrier sense multiple access with collision avoidance) protocol. With DCF, 802.11 stations contend for access and attempt to send frames when there is no other station transmitting. If another station is sending a frame, stations are polite and wait until the channel is free. As a condition to accessing the medium, the MAC Layer checks the value of its network allocation vector (NAV), which is a counter resident at each station that represents the amount of time that the previous frame needs to send its frame. The NAV must be zero before a station can attempt to send a frame. Prior to transmitting a frame, a station calculates the amount of time necessary to send the frame based on the frame's length and data rate. The station places a value representing this time in the duration field in the header of the frame. When stations receive the frame, they examine this duration field value and use it as the basis for setting their corresponding NAVs.

This process reserves the medium for the sending station. Medium Access control [MAC] layer performs function like i) On transmission, assemble data in to a frame with address and error detection fields ii) On reception, disassemble frame and perform address recognition and error detection iii) Govern access to the LAN transmission medium Physical layer performs functions like. i) Encoding/decoding of signals ii) Preamble generation/ removal [for Synchronization].iii) Bit transmission I reception iv) Includes specifications of the transmission medium [4].

III.WI-FI FEATURES Wi-Fi:

Wireless Fidelity [802.11 family of standards] for LAN. WiFi is designed for local area networks, which are private, local (short range), but where competing cable systems run at very high speeds. WiFi achieves greater than 10MBit/ Sec throughput for a user in many circumstances. Currently WiFi carries more user data than any other wireless technology. Evolution is to go further, faster and at lower power consumption [2] Upstart wireless LAN [WLAN] technologies Funder the 802.11 (Wi-Fi) umbrella have leapfrogged Ktowards cellular and other efforts edging towards broad IO band wireless [such as 802.16! WiMAX] and have led to Have the first wide spread, commercially successful broadband wireless access technology . Infact, Wi-Fi is a runaway A a success around the globe [5].

IV.PROPOSED BLOCK DIAGRAM OF TRANSMITTER:

As discussed earlier, the transmitter block is Fig 4 Block diagram of transmitter divided in to five parts as shown in fig 4 and only two blocks are considered for Verilog HDL simulation. These are Payload Data Storage block & Data Processing block.

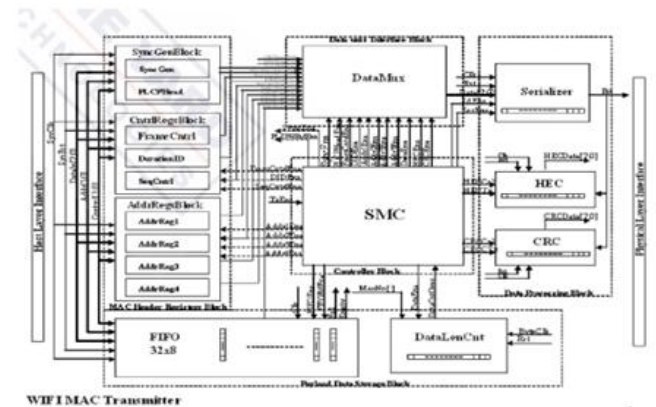


Fig. 1: Block Diagram Of Transmitter

A. Payload Data storage block:

Is further divided into two modules i.e. FIFO module & Data length counter module. These modules are discussed as shown below.

1) FIFO Module:

FIFO Module is shown in Figure 2 a. It contains the data to be transmitted. It acts as the synchronizing tool i.e. the data are entered at high rate but it is retrieved at the slower rate. Here, we have taken 32x8 bits of data storage. Here, the first incoming data goes out first. It acts on two clocks i.e. SysClk and ByteClk, on their rising edge and when the FIFO is enabled the input data is retrieved. The Full and Empty signals shows the state of the FIFO.



Fig. 2: FIFO Module

2) Data length counter module:

Fig. 3 shows Data length conter module. This module acts as a counter. It simply accepts a Max Number and counts the data being transmitted.

When the number field of the data is equal to the Max Number then the Data When the TxEna signal is high, then the CRC data is Count Over signal is turned high. It acts at every rising given out and when the CRCCIena is high, then the CRC edge of the clock.



Fig. 3: Data length counter module

B. Data Processing Block:

It is divided in to three modules i.e, serializer module, HEC and CRC modules and they are discussed in details as shown below

1) SerialiZer Module:

Fig. 4 a shows serializer Module. It is basically the parallel input and serial out put device. Various data selected at the multiplexer are serially obtained. It occurs at every rising edge of the clock and when the serial enable is high. The output bit is designated as SBit. When all the output bits are over, then the End of Conversion i.e. efficiency of EOC goes high.

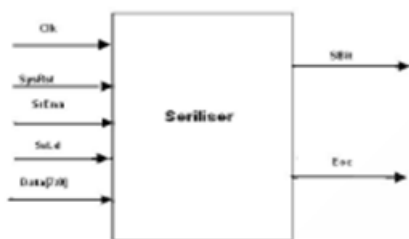


Fig.4: SerialiZer Module

2) HEC Module:

Fig. 5 shows HEC Module. This module produces the Head Error Check bits. It is the 16-bit error check bit. The HEC is calculated when the HRCCaEna is high and when the TxEna is high then the HEC data is transmitted along with the PLCP Header Bits.

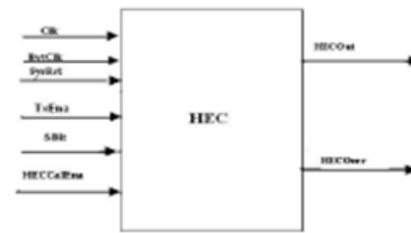


Fig 5: HEC Module

3) CRC Module:

Fig.6 shows CRC Module. The CRC is 32 bit field containing the 32-bit Cyclic Redundancy Check. When the TxEna signal is high, then the CRC data is given out and when the CRCCIena is high, then the CRC is calculated. CRCOver is high when the transmission of the data is over. This module helps in error free transmission of the data with proper reliability

V. VERILOG MODELING OF WI-FI MAC LAYER FOR TRANSMITTER:

There are two types of widely used hardware description languages i.e. Verilog HDL with C-language like syntax, easy to learn and another is VHDL which follows the structure of ADA programming language. Verilog and VHDL each have about 50% share of the commercial user base [8]. Due to high computational complexity of WLAN systems and the capabilities of state-of-the-art microprocessors, an implementation based solely in microprocessors would require a large number of components and would be cost inefficient FPGAs with their spatial / parallel computation style can significantly accelerate complex parts of WLANs and improve the efficiency of discrete components implementations[10]. The design has been synthesized using reference Spartan 3E FPGA. This device belongs to the spartan -E group of FPGAs from xilinx. FPGAs are reasonably cheap, with short design cycle and are reprogrammable. They are more flexible than PLDs and more compact than MSI/SSI. FPGAs have evolved to meet new application demands with features like i) Newer devices incorporate entire CPUs i.e. Xilinx,Spartan3E has 1-3programmable devices ii) Have carry chains to have a better support for multibit operations iii) Have

integrated memories, such as block RAMs in the devices we use iv) Have specialized units, such as Multipliers to implement functions that are Slow/inefficient in CLBs [Configurable Logic Blocks] [6] FPGA enables high performance due to the following factors i) Tailoring to desired bit-width (ii) Ease of applying varying sample rates (iii) Flexibility of parallel execution of basic functions due to uniform architectural resources [7]. Here, two modules of Wi-Fi MAC layer transmitter are chosen and synthesized and simulated on Spartan3E XC3S500E FPGA device.

VI. SIMULATION RESULTS & DISCUSSION:

The payload data storage and data processing blocks consists of a total of five different individual modules i.e FIFO, Data length counter modules and serializer, HEC, CRC modules respectively all these modules are synthesized and simulated using Xilinx XST and Xilinx ISE simulator. The simulation results are shown in following figures.

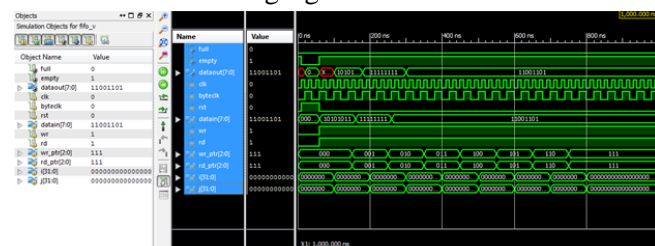


Fig.6. Simulation result of FIFO Module

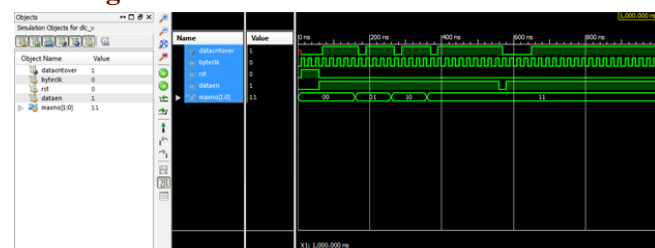


Fig.7. Simulation result of DLC Module

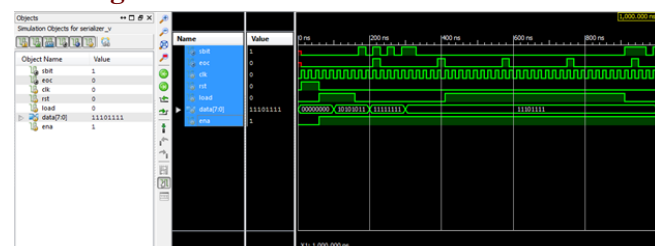


Fig.8. Simulation result of Serializer Module

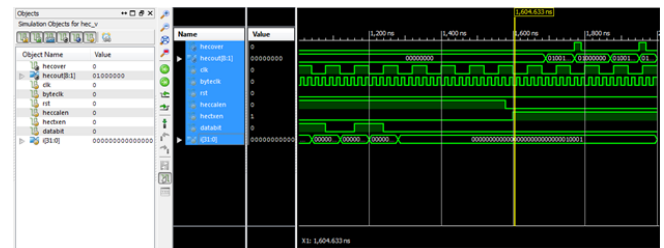


Fig.9. Simulation result of HEC Module

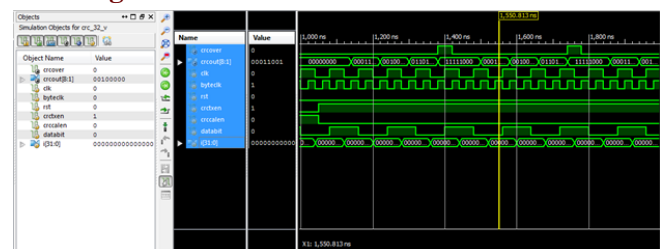


Fig.10. Simulation result of CRC Module

VII. CONCLUSIONS:

The design of Wi-Fi MAC layer for transmitter is modeled with Verilog HDL. Various individual modules of Wi-Fi Transmitter have been designed, verified functionally using Verilog HDL-simulator, synthesized by the synthesis tool. This design of the Wi-Fi transmitter is capable of transmitting the frame formats. The formats include all 802.11 frames i.e. MAC frame, RTS frame, CTS frame and ACK frame. The transmitter is also capable of generating errorchecking codes like HEC and CRC. It can handle variable data transfer.

REFERENCES:

- [1] A.M. BHAVIKATTI* Research Scholar, Dr.MGR University, Chennai." Vhdl Modeling of Wi-Fi MAC Layer for Transmitter".
- [2] W.L.Pang, K.W.Chew, F.Choong, E.S.Teoh, "Vhdl Modeling of the IEEE 802.11b DCF MAC", Proceedings of the 6th WSEAS International Conference on Instrumentation, Measurement Circuits and systems, Hangzhou, China, April 15 -17, 2007.
- [3] Broadband wireless Access, Institution of Engineering and Technology Seminar, 6th Dec 2006, London, UK

[4]Pabolo Brenner , "A Technical tutorial on the IEE802.11 Protocol"

[5]Shambhu Upadhyaya, " Wireless Network Security," Lecture 5, University at Buffalo, the State University of Newyork

[6]Sebastien Roy, " The Design of an FPGA Based MIMO Transceiver for Wi-Fi,"DSP Magazine, May 2006.

[7]Prof. David Brooks, "Computer Science 141 Computing Hardware", Fall 2007, Harvard University.

[8] Introduction to DSP Design flow, 2006 Xilinx, Inc

[9] Janak. H.Patel, Introduction to VHDL 1 and 2, Dept of Electrical and Computer Engineering, University of Illinois at urbana- campaign.

[10] Ahmed Abu-Hajar, Digital Design Using VHDL Digitavid, Inc, San Jose, CA.

[11] K.Masselos, N.S.Voros. "Implementation of of wireless Communications system on FPGA-Based platforms", EURASIP Journal on embedded systems, volume 2007, article ID 12192.

Author's Details:



M. Balaji

Is a M.Tech (VLSI & Embedded Systems) student in Department of Electronics and Communication Engineering from Siddhartha Institute of Engineering and Techno-logy, Ibrahimpatnam, Hyderabad. His interest of field in Embedded Systems and Networking.



Ashok Babu Amudapakula

Completed his B. Tech in ECE from Rao&Naidu Engineering College of Technology, ongole, affiliated to JNTU, Kakinada, A.P, India and M. Tech in DECS at QIS College of Engineering & Technology ongole, affiliated to JNTU, Kakinada, A.P, India. He is currently as an Assistant Professor in Electronics and Communication Engineering Department at Siddhartha Institute of Engineering and Technology, Ibrahimpatnam, Hyderabad. His area of interest are Digital VLSI Design & VLSI Image Processing.



Dr. D Subba Rao

Is a proficient Ph.D person in the research area of Image Processing from Vel-Tech University, Chennai along with initial degrees of Bachelor of Technology in Electronics and Communication Engineering (ECE) from Dr. S G I E T, Markapur and Master of Technology in Embedded Systems from SRM University, Chennai. He has 13 years of teaching experience and has published 12 Papers in International Journals, 2 Papers in National Journals and has been noted under 4 International Conferences. He has a fellowship of The Institution of Electronics and Telecommunication Engineers (IETE) along with a Life time membership of Indian Society for Technical Education (ISTE). He is currently bounded as an Associate Professor and is being chaired as Head of the Department for Electronics and Communication Engineering discipline at Siddhartha Institute of Engineering and Technology, Ibrahimpatnam, Hyderabad.