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VHDL Implementation of FPGA Based OFDM Modem for Wireless Applications

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Abstract:

The new mobile technologies trying to give broadband over wireless channel allowing the user to have bandwidth connectivity even inside moving vehicle. The metropolitan broadband wireless networks require a non-line-of-sight (NLOS) capability, and the scheme Orthogonal Frequency Division Multiplex (OFDM) becomes essential to overcome the effects of multipath fading. Orthogonal Frequency Division Multiplexing (OFDM) has become very popular, allowing high speed wireless communications. OFDM could be considered either a modulation or multiplexing technique and its hierarchy corresponds to the physical and medium access layer. A basic OFDM modulator system consists of a QAM or PSK modulator, a serial to parallel, and an IFFT module.

The iterative nature of the IFFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor.The VHDL implementation allows the design to be extended for either FPGA or ASIC implementation, which suits more for the Software Defined Radio (SDR) design methodology. In this project the OFDM modulator and demodulator will be implemented with full digital techniques. VHDL will be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. Modelsim Xilinx Edition will be used for functional simulation and verification of results. Xilinx ISE will be used for synthesis. The Xilinx's Chipscope tool will be used for verifying the results on Spartan 3E 3S500EFG320-4 FPGA.

Keywords:

OFDM Technology, FFT, IFFT, VHDL, FPGA design.

I.INTRODUCTION:

The telecommunications industry faces the problem of providing telephone services to rural areas, where the customer base is small, but the cost of installing a wired phone network is very high. One method of reducing the high infrastructure cost of a wired system is to use a fixed wireless radio network. The problem with this is that for rural and urban areas, large cell sizes are required to obtain sufficient coverage. This result in problems caused by large signal path loss and long delay times in multipath signal propagation. Currently Global System for Mobile Telecommunications (GSM) technology is being applied to fixed wireless phone systems in rural areas or Australia. However, GSM uses Time Division Multiple Access (TDMA), which has a high symbol rate leading to problems with multipath causing inter-symbol interference. Several techniques are under consideration for the next generation of digital phone systems, with the aim of improving cell capacity, multipath immunity, and flexibility. These include Code Division Multiple Access (CDMA) and Coded Orthogonal Frequency Division Multiplexing (COFDM). Both these techniques could be applied to providing a fixed wireless system for rural areas. However, each technique has different properties, making it more suited for specific applications. With CDMA systems, all users transmit in the same frequency band using specialized codes as a basis of channelization. The transmitted information is spread in bandwidth by multiplying it by a wide bandwidth pseudo random sequence. Both the base station and the mobile station know these random codes that are used to modulate the data sent, allowing it to descramble the received signal. OFDM allows many users to transmit in an allocated band, by subdividing the available bandwidth into many narrow bandwidth carriers. Each user is allocated several carriers in which to transmit their data.

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The transmission is generated in such a way that the carriers used are orthogonal to one another, thus allowing them to be packed together much closer than standard frequency division multiplexing (FDM).This leads to OFDM providing a high spectral efficiency. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, which are then allocated to users. However, OFDM uses the spectrum much more efficiently by spacing the channels much closer together. This is achieved by making all the carriers orthogonal to one another, preventing interference between the closely spaced carriers. With the rapid growth of digital communication in recent years, the need for high-speed data transmission has been increased.

The mobile telecommunications industry faces the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system has gained much attention for different reasons. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.Since OFDM is carried out in the digital domain, there are several methods to implement the system.

One of the methods to implement the system is using Field-Programmable Gate Array (FPGA).This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility.An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

II. FPGA BASED VLSI DESIGN:

Recent strides in programmable logic density, speed and hardware description languages (HDL's) have empowered the engineer with the ability to implement digital signal processing (DSP) functionality within programmable logic devices (PLDs or FPGAs). In this chapter the VLSI design methods on FPGAs using VHDL are discussed. The FPGA architectures basics are also discussed. The following section presents fundamentals of VHDL and synthesis issues related to it.

VHDL:

VHDL is a high level description language for system and circuit design. The language supports various levels of abstraction. In contrast to regular netlist formats that supports only structural description and a boolean entry system that supports only dataflow behavior, VHDL supports a wide range of description styles. These include structural descriptions, dataflow descriptions and behavioral descriptions. The structural and dataflow descriptions show a concurrent behavior. That is, all statements are executed concurrently, and the order of the statements is not relevant. On the other hand, behavioral descriptions are executed sequentially in processes, procedures and functions in VHDL. The behavioral descriptions resemble high-level programming languages. VHDL allows a mixture of various levels of design entry abstraction. Precision RTL Synthesis Synthesizes will accept all levels of abstraction, and minimize the amount of logic needed, resulting in a final netlist description in the technology of your choice. The Top-Down Design Flow is shown in Figure 1.

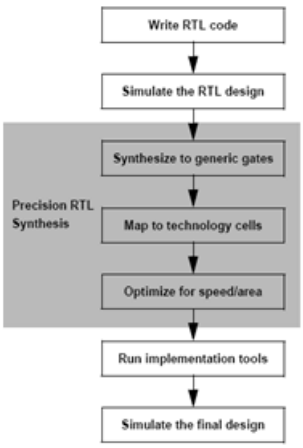

Figure 1: Top-Down Design Flow with Precision RTL Synthesis

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VHDL and Synthesis:

VHDL is fully simulatable, but not fully synthesizable. There are several VHDL constructs that do not have valid representation in a digital circuit. Other constructs do, in theory, have a representation in a digital circuit, but cannot be reproduced with guaranteed accuracy. Delay time modeling in VHDL is an example. State-of-the-art synthesis algorithms can optimize Register Transfer Level (RTL) circuit descriptions and target a specific technology. Scheduling and allocation algorithms, which perform circuit optimization at a very high and abstract level, are not yet robust enough for general circuit applications. Therefore, the result of synthesizing a VHDL description depends on the style of VHDL that is used.

III.DESIGN OF OFDM MODEM:

The OFDM SDR which consists of shows the configuration for a basic OFDM transmitter and receiver.

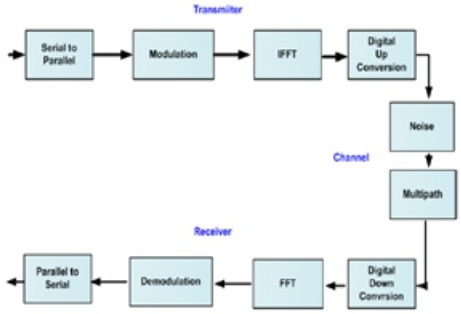

Figure 2: Block Diagram of Ofdm modem

The OFDM transmitter which consists of
1. Clock Distributor
2. Input data sampler
3. Symbol Mapper
4. Modulation
5. Serial to Parallel
6. IFFT

The OFDM receiver which consists of
1. Clock Distributor
2. FFT
3. Parallel to Serial
4. Demodulation
5. IQ extractor
6. Symbol demapper
7. Output Data

The signal generated is at base-band and so to generate an RF signal the signal must be filtered and mixed to the desired transmission frequency. To generate OFDM successfully the relationship between all the carriers must be carefully controlled to maintain the Orthogonality of the carriers. For this reason, OFDM is generated by firstly choosing the spectrum required, based on the input data, and modulation scheme used. Each carrier to be produced is assigned some data to transmit. The required amplitude and phase of the carrier is then calculated based on the modulation scheme (typically differential BPSK, QPSK, or QAM). The required spectrum is then converted back to its time domain signal using an Inverse Fourier Transform. In most applications, an Inverse Fast Fourier Transform (IFFT) is used. The IFFT performs the transformation very efficiently, and provides a simple way of ensuring the carrier signals produced are orthogonal.

The Fast Fourier Transform (FFT) transforms a cyclic time domain signal into its equivalent frequency spectrum. This is done by finding the equivalent waveform, generated by a sum of orthogonal sinusoidal components. The amplitude and phase of the sinusoidal components represent the frequency spectrum of the time domain signal. The IFFT performs the reverse process, transforming a spectrum (amplitude and phase of each component) into a time domain signal. An IFFT converts a number of complex data points, of length that is a power of 2, into the time domain signal of the same number of points. Each data point in frequency spectrum used for an FFT or IFFT is called a bin. The orthogonal carriers required for the OFDM signal can be easily generated by setting the amplitude and phase of each frequency bin, then performing the IFFT. Since each bin of an IFFT corresponds to the amplitude and phase of a set of orthogonal sinusoids, the reverse process guarantees that the carriers generated are orthogonal.

Design of Ofdm_tx

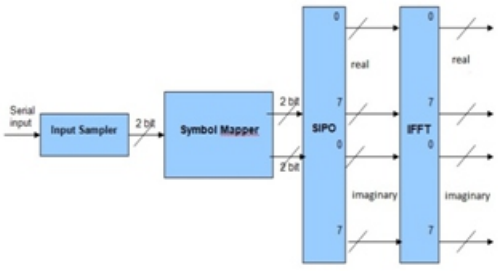

Figure 3: Block Diagram Ofdm_tx

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Input Sampler IQ Gen:

This block samples the serial input and generates 2 bit IQ output.

Symbol Mapper:

This block maps the input I, Q to the corresponding to the real part and imaginary part of the constellation symbols.

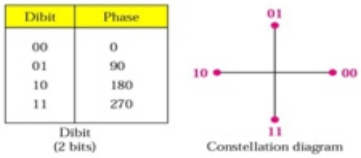

Figure 4: Constellation Diagram

SIPO:

This block converts the serial input to the parallel output. This block is used in OFDM TX, to convert serial input to parallel output. This block's output is given to the input of IFFT.

Design of Ofdm_rx

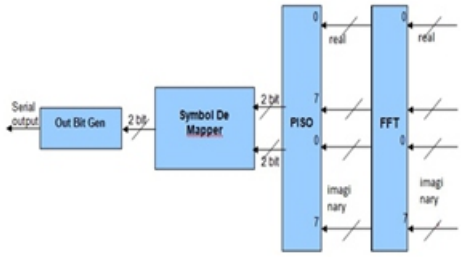

Figure 5: Block diagram of Ofdm_rx

PISO:

This block converts the parallel input to the serial output. This block is used in OFDM RX, to convert parallel input to serial output. This block's output is given to the Symbol_ de_mapper.

Symbol_de_mapper:

This block maps, the Real and imaginary parts of the serial out from PISO, to the IQ corresponding to the real part and imaginary part of the constellation symbols. It extracts the IQ values from the serial out of PISO.

Out_bit_gen:

This block takes 2 bit IQ s from Symbol_de_mapper and generates output bits.

Clk distr:

This is the clock distributer block, which generates two enable signals en_div_2 and en_div_16.
en_div_2 is divided by 2 of input clock.
en_div_16 divided by 16 of input clock.

IV.RESULTS AND DISCUSSIONS:

The following chapter consists of all the Software and Hardware results observed in the project. The Results include snapshots of Top module with the inputs, outputs and intermediate Waveforms.

Top ofdm_tx_and_rx:

Figure 6: Simulation Result of Top ofdm_tx_rx.

OFDM TX:

It consists of all the above sub blocks as components. The simulation result of above module is shown below.

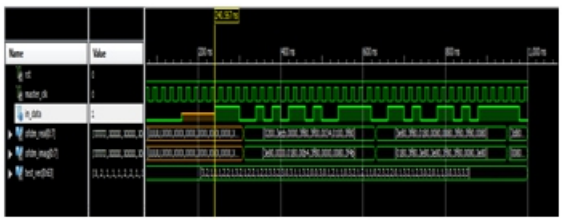

Figure 7: Simulation Result of Top Ofdm_tx

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OFDM_RX:

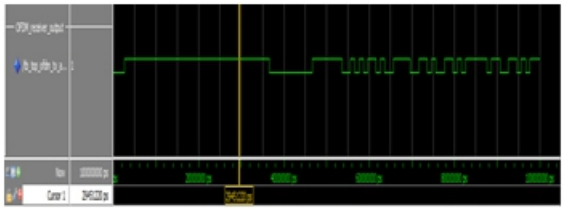

Figure 8: Simulation Result of Top Ofdm_rx

Chipscope result:

Chipscope is an embedded, software based logic analyzer. By inserting an "integrated Controller core" (icon) and "integrated logic analyzer" (ila) into your design and connecting them properly, you can monitor any or all of the signals in your design. Chipscope provides you with a convenient software based interface for controlling the "integrated logic analyzer," including setting the triggering options and viewing the waveforms. Users can place the ICON, ILA, VIO, and ATC2 cores (collectively called the Chipscope Pro cores) into their design by generating the cores with the Core Generator and instantiating them into the HDL source code. We can also insert the ICON, ILA, and ATC2 cores directly into the synthesized design net list using the Core Inserter tool. The design is then placed and routed using the ISE 9.2i implementation tools. Next, we download the bit stream into the device under test and analyze the design with the Analyzer software. The tools design flow merges easily with any standard FPGA design flow that uses a standard HDL synthesis tool and the ISE 9.2i implementation tools. Chipscope pro analyzer we are using here.

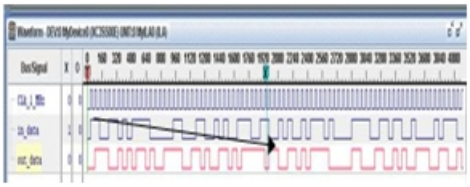

Figure 9: Chipscope Result of Top Ofdm_tx_rx

V.CONCLUSION:

In this paper, OFDM MODEM has been studied and implemented for Modulator and Demodulator and Its applications have been extended from high frequency radio communications to telephone networks, digital audio broadcasting and terrestrial broadcasting of digital television.

The advantages of OFDM, especially in the multipath propagation, interference and fading environment, make the technology a promising alternative in digital communications including mobile multimedia. Therefore this design can be applied to real-time signal processing system, which completes the main computing modules in the OFDM for multi services. The capability of designing and implementing an OFDM MODEM is presented in this work, the design considered using a pure VHDL with the aid of IPs to implement the IFFT and clock Synthesis Function, from the Mapping results the design can be easily fit into Xilinx FPGA XC3S500E.

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