ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Novel Design of Balanced Quaternary Reversible Logic Circuits Using Verilog HDL

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Abstract:
Routing has become the main contributor in many areas of design such as area, delay and power. Multiple Valued Logic (MVL) offers a means to reduce the routing since each wire in MVL can carry the twice as much information as single binary wire. Reducing this routing directly leads to the reduction of overall circuit area and power consumption. Multi–valued ternary logic under GF (3) and quaternary logic under GF (4) are available in the literature, but circuit design based on these logic systems is very few. As traditional computing devices based on irreversible logic are approaching their limit in terms of heat dissipation, power and speed requirement. Reversible computing is emerging as an alternative technology. Usage of multi–valued logic for irreversible computing is also growing.

Ternary and quaternary logic based reversible gate have been proposed recently. Ternary logic based design has further been enhanced using balanced logic levels. But, the same is not available for quaternary logic. In this paper, we propose balanced quaternary logic and synthesis approach, which offers significant advantages in logic design. Small circuits like adders and Multipliers have been designed based on that approach. We feel that balanced logic based approach will open a new era in multivalued logic design.

Keywords:
Balanced quaternary logic, reversible logic gate, m-s gate, half-adder, full-adder, multiplier.

I. INTRODUCTION:

For many years digital devices have been designed using binary logic.

Even today also, the latest computing systems are designed and developed using binary logic only. Then why there is a need of inventing multi valued logic over binary logic??? With the advancing technology, interconnections are the main contributor for delay, area and power consumption. One of the solution for the problem of interconnection is that: what if we will develop the idea of transmitting the number of logic levels through a single wire. Since, multi valued logic scheme allows more data to be grouped in single digit, researchers seems the use of multivalued logic as a solution for the above problem.so, researchers have been working on the idea of using multivalued logic for many years. Existing VLSI technology has put some limitations on the selection of number of logic states, therefore researchers seems the use of Quaternary logic systems to be best in this regards.

In literature, the multivalued ternary (in 3-demensional Hilbert space under GF (3)) [1], quaternary (GF (4)) [2] logics have been discussed by the researchers. To realize the ternary logic circuit three digits (trit) 0, 1 and 2 are used with balanced ternary logic states -1, 0 and 1 [3]. Circuit balancing is necessary for realizing the ternary reversible logic and above. This paper introduces the balancing rules and their implementation mechanism for quaternary reversible logic gates. Quaternary logic circuits realize 4-digits 0, 1, 2 and 3 (quaternary standard states) [2]. The balanced quaternary is a non-standard number system which is useful for comparison with quaternary numbers. In a quaternary system, the balanced quaternary logic contains 4-states -2, -1, +1 and +2. For more precise representation, some conventions are also assumed for balanced quaternary logic states. -2 and -1 states are represented as low state (L) and high

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state (H), respectively. +1 and +2 states are the inverse states of H and L, respectively. All integers can be represented by the balanced quaternary. Any unbalanced quaternary can be converted into balanced quaternary notation by subtracting +2 and +1 from 0, 1 and 2, 3, respectively. For example, $(2301)_{unbal.4} = (12LH)_{bal.4} = (177)_{10}$. From the balancing rules of quaternary reversible logic, the realization of balanced quaternary reversible half-adder, full-adder and multiplier is also proposed in this paper. To the best of our knowledge, it is the first attempt for balanced quaternary circuit realization.

The next sections of this paper are arranged as follows: The basics of quaternary algebra are described in section II. Quaternary reversible logic gates and their literature survey are addressed in section III. Section IV has our proposed balanced quaternary operation rules on balanced quaternary reversible gates. Section V has the design of balanced quaternary reversible circuits, half-adder, full-adder and multiplier. The synthesis and simulation results are presented in section VI, The conclusion of the paper and future work is discussed in section VII.

II. THE BASICS OF QUATERNARY ALGEBRA

The set Q_{gf} has the elements (0, 1, 2 and 3) exhibits an algebraic structure of quaternary Galois Field (GF (4)). The two binary operations addition and multiplication are defined in Table1 (a) and Table1 (b)
TABLE I (A)GF(4) ADDITION; (B)GF(4) MULTIPLICATION

(a)

+	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

(b)

.	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

(A1) a + (b + c) = (a + b) + c (associative law for addition)
(A2) a + b = b + a (commutative law for addition)
(A3) There is an element 0 such that a + 0 = a for all a
(A4) For any a, there is an element (−a) as a + (−a) = 0
(M1) a ·(b·c) =(a·b) · c (associative law for multiplication)
(M2) a · b = b ·a (commutative law for multiplication)
(M3) There is an element 1 (not equal to 0) such that a · 1 = a for all a
(M4) For any $a \neq 0$, there is an element a^{-1} as $a \cdot a^{-1} = 1$
(D) a· (b + c) = (a · b) + (a · c) (distributive law)

III. QUATERNARY REVERSIBLE LOGIC GATES AND LITERATURE SURVEY

Before describing the quaternary reversible gates a close look on reversible logic gate is necessary.

A. Reversible Logic Gate:

The permutation of a gate computes a bijective function then a gate is a reversible. There must be exist a one-one and onto correspondence between its inputs and outputs. The logic values 0 and 1 are computed in binary reversible gates whereas logic values 0, 1, 2 and 3 are accepted inquaternary reversible gates. The famous reversible gates are NOT gate Feynman gate (CNOT gate) [4], Toffoligate(C^2 NOT gate) [5] and Fredkin gate [6]. The representation of these gates is described in Fig.1 (a) – (d).

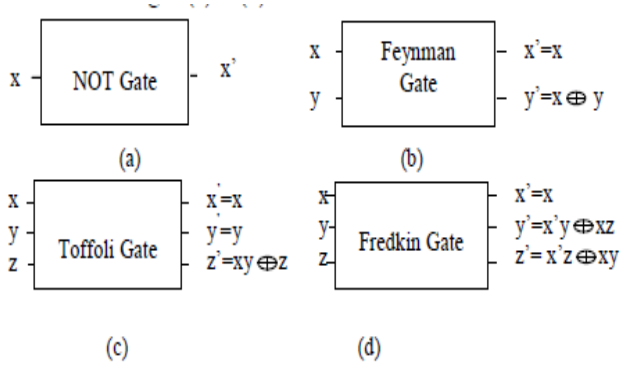

Fig. 1. Reversible Gates (a) NOT Gate (b) Feynman Gate (c) Toffoli

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The NOT gate invert its input to the output. In Feynman gate the 1st input is unchanged, and the state of the 2ndinput is inverted when the 1st input is 1. Same in Toffoli gate, first two inputs unchanged their states and the 3rdinput is inverted when both inputs are 1. In Fredkin gate the 1stinput is unchanged, and 2nd and 3rd inputs are interchanged when the first input is 1. Quaternary reversible gates are NOT gate, Shift gates, Feynman gate, Toffoli gate and Muthukrishnan–Stroud Gate (M-S gate) [7] etc. There are 24 (4!) shift g ates in quaternary reversible logic, but these are more, so here we show only four quaternary reversible shift gates with their symbols.

Gate Name	Gate Symbol	Logic State			
		0	1	2	3
Buffer	x — x	0	1	2	3
Single-shift	x — +1 — x+1	1	0	3	2
Dual-shift	x — +2 — x+2	2	3	0	1
Tri-shift	x — +3 — x+3	3	2	1	0

Fig. 2. Shift Gates

Here addition (+) and multiplication (x or denoted by dot/absent mark) operations are followed over modulo 4 or GF (4). These all 24 shift gates are 1-qudit g ates. These gates are represented by the following Fig. 2 and its simple symbolic representation is shown in Fig. 3.

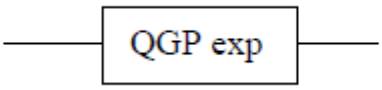

Fig. 3. Representation of quaternary reversible 1-qudit gate

B. Quaternary 2-qudit Muthukrishnan-Stroud Gate family:

The liquid ion trap technologies [8] are used to realize the 2-qudit multi- valued logic m uthukrishnan-stroud gate. It is shown but not tested in the laboratory.

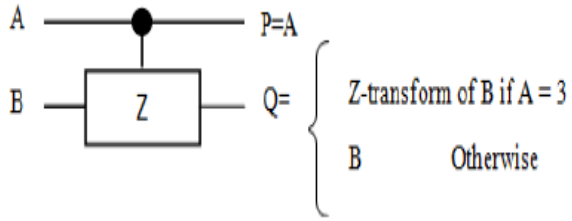

Fig. 4. Quaternary Muthukrishnan–Stroud Gate

Here Z-transform is the process of translating the controlled-input, when the controlling–input is 3. The above Fig. 4 shows the family of M-S gate.

TABLE II TRUTH TABLE OF QUATERNARY MUTHUKRISHNAN- STROUD GATE

Input		Output	
A	*B*	*P*	*Q*
0	0	0	0
0	1	0	1
0	2	0	2
0	3	0	3
1	0	1	0
1	1	1	1
1	2	1	2
1	3	1	3
2	0	2	0
2	1	2	1
2	2	2	2
2	3	2	3
3	0	3	0
3	1	3	2
3	2	3	3
3	3	3	1

Fig. 5 and Fig. 6 show the symbols of standard quaternary logic gates quaternary Feynman gate.Realization of quaternary reversible circuits is more complex to reversible binary circuits. Recently, researchers have addressed a very few but promising research articles on realization and implementation of quaternary reversible circuits. In 2006, Mozammel H. A. Khan [9] proposed a successful implementation of quaternary Feynman and Toffoli gate. The realization of quaternar y Feynman and Toffoli gate is shown using M-S primitive gate.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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Md. Mahmud Muntakim Khan et al. [10] addressed an optimized realization of quaternary Toffoli gate in 2007. The quaternary realization of modified Fredkin gate, 4 □ 1 MUX, 1 □ 4 DEMUX and 16 □ 2 encoder are also addressed in this artic le [11]. In 2008, Mozammel H. A. Khan [12] proposed an improved (from previous work) realization of quaternary Toffoli gate using quaternary control shift gates.

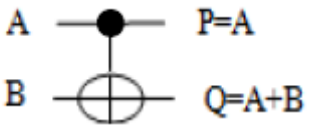

Fig. 5. Standard Quaternary Feynman Gate

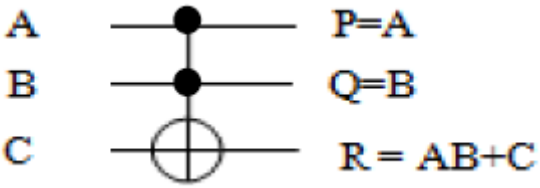

Fig. 6. Quaternary Toffoli Gate

Thus, from a careful survey of existing literature on quaternary reversible circuits, it can be sum marized that the realization of all basic reversible gates and r eversible circuits (half-adder, full-adder and multiplier) are proposed using M-S primitive gate. It is observed in previous proposed quaternary circuits that the shift gate c ounts and M-S primitive gates are too high. Hence, the hard ware complexity of these circuits will also be high.

In this article, our goal is to reduc e the hardware complexity of the circuits using balanced quaternary reversible logic. To the best of our knowledge no significant effort has been found on the realization of balanced quaternary reversible circuits. The balanced quaternary logic can represent both positive and negative numbers without complement operation.

TABLE III UNITARY MATRIX OF FEYNMAN GATE

INPUT \ OUTPUT	00	01	10	11
00	1	0	0	0
01	0	1	0	0
10	0	0	0	1
11	0	0	1	0

C. Unitary Matrix

Unitary Matrix (U) is an n*n matrix which have the same number of rows & columns. Here the row and column means the input and output. The conjugate transpose of unitary matrix is U* and UU* = U*U = I, here I is the identity matrix. The Input Output relationship of the reversible gate / circuit is the unitary matrix of that gate. For example, the unitary matrix of Feynman gate is shown in table III.

IV.BALANCED QUATERNARY REVERSIBLE LOGIC GATES

For the design of quaternary balanced reversible gates four states -2, -1, +1 and +2 are used for corresponds to 0, 1, 2 and 3. The unique column vector representations of these states are represented by Fig. 7.

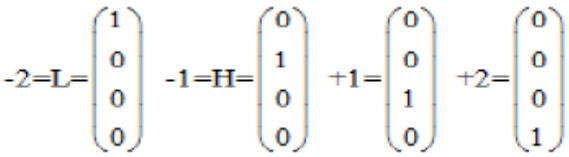

Fig. 7. Vector Representation of Balanced Quaternary States

A. BALANCED QUATERNARY NOT GATE

It inverts the input to th e corresponding output of the input, e.g. -2 inverts into +2 and -1 inverts into +1. Fig. 8 shows the symbol of balanced quaternary reversible NOT gate with its Truth Table.

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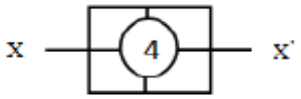
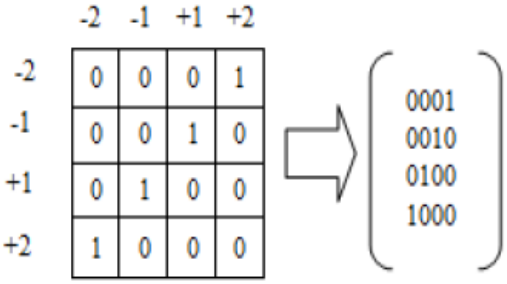


Fig. 8. Symbol of Balanced Quaternary NOT Gate

TABLE IV TRUTH TABLE OF BALANCED QUATERNARY NOT GATE

Input	Output
A	A'
+2	-2
+1	-1
-1	+1
-2	+2

The unitary matrix of the balanced quaternary reversible NOT gate is as-



The fig. 10 shows the balanced quaternary NOT operation e.g. Input -2 produce +2.

$$\begin{pmatrix}0001\\0010\\0100\\1000\end{pmatrix} \times \begin{pmatrix}1\\0\\0\\0\end{pmatrix} = \begin{pmatrix}0\\0\\0\\1\end{pmatrix}$$

Fig.10. Balanced Quaternary NOT Operation

B. BALANCED QUATERNARY FEYNMAN GATE

It is a 2*2 reversible logic gate. The 1st input is unchanged for the 1st output and the 2nd input is changed by the balanced quaternary NOT gate. It is not dependent on the 1st input. Table V and VI shows the operation and Truth Table of balanced quaternary Feynman gate.

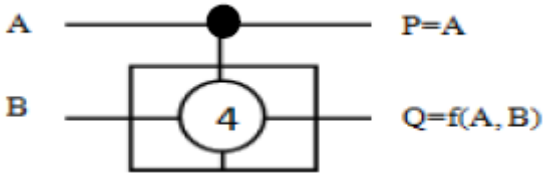


Fig. 11. Symbol of Balanced Quaternary Feynman Gate

TABLE V. BALANCED QUATERNARY FEYN MAN OPERATION

Control Input	Target Output
-2	NOT of Input
-1	
+1	
+2	

TABLE VI. TRUTH TABLE OF BALANCED Q UATERNARY FEYNMAN GATE

Input		Output	
A (Control)	B	$A' = A$	$[B' = f(A,B)]$
-2	-2	-2	+2
-2	-1	-2	+1
-2	+1	-2	-1
-2	+2	-2	-2
-1	-2	-1	+2
-1	-1	-1	+1
-1	+1	-1	-1
-1	+2	-1	-2
+1	-2	+1	+2
+1	-1	+1	+1
+1	+1	+1	-1
+1	+2	+1	-2
+2	-2	+2	+2
+2	-1	+2	+1
+2	+1	+2	-1
+2	+2	+2	-2

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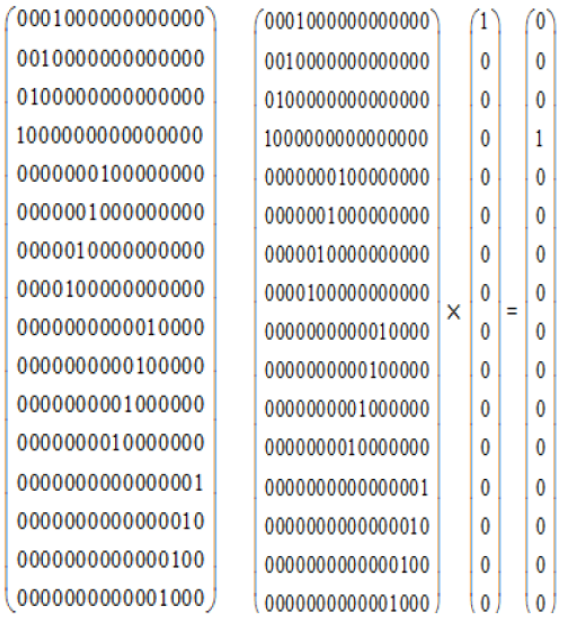

Fig.12. Unitary Matrix of Balanced Quaternary Feynman Gate Fig. 13. Balanced Quaternary Feynman Operation

Fig. 11, 12 and 14 shows the symbol, unitary matrix and column vector representat ion of balanced quaternary Feynman gate. Fig. 13 shows the Feynman operation when the Input -2-2 converted into -2+2 Output.

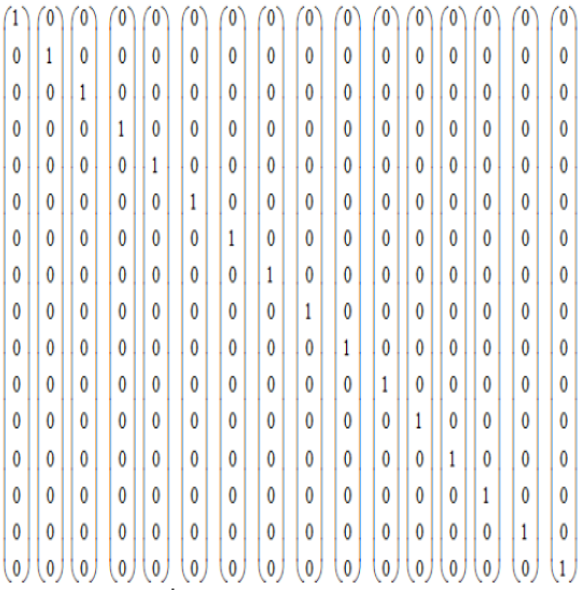

Fig. 14. Column Vector representation of -2-2,-2-1,-2+1,-2+2,-1-2,-1-1,-1+1,-1+2,+1-2,+1-,+1+1,+1+2,+2-2,+2-1,+2+1,+2+2

C.BALANCED QUATERNAR Y TOFFOLI GATE

It is a 3*3 reversible logic gate. The 1st and 2nd inputs are unchanged, and the 3rd in put changed by the balanced quaternary NOT operation o n the 3 rd input to convert 3rd output. It is also not dependant on the 1st and 2nd input which can have any quaternary b alanced states. The balanced quaternary Toffoli operations are shown by the table VII.

TABLE VII. BALANCED QUATER NARY TOFFOLI GATE OPERATION

Control Input		Output (Target)
A	*B*	
Any	Any	NOT of the input

Fig. 15 shows the symbol of balanced quaternary Toffoli gate, which is newly proposed, without Truth Table (table must be too large, so here we are not showing its truth table).

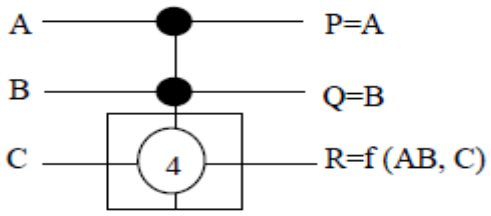

Fig. 15. Symbol of Balanced Quaternary Toffoli Gate

V. BALANCED QUATERNARY REVERSIBLE CIRCUITQUATERNARY HALF-ADDER:

An n*n balanced reversible logic circuit is designed by the use of the balanced reversible logic gate. Here we are designing some balanced quaternary reversible logic circuit by the help of the balanced quaternary reversible logic gates. The designing of balanced quaternary reversible half adder, full adder and multiplier circuits are designed here by the specific rules of circuits.

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A. BALANCED QUATERNARY REVERSIBLE ADDE R

In balanced quaternary logic, the states -2, -1, +1 and +2 are represented by the --, -, + and ++, respectively. By these conventional, the addition table is shown following.

TABLE VIII. BALANCED QUATERNARY ADDITIONTABLE

+	--	-	+	++
--	--|--	--|-	--|+	--|++
-	--|-	--|+	--|+	-|--
+	--|+	--|++	-|--	-|-
++	--|++	-|--	-|-	-|+

B. DESIGNING OF BALANCED QUATERNARY HALFADDER

It is a 2*2 reversible logic circuit, where the inputs are simple A and B, and the outputs are sum an d carry. There are some rules to find the sum and carry for the balanced quaternary reversible circuit.

Step1. Changed the both balanced quaternary input number into its standard quaternary.
Step2. Add them.
Step3. If the addition is less than or equal to 3, then the number has the Carry 0 and Sum the addition of standard state, and these are converted into balanced states.
Step4. If addition is more than 3, then number is changed into standard quaternary, the LSD is the sum and the MSD is the carry, and these standard states are converted into corresponding balanced states.

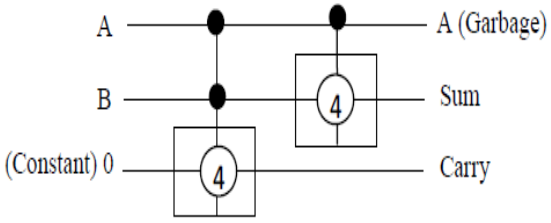

Fig. 16. Symbol of Balanced Quaternary Half Adder

Fig. 16 and table IX show the symbol and truth table of balanced quaternary half adder. The function of reversibility is not followed, so an extra ancilla line 0(constant line) is added to make it reversible and it generates two basic outputs (sum, carry) with a garbage output.

TABLE IX. TRUTH TABLE OF BA LANCED

Input		Output	
A	B	Carry	Sum
--	--	--	--
--	-	--	-
--	+	--	+
--	++	--	++
-	--	--	-
-	-	--	+
-	+	--	++
-	++	-	--
+	--	--	+
+	-	--	++
+	+	-	--
+	++	-	-
++	--	--	++
++	-	-	--
++	+	-	-
++	++	-	+

C.DESIGNING OF BALANCED Q UATERNARY FULL ADDER

It is 3x3 reversible logic gate it has 4^3(64) combinations of the states and the truth table must be larger, so here we show only balanced quaternary reversible full adder circuit, not the truth table of the circuit. It has two inputs with one $carry_{in}$ input and one 0 (constant) input to make reversible, It produces two garbage outputs A and B, and Sum and $Carry_{out}$.

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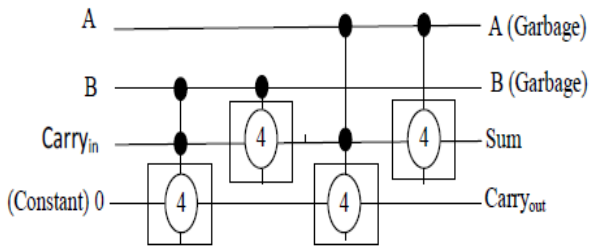

Fig. 17 Symbol of balanced quaternary full adder

The figure shows that it is designed by the two balanced quaternary half adders, means it is the double of the balanced quaternary reversible half adder. It has the two balanced quaternary Toffoli gate and two balanced quaternary Feynman gate.

D. BALANCED QUATERNARY REVERSIBLE LOGIC MULTIPLIER

The balanced quaternary logic multiplication table is shown in table X.

The multiplication table has some rules-

Step1. Firstly, change the balanced quaternary numbers into standard quaternary numbers.
Step2. And multiply with each other, and find, if number is in standard quaternary then it changed in balanced quaternary else the digits multiplied with each other and then find standard quaternary.
Step3. This process is followed when the result is not finding in a standard quaternary.
Step4. Finally, the standard quaternary number is changed in balanced quaternary number, which shows the multiplier of the balanced states.

TABLE X. BALANCED QUATERNARY MULTIPLICATIONO PERATION

x	--	-	+	++
--	--	--	--	--
-	--	-	+	++
+	--	+	--	+
++	--	++	+	+

E. DESIGNING OF REVERSIBLE LOGIC MULTIPL IER

It is a 3*3 reversible logic multiplier circuit. The symbol and Truth table of the quaternary multiplier is shown in Fig18 and Table XI.

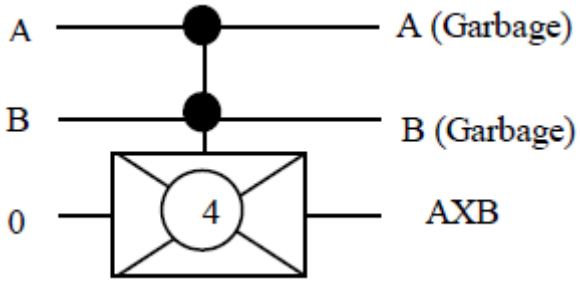

Fig. 18. Symbol of balanced quaternary multiplier

TABLE XI. TRUTH TABLE OF BALANCED QUATERNARY MULTIPLIER

Input A	Input B	Output (AxB)
--	--	--
--	-	--
--	+	--
--	++	--
-	--	--
-	-	-
-	+	+
-	++	++
+	--	--
+	-	+
+	+	--
+	++	+
++	--	--
++	-	++
++	+	+
++	++	+

VI.SIMULATION RESULTS

The corresponding simulation results of the floating point Balanced Quaternary Reversible Logic Multiplierare shown below. All the synthesis and simulation results are performed using VHDL.

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The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

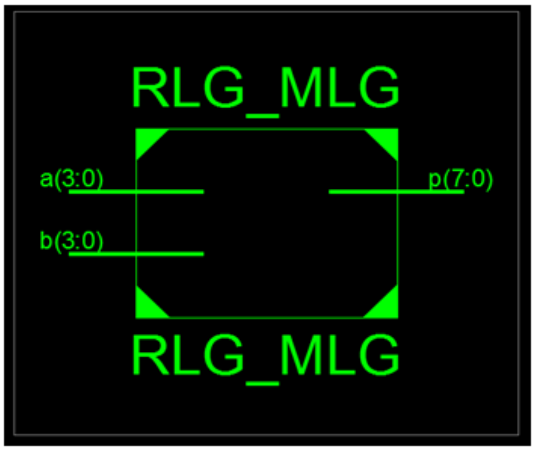

Figure-19.a RTL schematic of Top-level of Balanced Quaternary Reversible Logic Multiplier

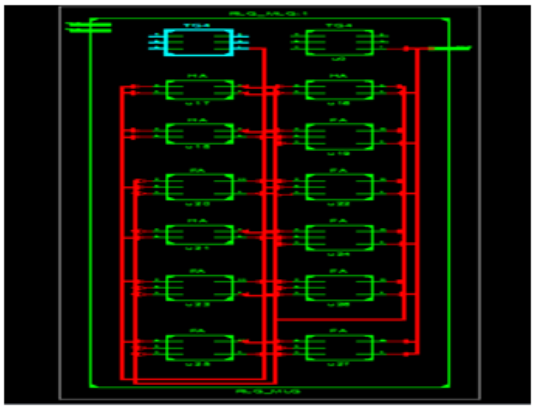

Figure-19.b: RTL schematic of Internal block of Balanced Quaternary Reversible Logic Multiplier

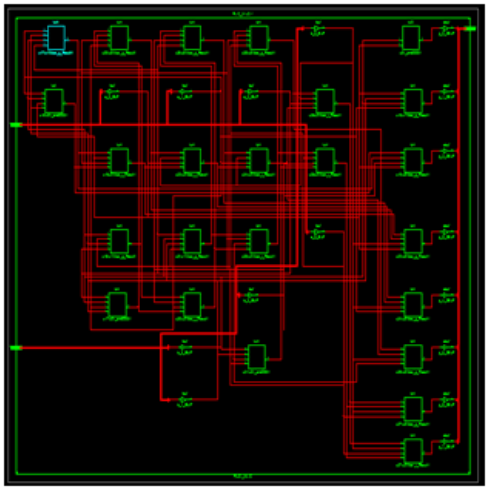

Figure-19.c: Technology schematic of Balanced Quaternary Reversible Logic Multiplier

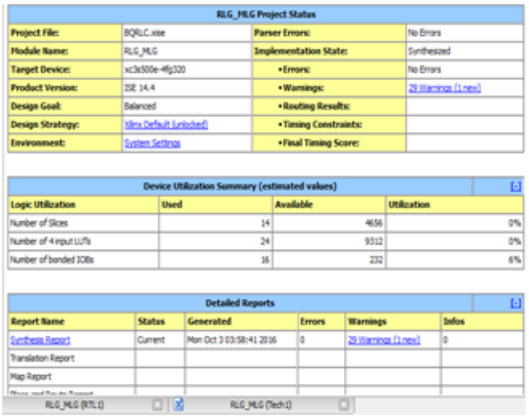

Figure-19.d: Synthesis report of Balanced Quaternary Reversible Logic Multiplier

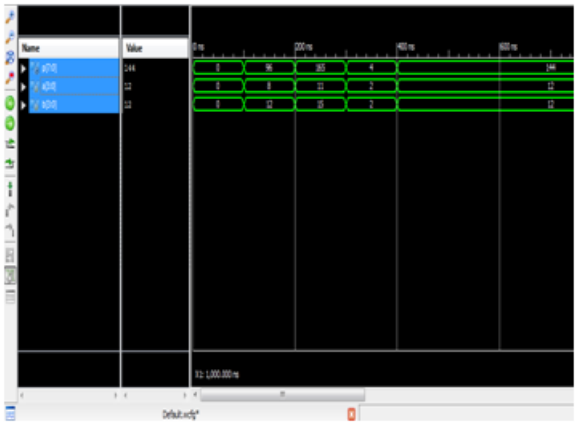

Figure-19.e: simulated outputs for Balanced Quaternary Reversible Logic Multiplier

VII. CONCLUSION AND FUTURE SCOPE

Due to efficient realization of balanced quaternary reversible logic there would be a very high prospect to generate quaternary reversible logic synthesis. In this article, a significant realization of balanced quaternary reversible gates, circuits is proposed which will promote a standard balancing in reversible com puting. We have proposed a methodology and balancing principles for the realization of balanced quaternary reversible gates, circuits. It significantly optimizes the hardware complexity of our proposed design of balanced quaternary reversible half-adder, full-adder and multiplier. The future work of the quaternary reversible logics is to realize a synthesis of reversible logic circuits. The fault tolerance can also be proposed in future based on this approach.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

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