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Design of All-Optical Reversible Logic Circuits Using Novel Optical Reversible Gates

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Abstract:
The advancement in the field of nanometer innovation prompts minimize the force utilization of rationale circuits. Reversible rationale outline has been one of the promising advances increasing more prominent enthusiasm because of less dispersal of warmth and low power utilization. As of late, in the writing, reversible rationale doors and combinational circuits have been proposed in optical space utilizing Semiconductor Optical Amplifier (SOA) based Mach Zehnder interferometer (MZI) changes because of its huge points of interest, for example, rapid, low power, quick exchanging and simplicity of manufacture.

Optical reversible plans have utilized impromptu methodologies and require high cost as far as MZI switches, Beam Splitters (BS), and Beam Combiners (BC) and additionally optical deferral. In this work, an optical reversible MNOT entryway and all-optical acknowledgment of 4×4 Toffoli Gate have been proposed which is utilized as a part of all-optical acknowledgment of enhanced reversible combinational circuits.

A general configuration way to deal with understands all-optical reversible circuits in light of MZI switches have been proposed first time in the writing. Enhanced all-optical reversible 2×1 multiplexer and full snake circuits have been composed utilizing these proposed entryways and outline approach. All-optical reversible outlines of 4×1 multiplexer, 1×4 Demultiplexer and 3to8 Decoder circuits have additionally been introduced in this work first time in the writing. Our outcomes have indicated noteworthy upgrades over existing plans as far as MZI switches, BS, BC and optical postponement.

Keywords:
Optical Reversible computing; Mach-Zehnder Interferometer (MZI); Full Adder; Multiplexer; Decoder; optical cost.

I. INTRODUCTION:

The developing advancements have expanded the interest of elite figuring. As per G. Moore's low [1], number of transistor checks to be incorporated per unit zone in gadgets will twofold in one and half year. To accomplish fast calculation, high bundling thickness in the rationale circuits is required which brings about more warmth dispersal. The routine figuring is discovered not able to manage low power, high compaction and warmth dissemination issues of the present processing environment. In 1961, R. Laundaur [2] expressed that warmth scattering happens because of vitality misfortune in irreversible rationales.

Every piece of data disseminates a measure of vitality equivalent to KTln2 joules where K is Boltzmann's Constant and T is the supreme temperature. In 1973, C. H. Bannett [3] expressed that reversible rationale can defeat the warmth dissemination issue of VLSI circuits on the grounds that the bits of data are not eradicated in reversible processing. New innovations are developing to manage these issues. Reversible Computing is one approach to defeat the issue of warmth scattering in registering chips which thus help in expanding the bundling thickness.

Reversible Logic is by all accounts cheerful because of its wide application in developing advances, for example, quantum registering, optical figuring and power effective nanotechnologies and so forth. Reversible circuits don't lose data.

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A reversible rationale entryway has coordinated mapping amongst information and yield vectors i.e. number of info lines are equivalent to number of yield lines in the reversible entryway [12], [14]. Fan-out is not allowed in the reversible logic. Constant sources of info and junk yield line can be added to the circuit to make it reversible [12], [13], [14]. Optical Computing is calculation with photon rather than traditional electron based calculation. Unmatched fast and zero mass of photon have pulled in the scientists towards the optical acknowledgment of reversible rationale entryways utilizing Semiconductor Optical Amplifier (SOA) based Mach Zehnder Interferometer (MZI) switches.

MZI Switches are favored due to its rapid, quick exchanging; low power and straightforwardness in manufacture [4], [5], [6]. The creators have introduced the optical acknowledgment of famous reversible rationale doors, for example, Feynman and Toffoli Gates [4], Fredkin Gate [5], and Peres Gate [6] and so forth. All-optical reversible combinational circuits for occasion 2×1 Multiplexer [7], Binary Ripple Carry Adder [8], NOR Gate [9], New Gate [10], Hybrid New Gate (HNG) [11] and Modified Fredkin Gate [15] and so forth are proposed by the creators in the writing.

In this paper, we have proposed an optical reversible MNOT door utilizing one MZI switch. All-optical acknowledgment of 4×4 Toffoli Gate has been displayed which is utilized as a part of alloptical acknowledgment of upgraded reversible combinational circuits. A general outline way to deal with understands all-optical reversible circuits in view of MZI switches have been proposed first time in the writing. Advanced all-optical reversible 2×1 multiplexer and full viper circuits have been outlined utilizing these proposed doors and configuration approach. All-optical reversible outlines of 4×1 multiplexer, 1×4 D e-multiplexer and 3to8 Decoder circuits have additionally been presented in this work first time in the writing.

Our outcomes have demonstrated noteworthy enhancements over existing plans as far as MZI switches, BS, BC and optical deferral.

II.BASICS OF ALL OPTICAL REVERS IBLE LOGIC

Reversible rationales are actualized with optical innovation utilizing some building squares, for example, MZI based optical switch, shaft splitter and pillar combiner.

A. SOA Based MZI Switch

A SOA based MZI switch can be outlined utilizing two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C - 1, C-2) [8], [9]. In a MZI switch, there are two sources of info ports An and B, and two yield ports called bar port and cross port, separately, as appeared in Figure 1 and 2.

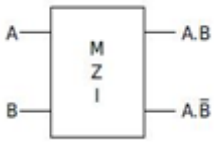

Fig.1. Block diagram of Mach-Zehnder Interferometer switch [8]

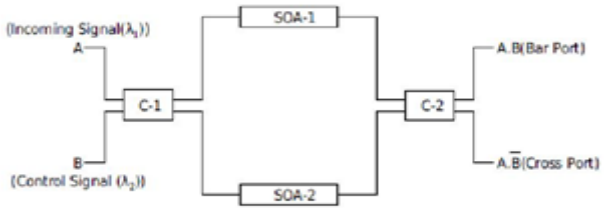

Fig.2.SOA based Mach-Zehnder Interferometer switch [8]

The optical sign at port B is named as the control flag and flag at port An is named as approaching sign. At the point when there are signs present at port An and port B then there is a nearness of light flag at the bar port a d nonattendance of light flag at the cross port. Without co ntrol signal at port B and nearness of approaching sign at port A, the yields of MZI are traded and results within the sight of light at the cross port and no light at the bar port. Here, nonappearance of light is considered as the rationale esteem 0 and p resence of light is considered as rationale quality 1.

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This conduct of SOA based MZI switch can be composed as Boolean capacities having contributions to yields mapping as (A, B) → (P=A.B, Q = A.B), where A, B are the sources of info and P, Q are the yields of MZI, individually. The optical expense and the postponement ( ) of MZI based all optical switch is considered as solidarity. The creators have considered the accompanying enhancement parameters for the all-optical reversible rationales: optical expense i.e. number of MZI switches, number of BC and BS utilized as a part of the rationale circuit, and optical postponement i.e. number of phases of MZI switches utilized as a part of the outline of rationale circuit.

All-optical Feynman gate:

The Feynman door (FG) has mapping (A, B) → (P=A, Q=A⊕B) where A, B are the sources of info and P=A, Q=A⊕B are the yields, individually. The Feynman entryway can be acknowledged utilizing 2 MZI switches, 2 beam combiners (BC) and 3 pillar splitters (BS) in all optical domain as appeared in figure 3 [4].

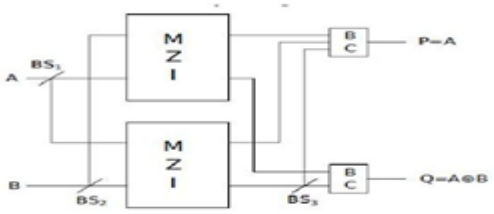

Fig.3. Feynman gate and its all-optical implementation [4]

III.PROPOSED ALL-OPTIC AL REVERSIBLE LOGIC GATE:

We have proposed another M NOT door and exhibited an all-optical acknowledgment of 4×4 Toffoli Gate which is effective to outline upgraded optical reversible circuits.

A. Proposed all-optical reversible MNOT Gate:

Another 2×2 all-optical reversible MNOT entryway (1, A) → (P, Q) has been proposed, where P =A and Q = A. Figure 4 demonstrates the Block chart of M NOT entryway. This entryway produces sensible NOT of the information rationale A. Table I demonstrates reality table of MNOT entryway.

Fig. 4. Block diagram of Proposed 2×2 MNOT gate

TABLE I TRUTH TABLE OF THE PROPOSED REVERSIBLE GATE

Input		Output	
1	*A*	$P = A$	$Q = \bar{A}$
1	0	0	1
1	1	1	0

The all-optical reversible MNOT entryway has been appeared in figure 5. This entryway is planned with single MZI switch. The approaching sign of MZI switch is set to 1 then yield produced at cross port is backwards of the contribution at control signal. The optical expense of MNOT entryway is one. NO Beam Splitter (BS) or Beam Combiner (BC) is utilized as a part of this entryway. As stand out MZI switch is utilized, so the postponement is 1∆.

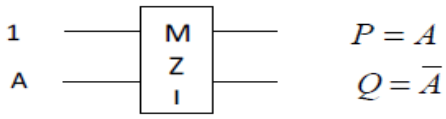

Fig.5. Proposed 2×2 Optical Reversible MNOT gate

The optical MNOT entryway is a valuable rationale door altogether optical reversible circuit acknowledgment. Prior the creators have utilized Feynman entryway to produce reverse of rationale with optical cost 2 MZI switches. Utilizing this door cost has been diminished to one MZI switch.

B.Optical Realization of 4×4 Toffoli Gate:

The 4×4 Toffoli Gate (4×4 TG) is mapped from information vector (A, B, C, D) to yield vector (P, Q, R, S), where P=A, Q=B, R=C, and S=D ⊕ABC, separately. Fundamentally, 4×4 Toffoli entryway is Multiple Controlled Toffoli door (MCT) with 3.

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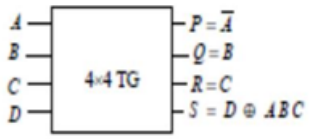

Fig. 6. Block diagram of 4×4 Toffoli gate

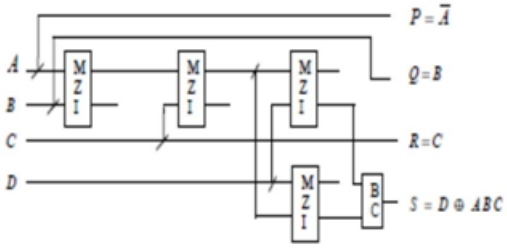

Fig. 7. All-optical Realization of 4×4 Toffoli gate control lines.

Figure 6 demonstrates the Block diagram and Figure 7 Shows the all - optical acknowledgment of 4×4 Toffoli door. This entryway has been acknowledged with 4 MZI Switches, Five Beam splitters (BS) and one Beam Combiners (BC). The optical deferral of this entryway is considered as 3Δ.

IV.PROPOSED GENERAL DESIGN A PPROACH

We have acknowledged optical reversible circuits utilizing MZI switches as a part of various ways. No predetermined methodology is followed in the combination of the all - optical reversible circuits. In this work, we have proposed a general configuration way to deal with understand all-optical reversible circuits. The methodology is depicted as takes after:

Algorithm 1: Design approach to realize optical reversible circuits
Step1. Consider the craved combinational rationale circuit
Step2.IF the craved rationale capacity is unpredictable then
Step3.Apply Replacement Method
Step4. ELSE apply Truth Table based Method with wanted yield rationale capacity
Step5. Understand the optical reversible rationale circuit

Algorithm 2: Replacement Method
Step1. Rehash step 2 to 6 WHILE every one of the entryways in the ordinary rationale circuit are supplanted
Step2. Pick a rationale entryway from ordinary circuit
Step3. In the event that proportional optical reversible door is as of now existed then
Step4. Supplant the picked entryway with proportional door
Step5. ELSE plan the required optical reversible rationale door with truth table based technique
Step6. Supplant the picked entryway with this outlined door
Algorithm 3: Truth table Based method
Step1. Determine the wanted yield rationale capacity from reality table of the circuit
Step2. Include steady information sources and junk yield lines to make it reversible if necessary
Step3. Outline the all-optical reversible circuit utilizing MZI switches, Beam Splitters and Beam Combiners understanding the rationale capacities at yield lines

V.PROPOSED ALL-OPTICA L REVERSIBLE LOGIC CIRCUITDESIGNS

A. Proposed All-optical Reversible 2×1 Multiplexer

This area portrays the outline and acknowledgment of the reversible 2×1 Multiplexer taking all things together optical space utilizing the proposed MNOT door and optical Toffoli Gate (TG) [4]. It has two information inputs (D0 and D 1), a solitary yield O and a select line S0 to choose one of the two info information lines.

The yield capacity of 2×1 Multiplexer is given by O = S0D0+S0D1. Reality table of 2×1 Multiplexer is appeared in table II. The optical acknowledgment of 2×1 Reversible Multiplexer is appeared in figure 8. It is planned with one MNOT and two TG doors. Here, MNOT door acts as NOT entryway. At the point when the third info line of TG is set to Constant 0 (Zero), the TG carries on as AND door.

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TABLE II TRUTH TABLE OF 2×1 MULTIPLEXER

Input			Output
D_0	D_1	S_0	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

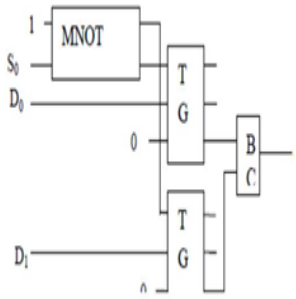

Fig.8.Optical Realization of 2×1 Reversible Multiplexer

The MNOT entryway is made of 1 MZI Switch. No BS and BC are utilized as a part of the outline of MNOT entryway. The TG is made of 3 MZI Switches, 4 BS and one BC [4]. The deferral of MNOT entryway is 1Δ and that of TG is 2Δ. Hence, add up to optical expense of Optical Reversible 2×1 Multiplexer is 7 MZI Switches; all out Beam splitters utilized are 8; pillar Combiners utilized are 3 and Delay of the multiplexer circuit is figure d as 3Δ as the two TG are working in parallel. It can be watched that optical expense of the Optical Reversible 2×1 Multiplexer has been enhanced fundamentally in contrast with existing one [7] which was actualized utilizing 8 MZI switches, 12 Beam splitters, 5 Beam combiners, and optical deferral 3Δ.

B. Proposed All-optical Reversible Full Adder Circuit

This area depicts a configuration of all-Optical reversible full Adder circuit utilizing two existing all-Optical Reversible Logic entryways with enhanced Optical expense.

Reality table of the full snake circuit is appeared in the table III. The yield elements of Full Adder circuit are given as takes after:

S = A ⊕B ⊕C ; Cout=AB+ (A⊕ B) C

TABLE III TRUTH TABLE OF THE FULL ADDER CIRCUIT

Input			Output	
A	B	C	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The new enhanced Optical Reversible Full Adder circuit is composed utilizing two existing all-optical reversible rationale doors; One is Optical Feynman Gate which is mapped as (A, B) → (P,Q) where P=A and Q=A⊕B, and another is ORG-I [8] which is mapped as (A, B, C) → (P, Q, $\overline{R}$) where P=AB+(A⊕B)C,Q=A⊕B and $R=A\overline{B}+(A\oplus B)C$. The ORG-I entryway is appeared in the Figure 9. T he enhanced all-optical reversible full viper is appeared in the figure 10. Input bit A, B and C are passed at three contributions of the ORG - I entryway. The yield P of ORG-I executes the yield convey capacity of Full viper; Output Q of ORG-I and information C are passed to info lines of Feynman door which produces yield Sum Function of Full Adder.

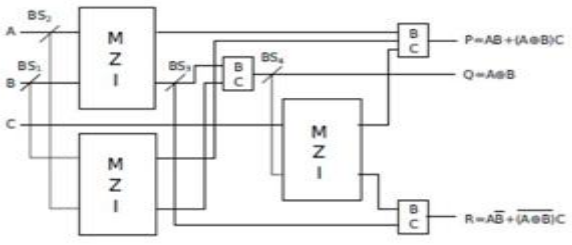

Fig. 9.Optical Reversible Gate (ORG)-I [8]

The ORG-I has 3 MZI switches, 4 BS and 3 BC with optical deferral as 2Δ. The Feyn man Gate is acknowledged with 2MZI switches, 3 BS, 2 BC and optical postponement is 1Δ.

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Hence, it can be seen from the assume that All-Optical Reversible Full Adder is acknowledged with 5 MZI switches, 8 Beam Splitters and 5

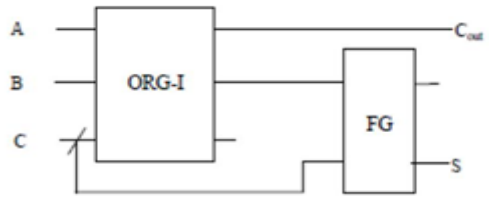

Fig.10.The improved All- Optical Reversible Full Adder

Shaft Combiners. The optical deferral is considered as 3Δ. It can be seen that the optical expense of the All-Optical Reversible Full Adder Circuit is enhanced essentially contrasted with the current outline of Full viper circuit [8] regarding MZI switches and Beam Combiners.

B.1. 4-bit Optical Reversible Full Adder Circuit:

A 4 - bit optical reversible full viper circuit is composed utilizing 4 ORFA (optical reversible full snake). The graph of the 4-bit optical reversible full viper is appeared in the Figure 11. The convey yield of first ORFA is passed to convey contribution of second ORFA, convey yield of second ORFA is passed to convey contribution of third ORFA et cetera. At long last the convey yield line of the fourth ORFA produces yield convey of expansion of two 4-bit numbers. The aggregate yield line of all he ORFA on the whole delivers 4-bit entirety of two 4-bit numbers.

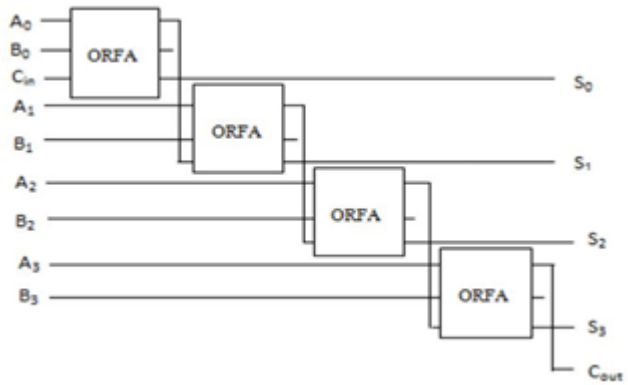

Fig. 11. 4-bit Optical Reversible Full Adder Circuit

Optical expense of the circuit is 20 MZI switches as each ORFA is planned with 5 MZI switches, 8 Beam Splitters and 5 Beam Combiners. In this way, add up to 32 BS and 20 BC are utilized as a part of the outline of 4-bit optical reversible full viper. The optical deferral of the circuit is 12Δ.

C. Design of Optical Reversible 4×1 Multiplexer:

This is first endeavor in the writing for planning all-Optical Reversible 4×1 multiplexer circuit. The all-optical Reversible 4×1 Multiplexer circuit has been acknowledged with proposed Optical Reversible MNOT entryway and Optical 4×4 Toffoli Gate (4×4 TG). It has four information input lines (D0-D3), two choice lines S0 and S1 to choose one of the four sources of info and a solitary yield line O. the expression for information yield O is given as

$$O = D_0\overline{S}_0\overline{S}_1 + D_1S_0\overline{S}_1 + D_2\overline{S}_0S_1 + D_3S_0S_1$$

Reality table of 4×1 Multiplexer is appeared in table IV .The optical acknowledgment of the 4×1 Reversible Multiplexer is appeared in the figure 12. It is planned utilizing two MNOT entryways and four optical 4×4 TG doors. The fourth info lines of all the 4×4 TG are set to steady 0, which brings about Logical AND of the staying three contributions at fourth yield line of 4×4 TG. The fourth yield lines of all the 4×4 TG are joined utilizing Beam Combiner (BC) at the last yield. The MNOT door is composed with 1 MZI Switch. No BS and BC are utilized as a part of the configuration of MNOT door.

The 4×4 TG is acknowledged with four M ZI Switches, Five Beam splitters (BS) and one Beam Combiners (BC). The deferral of this door is considered as 3Δ. Along these lines, the optical expense of the all - optical 4×1 Reversible Multiplexer circuit turns out to be 18 MZI Switches, 24 BS, 5 BC. The deferral is figured 4Δ as two MNOT doors and in addition four 4×4 T G are working in parallel.

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TABLE IV THE TRUTH TABLE OF 4×1 MULTIPLEXER

Input		Output
S_1	S_0	O
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

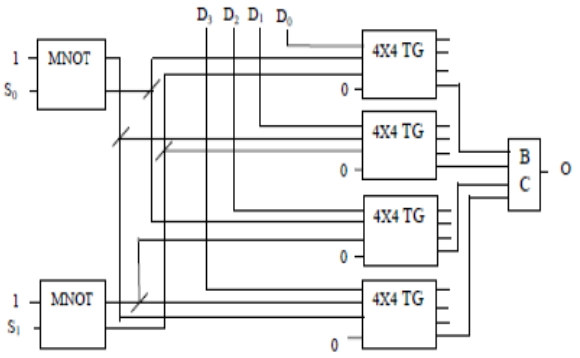

Fig. 12. Design of 4×1 Optical Reversible Multiplexer

D. Design of Optical Reversible 1×4 De-Multiplexer:

Creators, in the writing, have not yet composed any single Reversible 1×4 De-Multiplexer in optical area. This is first time, an All - optical Reversible 1×4 De-Multiplexer has been proposed. It has one info information line D, 2 select info lines (S0 and S1) and four yield lines (O 0-O3). Reality table of 1×4 De-Multiplexer is appeared in table V. The expression for yield lines are given as takes after:

$$O_0 = D\bar{S}_1\bar{S}_0, O_1 = D\bar{S}_1S_0, O_2 = DS_1\bar{S}_0 \text{ and } O_3 = DS_1S_0$$

For optical realization of Reversible 1×4 De-Multiplexer, transformation based approach is used. The Optical Reversible 1×4 De-Multiplexer is designed with optical MNOT gate and optical 4×4 TG gates. The logical NOT Gate and the logical AND are replaced with proposed optical reversible MNOT gate and 4×4 TG, respectively. Optical realization is shown in Figure 13.

TABLE V TRUTH TABLE OF 1×4 DE-MULTIPLEXER

Input		Output			
S_1	S_0	O_3	O_2	O_1	O_0
0	0	0	0	0	D
0	1	0	0	D	0
1	0	0	D	0	0
1	1	D	0	0	0

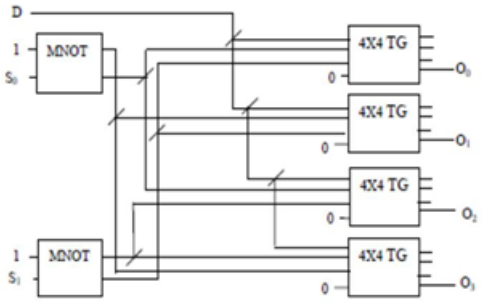

Fig. 13.Optical realization of reversible 1×4 De-Multiplexer

It can be watched that 2 optical MNOT entryways and four 4×4 TG doors have been utilized as a part of optical acknowledgment of 1×4 De-Multiplexer. This circuit is composed utilizing 18 MZI Switches, 27 Beam Splitters and 4 Beam Combiners. Two MNOT Gates and also four 4×4 TG are associated in parallel. Along these lines, Delay is ascertained as 4Δ.

E. Design of Optical Reversible 3to8 Decoder:

A Decoder circuit is like the De-Multiplexer circuit yet there is no information input line. This is additionally first time endeavor in the writing to outline an all-Optical Reversible 3to8 Decoder circuit. A 3to8 Decoder has three information lines (P, Q, R) and eight yield lines (O0 - O7). Reality table of 3to8 decoder has been given in table VI. The yield capacity of the 3to8 Decoder is communicated as takes after:

$$O_0 = \bar{P}\bar{Q}\bar{R} \; ; \; O_1 = \bar{P}\bar{Q}R \; ; \; O_2 = \bar{P}Q\bar{R} \; ; \; O_3 = \bar{P}QR$$

$$O_4 = P\bar{Q}\bar{R} \; ; \; O_5 = P\bar{Q}R \; ; \; O_6 = PQ\bar{R} \; ; \; O_7 = PQR$$

Optical reversible 3t08 decoder outlines utilizing proposed MNOT door and Optical 4×4 T G.

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To understand this circuit, three MNOT entryways and eight 4×4 TG doors are required. The all-Optical acknowledgment of the reversible 3to8 Decoder is appeared in the figure 14. The circuit is outlined with 35 MZI switches, 58 Beam Splitters and 8 Beam Combiners. Postponement of the circuit is 4Δ.

TABLE VI TRUTH TABLE OF 3TO8 DEC ODER

Input			Output							
P	Q	R	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

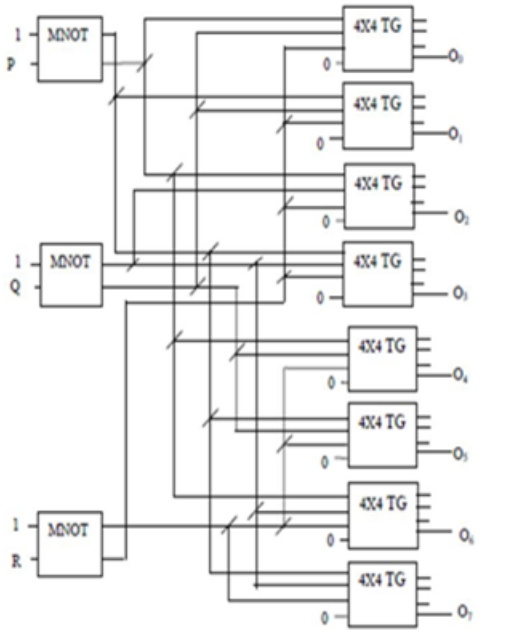

Fig. 14.All-Optical realization of the reversible 3to8 Decoder

VI. COMPARISION RESULTS:

The optical expense and optical proliferation deferral of the proposed all-optical reversible rationale circuits have been figured in the past area. Here the same have been broke down and a summery has been exhibited in the accompanying tables.

Comparative investigations of proposed outlines of all-optical reversible 2×1 multiplexer and full snake circuits with the current plans are introduced in table VII and VIII individually. This examination depends on the enhancement parameters, for example, optical cost, bar splitters, shaft combiners, and optical postponement of the circuits. The change rate (IP) is computed utilizing the formulae: (1-proposed outline cost/existing configuration cost) ×100. It can be watched that the proposed plans have been enhanced as far as MZI switch BS and BC.

TABLE VII COMPARATIVE STUDY OF ALL OPTICAL REVERSIBLE 2×1

Proposed Design	MZI Switch {IP in %}	BS {IP in %}	BC {IP in %}	Optical delay {IP in %}
Our proposed design	7 {12.5% }	8 {33.33%}	3 {40%}	3Δ {No IP }
G. K. Maity et al.	8	12	5	3Δ

TABLE VIII COMPARATIVE STUDY OF ALL-OPTICAL REVERSIBLE FULL ADDER CIRCUIT

Proposed Design	MZI Switch {IP in %}	BS {IP in %}	BC {IP in %}	Optical delay {IP in %}
Our proposed design	5 {16.66%}	8 { No IP }	5 {16.66%}	3Δ {No IP }
S. Kotiyal et al.	6	8	6	3Δ

All-optical reversible outlines of 4×1 multiplexer, 1×4 De-multiplexer and 3to8 Decoder circuits are proposed first time, accordingly, optical expense and optical deferral of the these circuits have been introduced in table IX.

TABLE IX OPTICAL COST AND DELAY OF ALL-OPTICAL REVERSIBLE 4×1

MULTIPLEXER, 1×4 DE-MULTIPLEXER AND 3TO8 DECODER

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Proposed Design	MZI Switch	BS	BC	Optical delay
4×1 multiplexer	18	24	5	4Δ
1×4 De-multiplexer	18	27	4	4Δ
3to8 Decoder	35	58	8	4Δ

VII. SIMULATION RESULTS

All the blend and reproduction results are performed utilizing Verilog HDL. The union and reenactment are performed on Xilinx ISE 14.4. The reenactment results are appeared underneath figures.

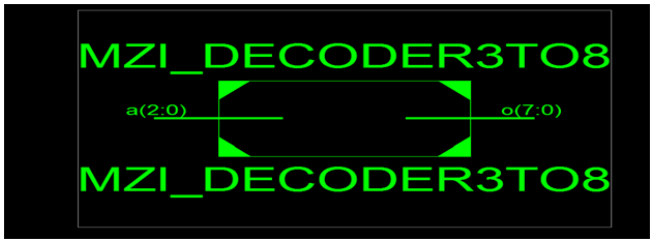

Fig.15: RTL schematic of All-Optical realization of the reversible 3to8 Decoder

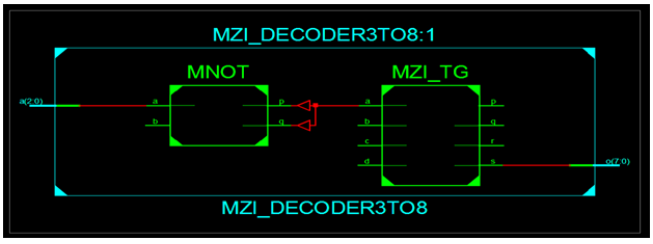

Fig.16:RTL sub schematic of All-Optical realization of the reversible 3to8 Decoder

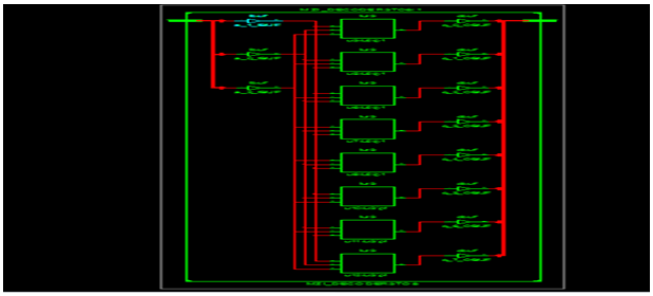

Fig.17: Technology schematic of All-Optical realization of the reversible 3to8 Decoder

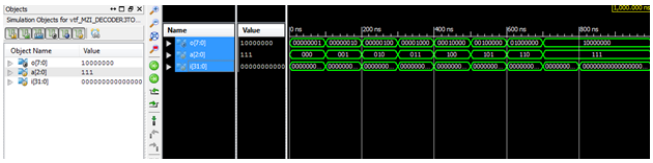

Fig.18: Simulation of All-Optical realization of the reversible 3to8 Decoder

CONCLUSION AND FUTURE SCOPE:

Optical figuring is developing as a possible innovation to execute reversible rationale. We have proposed another general configuration way to deal with understand all-optical reversible rationale circuits utilizing SOA based MZI switches. An all-optical reversible MNOT door has been proposed. The optical expenses of the all optical reversible 2×1 multiplexer and full viper circuits have been minimized in the proposed plans. A 4-bit full snake circuit has been additionally composed utilizing this full viper circuit. New plans of All-optical reversible outlines of 4×1 multiplexer, 1×4 De-multiplexer and 3to8 Decoder circuits are proposed first time. An advancement calculation might be proposed to minimize the optical expense of the all optical reversible circuits and the current outlines might be upgraded. All –optical reversible successive circuits might be outlined.

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