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Design and Analysis of Testable Reversible Sequential Circuit Using Verilog HDL

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Abstract:
Programmable reversible logic design is trending as a prospective logic design style for implementation in recent nanotechnology and quantum computing with low impact on circuit heat generation.The design of testable sequential circuits by two vectors using conservative logic. The proposed sequential circuits based on conservative logic outclass the traditional sequential circuits built using classical gates in terms of testability. Any sequential circuits based on conservative logic can test for stuck-at 0 and stuck-at 1 fault by using two vectors 0 and 1. The design of testable Master-slave D flip-flop, Double Edge triggered flip flop (DET) flip-flop using two vectors 0 and 1 are presented. The importance of the proposed work is that we are designing reversible sequential circuits suitable for testing. Hence both conservative logic and reversible logic is used. In the proposed work, we design a reversible sequential circuit using Fredkin gate. Fredkin gate is the only reversible gate which supports both conservative and reversible logic and also having less quantum delay.

Index terms: ***conservative logic, reversible logic, Fredkin gate, D flip-flop.***

INTRODUCTION

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. Reversible computing differs from conventional computing in that it performs the computation in a logically reversible way: The output of a (fully) reversible circuit always uniquely identifies the input. Circuits can take advantage of this logical reversibility to reduce power by reusing the information instead of discarding it: Landauer showed that any time a bit of information is discarded, it equates to some quantum of energy lost as heat [1].Moreover in 1973, Bennett has shown that this energy loss can be reduced or even removed if the circuits are designed using reversible gates [2].

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Reversible logic takes care of Fan-out problem. It supports the process of running the system both forward and backward. The proposed technique will take care of the fan-out (FO) at the output of the reversible latches and can also disrupt the feedback to make them suitable for testing by only two test vectors, all 0s and all 1s. By this way we can easily test the circuit with ease. In other words when circuit is executed in normal mode, feedback will be present because to compensate for the extra inputs. And similarly when executed in test mode its feedback is disrupted and the circuit is tested for stuck-at-faults. So proposed technique is divided in to two modes normal and test mode. Fan-out leads to increased capacitive load on the driving gate, and therefore longer delay. So the fan-out problem is taken care by the proposed technique. The proposed technique is

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extended toward the design of two vectors testable master-slave flipflops and double edge triggered (DET) flip-flops.

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any past stage by computing backwards or uncomputing the results. This is termed as logical reversibility. The advantages of logical reversibility can be gained only after employing physical reversibility. It is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically not possible. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, that is not only the outputs can be uniquely determined from the inputs, but also the inputs can be regained from the outputs. In this paper we will be discussing in section-II about the different reversible logic gates and a detailed explanation of Fredkin gate which is common to both conservative and reversible logic. And section-III explains about the literature survey undertaken in this project. Section-IV deals with design of testable D latch, master-slave D flip-flop, DET flip flop. Section-V deals with the future enhancement and conclusion to the project.

REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to find out the outputs from the inputs and also the inputs can be uniquely regained from the outputs. In reversible circuits, direct fan-Out is not allowed as one–to-many concept is not reversible. Also fanout in reversible circuits is achieved using extra gates.

A reversible circuit should be designed using minimal number of reversible logic gates. From the approach of reversible circuit design, there are many factors for determining the complexity and performance of circuits.

[1] The number of Reversible gates (N): The number of reversible gates used in circuit.

[2] The number of constant inputs (CI): This refers to the number of inputs that are to be preserved constant at either 0 or 1 in order to produce the given logical function.

[3] The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. Also the garbage outputs as these are very essential to achieve reversibility.

[4] Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate.

There are different reversible gates and they are:

- Not gate
- Feynman gate (CNOT)
- Fredkin gate (CSWAP)
- Toffoli gate
- Peres gate
- Sayem gate
- Double Feynman gate

In this Toffoli gate and Fredkin gate are universal gates. Universal gates means using these gates any type of Boolean expression can be obtained (i.e.) any type of circuits can be designed. Not gate is the basic reversible gate. Feynman gate is a 2*2 one through reversible gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q = A XOR B. Toffoli gate is a 3*3 gate, the input & output vector is I (A, B, C), O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB XOR C. NOT gate is an inverter which inverts the input. Likewise other gates are known. In this we select Fredkin gate mainly because it is compatible with both reversible and conservative logic.

FREDKIN GATE:

Fredkin gate is a 3*3 gate shown in Fig 1. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B XOR AC and R=A′C XOR AB. Quantum cost of a Fredkin gate is 5. It is used for designing sequential circuits because it is the only common gate that can be used in conservative, switch, interaction and reversible logic.

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Due to its unique characteristics and properties Fredkin gate is used for designing sequential circuit and also it reduces delay and area used for designing a circuit. It is reversible and Conservative in nature,(i.e.) it has unique input and output mapping and also has the same number of 1's in the outputs as in the inputs. Fredkin gate has three inputs, depending on the first input which is a control signal outputs are produced. If the first input is 1 means then the other two inputs are regained as outputs. If the input is 0 then the other two inputs are swapped and produced as outputs.

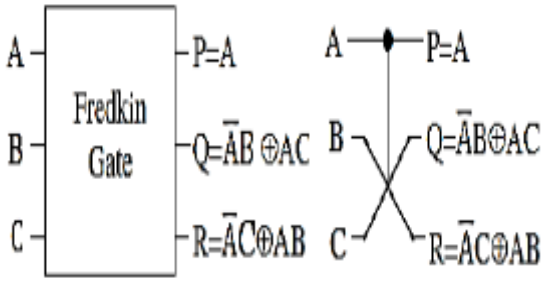

Fig1. Fredkin gate

III.LITERATURE SURVEY

Any nanotechnology having applications of reversible logic, such as based on nano-CMOS devices, low power molecular QCA computing, or NMR-based quantum computing, all are vulnerable to high error rates due to transient faults. With regard to this paper on reversible sequential circuits, the model of reversible sequential circuits is addressed in the various interesting contribution in which the designs are improved in terms of various functions, such as the number of reversible gates, quantum cost, garbage outputs, delay etc. To the best of our understanding, the offline testing of faults in reversible sequential circuits is not addressed in the literature. In this paper, we present the design of reversible sequential circuits that can be tested by only two test vectors, all 0's and all 1's, for any unidirectional stuck-at-faults. By giving all the inputs as 1 we test for stuck-at-0 fault and similarly if we give all the input as 0 means we test for stuck-at-1 fault.

IV. PROPOSED SYSTEM

A.DESIGN OF TESTABLE REVERSIBLE D LATCH

The characteristic equation of the D latch can be written as Q+ = D · E + .E · Q. In the proposed work, enable (E) refers to the clock and is used conversely in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q+ = D. While, when E = 0 the latch preserves its previous state, that is Q+ = Q. In Fig. 2(a) reversible D latch is shown and its characteristic equation is reverse of D latch characteristic equation but that designcannot be tested only by two vectors because of feedback. Some misinterruptions may occur. So in our proposed work we will cascade two Fredkin gate and Q output of one gate will follow the other. And it has two control signals C1 and C2 by which the design works. In normal mode which is shown in Fig. 2(b) works when C1 and C2 is given as 0 and 1 and the circuit works as aD latch without any fan-out problem. In test mode which is shown in Fig. 2(c) and (d) works when C1 and C2 is given as 1 and 1 or 0 and 0, the circuit disrupts the feedback and
checks for stuck-at-0 or stuck-at-1 fault.

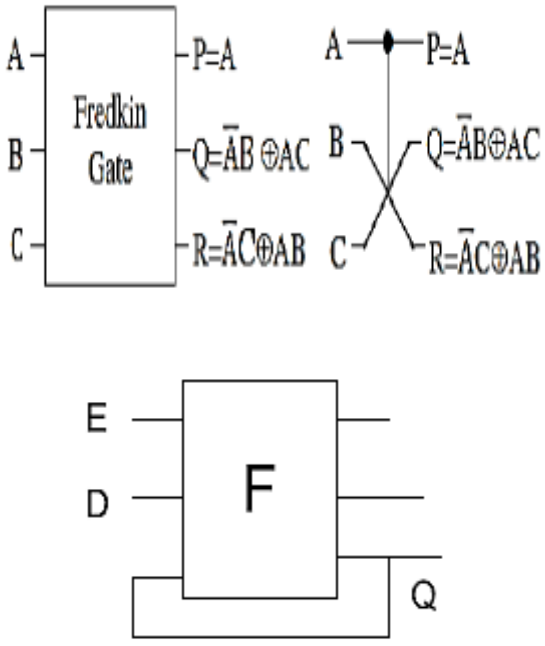

Fig .2(a).Reversible D latch

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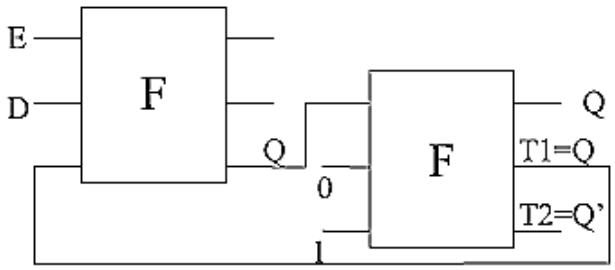

Fig .2(b).Normal mode

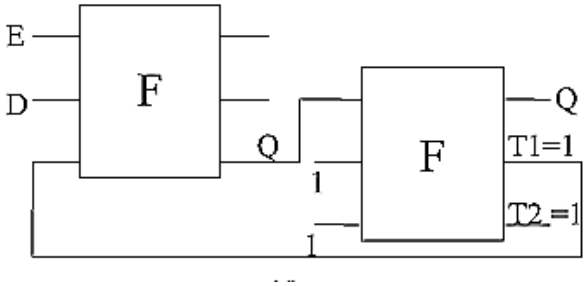

Fig .2(c.)Test mode for stuck-at-0 fault

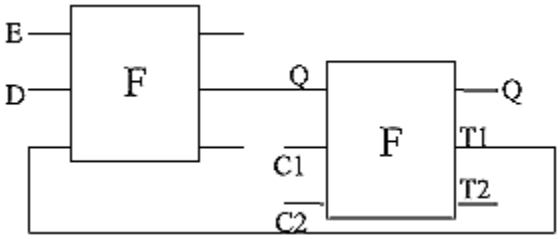

Fig .2(d). Test mode for stuck-at-1 fault

B. DESIGN OF TESTABLE NEGATIVE ENABLE DLATCH

A negative enable reversible D latch will pass the input Dto the output Q when E = 0; otherwise preserves the previousstate. The characteristic equation of the negative enable Dlatch is Q+ = D·E +E·Q. This characteristic equation of thenegative enable reversible D latch can be mapped on thesecond output of the Fredkin gate. The next Fredkin gate inthe design take cares of the FO. This Fredkin gate in thedesign also helps in making the design testable by two testvectors, all 0's and all 1's, by breaking the feedback based oncontrol signals C1 and C2 as illustrated above for positiveenable D latch. The negative enable D latch is helpful in thedesign of testable reversible master-slave flip flops. This isbecause as it can work as a slave latch in the testablereversible master-slave flip-flops in which no clock inversionis required.

C. DESIGN OF TESTABLE MASTER-SLAVE FLIPFLOPS

We have proposed the design of testable flip-flops usingthe master slave strategy that an be tested for any stuck-atfaults using only two test vectors, all 0s and all 1s. Masterlatch will be positive enabled Fredkin gate based D latch andslave latch will be negative enabled Fredkin gate based Dlatch. Fig 4 shows the master-slave D flip flop. There are 4control signals sC1, sc2, mC1 and mc2. mC1 and mC2control the master latch and similarly sC1 and sC2 control theslave latch. When signals are given as 0 and 1 it will work innormal mode and avoid fan outproblem. If the signals aregiven 0 and 0 it will disrupt the feedback and test the circuitfor stuck-at-1 fault. Suppose if the signals are given as 1 and1 then it will test the circuit for stuck-at-0 fault. Here Mastercontrols the slave latch. If signal is given as 1 master latchworks and vice-versa slave latch will work.

D. DESIGN OF TESTABLE REVERSIBLE DETFLIP-FLOPS

In the master-slave flip-flop, it does not sample the dataat both clock edges; instead it waits for the next rising edgeof the clock to work as a master or slave latch. In order toovercome the abovementioned problem, researchers haveintroduced the concept of DET flip-flops which sample thedata at both the edges. Thus, DET flip-flops can sample andreceive two data values in a clock period thus frequency ofthe clock can be reduced to half of the master- slave flip-flopwhile maintaining the same data rate. The half frequencyoperations make the DET flip flops very much useful for lowpower computing as frequency is equal to powerconsumption in a circuit. It is designed by connecting the twolatches, via, the positive enable and the negative enable inparallel rather than in series. The 2:1 Multiplexer at theoutput transfer the output from one of these latches which isin the storage state (is holding its previous state).

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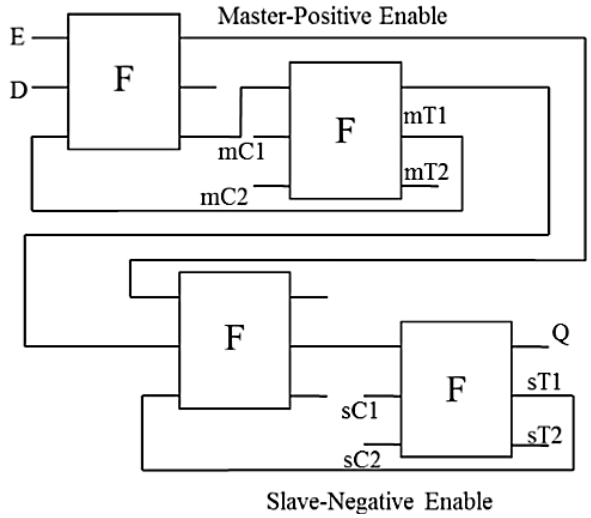

Fig4. Master-slave D flip-flop

In the proposed design of testable reversible DET flipflop, the positive enable testable reversible D latch and the negative enable testable reversible D latch are set up in parallel. The Fredkin gates labelled as 1 and 2 forms the positive enable, while the Fredkin gates labelled as 3 and 4 forms the negative enable testable D latch. In reversible logic Fan-out is not allowed so the Fredkin gate labelled as 6 is used to copy the input signal D. The Fredkin works as the 2:1 MUX and transfer the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state (is holding its previous state) to the output Q. In the proposed design of testable reversible DET flip-flop, nC1 and nC2 are the controls signals of the testable negative enable D latch, while pC1 and pC2 are the control signals of the testable positive enable D latch.Depending on the values of the pC1, pC2, nC1, and nC2, the testable DET flip-flops work either in normal mode or in the testing mode.

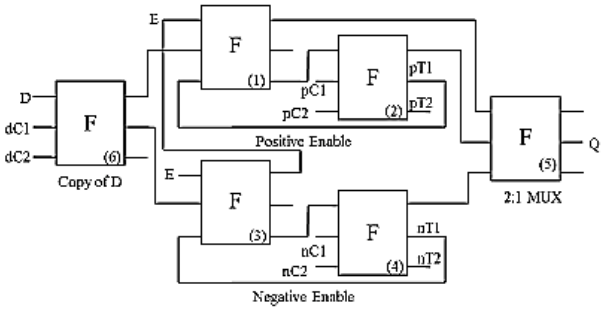

Fig5. DET flip-flop

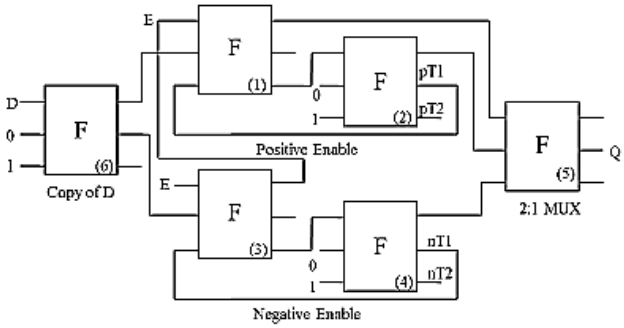

Fig5(b). normal mode

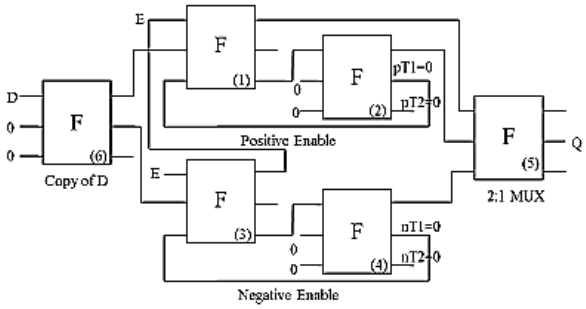

Fig5(c).test mode for stuck-at-1 fault

In normal mode pC1 and pC2 are given as 0 and 1 and similarly nC1 and nC2 are given as 0 and 1. The pC1 = 0, pC2 = 1 help in copying the output of the positive enable D latch thus avoiding the Fan-out while the nC1 = 0 and nC2 =1 help in copying the output of the negative enable D latch thus avoiding the FO. Similarly in test mode if all signals are given as 0 then it tests the circuit for stuck-at-1 fault. If all the signals are given as 1 then it tests for stuck-at-0 fault.

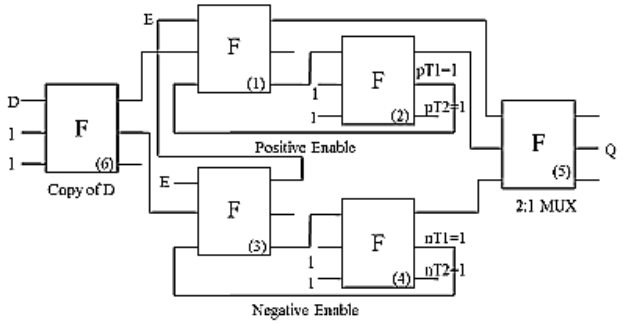

Fig5(d). test mode for stuck-at-0 fault

V.SIMULATION RESULTS

The corresponding simulation results of the reversible testable sequential circuits are shown below. All the

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synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

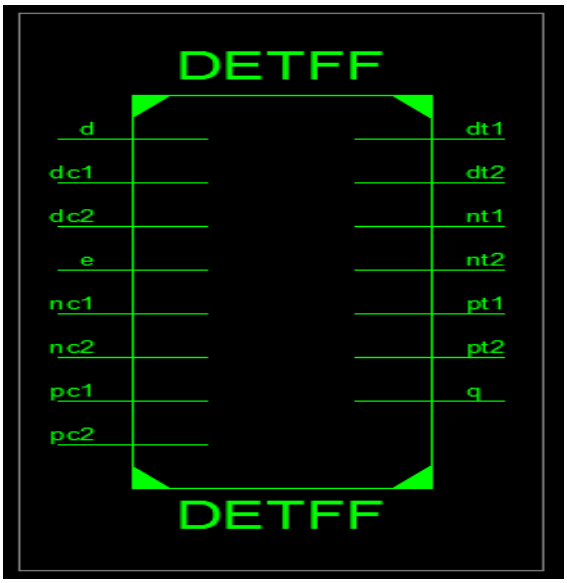

Figure-6: RTL schematic of Top-level of DET Flip Flop

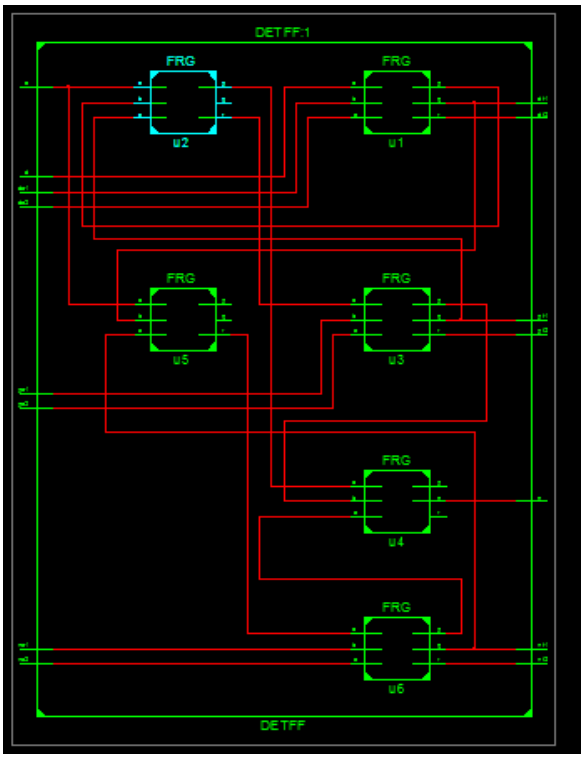

Figure 7: RTL schematic of Internal block of DET Flip Flop

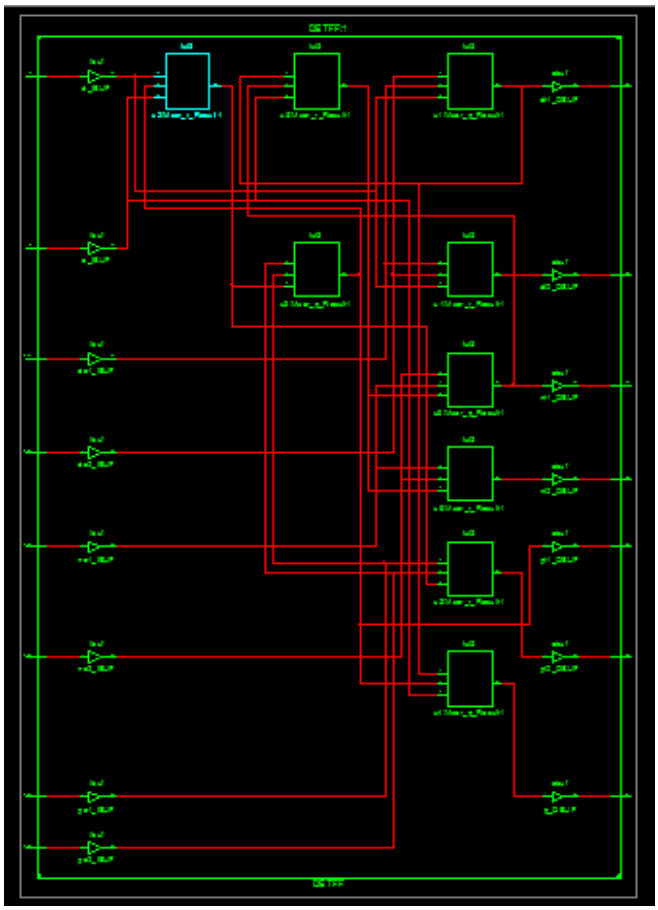

Figure 8: Technology schematic of DET Flip Flop

DETFF Project Status (10/01/2016 - 05:15:53)			
Project File:	SCKTS_ISE.xise	**Parser Errors:**	No Errors
Module Name:	DETFF	**Implementation State:**	Synthesized
Target Device:	xc3s500e-4fg320	**•Errors:**	No Errors
Product Version:	ISE 14.4	**•Warnings:**	2 Warnings (0 new)
Design Goal:	Balanced	**•Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	5	4656	0%
Number of 4 input LUTs	9	9312	0%
Number of bonded IOBs	15	232	6%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Oct 1 05:15:52 2016	0	2 Warnings (0 new)	0
Translation Report					
Map Report					

Figure 9: Design summary report of DET Flip Flop

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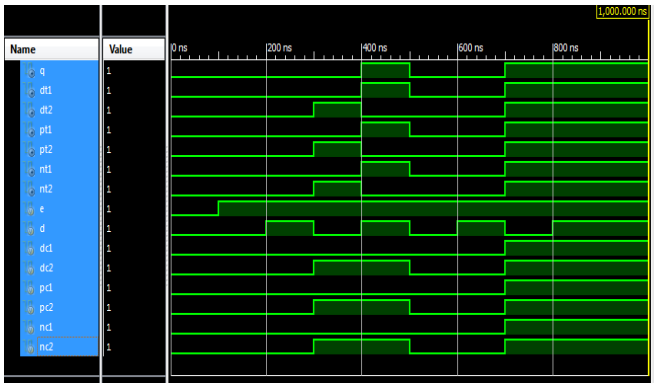

Figure 10: simulated outputs for proposed DET Flip Flop

CONCLUSION AND FUTURE ENHANCEMENT

Thus Reversible sequential circuits are designed using reversible and conservative logic successfully and tested forstuck-at-faults. A design of Fredkin gate, testable D latchusing Fredkin gate, Master slave flip-flop using Fredkin gate,DET flip flop is designed. It is made testable only using twovectors 0 and 1 and so complexity is reduced. In futurereversible and conservative logic will be designed forcombinational circuits and implemented and will be tested forfaults. Thus, the main advantage of the proposed conservativereversible sequential circuits compared to the conventionalsequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. Thereduction in number of test vectors minimizes the overheadof test time for a reversible sequential circuit.

In the proposed system we have designed sequentialcircuits using Fredkin gate. As sequential circuit has feedbackit supports reversible logic and hence we designed circuitsusing reversible logic gate. So in future I would be designingtestable combinational circuits which are irreversible using reversiblelogic.

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