

A Robust DC-Link Voltage Control Strategy to Enhance the Performance of Shunt Active Power Filters without Harmonic Detection Schemes



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Abstract:

This paper proposes a vigorous control procedure to diminish this disadvantage. In this methodology, the dc-link voltage is directed by a cross breed control system consolidating a standard proportional–integral P I and a sliding-mode (SM) controllers. The SM conspire constantly decides the increases of the P I controller taking into account the control circle blunder and its subsidiary. The babbling because of the SM plan is diminished by a move decide that fixes the controller picks up when enduring state condition is come to.

This controller is named as double sliding-mode-proportional–integral. The stage dog rents of the force matrix are by implication managed by twofold arrangement controllers with two degrees of opportunity, where the inner model rule is utilized to stay away from reference outline change. The proposed control methodology guarantees zero enduring state blunder and enhances the execution under hard homeless people, for example, load variety. Also, it presents power when the SAP F is working under unequal conditions. Trial comes about exhibit the execution of the proposed control plan.

Index Terms:

Adaptive control strategy, harmonic compensation, power factor correction, shunt active power filter (SAPF).

I. INTRODUCTION:

The developing utilization of force converters as inserted gadgets in family unit, business, or mechanical electronic-based machines has weakened the force nature of the mains. Those nonlinear burdens produce current sounds and receptive force that outcome in voltage drops on the supply system impedance and may instigate unbalance working conditions. These impacts can be surprisingly more terrible if the heaps change haphazardly. Ordinary arrangements, for example, detached channels for lessening consonant contamination are ineffectual.

Besides, the gauges and suggestions that delimit the limits of symphonious twisting and responsive force in the force framework have turned out to be more confined [1], [2], which has invigorated the use of dynamic force remuneration [3], [4]. SAP F s have been widely utilized for remuneration of sounds, responsive force, negative groupings, and/or flashes [5]– [7]. The customary control plans connected to SAP F are HEBSs on the grounds that their viability relies on upon how quickly and precisely the symphonious parts of the nonlinear burdens are distinguished [8]. Symphonious extractors utilized as a part of HEBSs can be actualized by utilizing diverse methodologies, for example, conventional $d - q$ strategy [9] and $p-q$ hypothesis [10], versatile channels [11], wavelet [12], GA [13], or ANN [14].

The SAP F can be additionally actualized without the utilization of the heap symphonious extractors. For this situation, the consonant remunerating term is acquired from the framework dynamic force parity [15]–[19]. These frameworks can be considered as BEBSs, and their execution relies on upon how quick the framework achieves the harmony state [17]. The control frameworks of SAP F actualized taking into account HEBS or BEBS ideas are by and large achieved by a course methodology formed by an inward control circle for managing the channel stage streams (HEBS) or lattice stage ebbs and flows (BEBS) and an external control circle to set the dc-join voltage. The adequacy of both arrangements relies on upon the execution of the control circles. On account of HEBS, the dc-join controller manages the dc capacitor voltage at the appropriate level to accomplish the remuneration goals. Besides, the present control circle ought to direct the SAP F stage streams, made primarily out of symphonious parts, which requires more mind boggling systems for accomplishing reasonable execution records. With respect to the situation when BEBS is utilized, the dc-join controller manages the dc capacitor voltage and guarantees the framework dynamic force equalization, which thusly decides the reference streams of the force matrix.

As the force framework stage streams in unflinching state are essentially made out of the principal part, the present control technique utilized can be disentangled. By and large, P I controllers have been utilized for managing the voltage of dc-connection capacitors of both methodologies. Be that as it may, a few other options to upgrade SAP F dc-join execution have been proposed, for example, the feedforward plans for repaying the force matrix voltage variances [20] or the utilization of versatile control systems for adaptability of receptive remuneration in half breed dynamic force channels [21]. As to current control circle, the strategy to be utilized relies on upon the system utilized. On account of HEBS, the standard arrangement utilizes P I controllers actualized in the directions of the network voltage vector reference outline [22].

Be that as it may, the utilization of these controllers brings about unflinching state mistakes, and the impediment of data transfer capacity has not took into account an attractive symphonious remuneration [23]. There are other conceivable arrangements, for example, bum control [24], SM control (SMC) [25], versatile control [26], thunderous control [27], and monotonous based control [28]. Among them, the last is by all accounts the most reasonable notwithstanding having the upside of specific consonant pay. Be that as it may, its usage requires a controller for the crucial recurrence and others for the staying consonant segments, which can be very costly [29]. At the point when the SAP F s are actualized by BEBS technique, the present control procedure can be improved by utilizing one and only thunderous controller per stage, tuned at the essential recurrence [17]. As of late, an alternate methodology of a versatile control system connected for SAP F utilizing the BEBS strategy has been proposed for repaying the consonant mutilation, receptive power, and unequal burden [17]. In this SAP F , the present control plan is executed by a versatile shaft situation control, incorporated with a variable structure plan (V S–AP P C). The primary preferred standpoint of the proposed control strategy refers to the diminishment of SAP F many-sided quality of usage

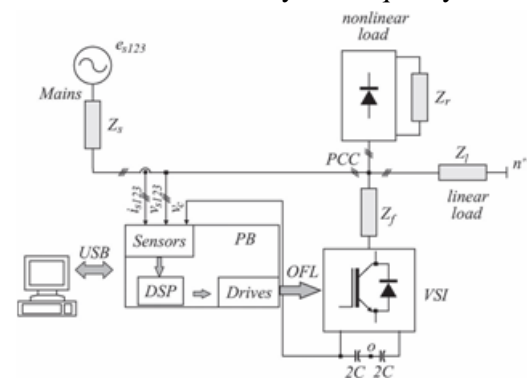


Fig. 1. Basic diagram of the proposed SAPF system:

Resulting in reduced costs (because it is not necessary to have load and filter phase current measurements, thus reduc-ing the number of current sensors), without reduction of its compensation effectiveness. However, this control scheme has a drawback that is the poor performance of the dc-link control loop during the

occurrence of severe load variations. This paper proposes a strong control procedure to enhance BEBS power channels amid extreme burden changes. In this approach, the dc-join voltage is managed by a crossover control technique made by the relationship out of a standard P I and a SM controllers. The SM plot consistently decides the additions of the P I controller in view of the control circle blunder and its subordinate. The prattling because of the SM plan is diminished by a move decide that fixes the controller picks up when framework consistent state is come to. This new controller is named as DSM – P I. The lattice stage streams are by implication regulated by DSCs with two degrees of opportunity, where the IMP is utilized to dodge reference outline change. These control structures guarantee zero consistent state mistake notwithstanding displaying heartiness to conceivable uneven characters in the SAP F system. The proposed control procedure is extremely appropriate for tested information control and can be effortlessly executed on DSPs. The execution of the proposed control plan is exhibited with a few test comes about.

II. SYSTEM DESCRIPTION AND MODELING:

Fig. 1 shows the topology of SAP F utilized as a part of the research center model. It involves a three-stage framework source es123 with its inside impedance ($Z_s = r_s + s l_s$) that sustains a three-stage load bank comprising of parallel relationship of a noncontrolled rectifier and a three-stage direct load ($Z_l = r_l + s l_l$). The SAP F is executed with a V SI associated with the P CC through inductors l_f (i.e., $Z_f = r_f + s l_f$, wherein r_f is the in-trinsic resistance of l_f). The control framework project is executed in a DSP connected in with a P B that handles the estimation of the variables, and additionally the converter drivers by means OF Ls.

A. SAPF Grid-Tied Power Converter Modeling:

The model of the SAP F grid-tied power converter considering the interaction of the grid impedances to both the system.

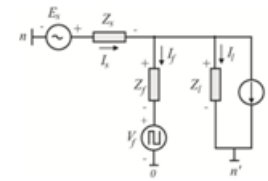


Fig. 2. Equivalent circuit of a SAPF system.

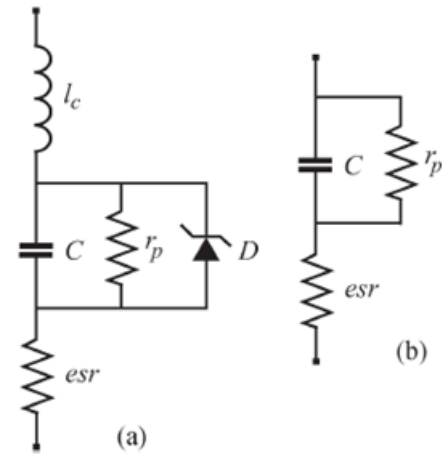


Fig. 3. Equivalent circuit of the electrolytic capacitor. (a) Manufacturer model. (b) Simplified model.

Load and the channel was comprehensively focused on in [17]. In perspective of this study, the structure in Fig. 1 can be depicted by the perphase practically identical circuit showed in Fig. 2. In this circuit, the nonlinear weight is addressed by a present source I_r that addresses the disfiguring streams made by the rectifier. From the indistinguishable circuit showed up in Fig. 2, repeat and temperature; it increases with terminal scattering. Resistance r_p accounts for spillage current in the capacitor; it decreases by extending capacitance, temperature, and voltage. The Zener diode D models the overvoltage and the inverse voltage conduct. Inductance l_c has basic qualities when the trading repeat used on the power converter is higher than 100 kHz. In applications with SAPF, the trading repeat used is far lower, and along these lines, the inductance l_c can be disregarded from the model. The Zener diode D is furthermore disregarded in light of the way that it doesn't impact the immediate behavior of the capacitor. Along these lines, the equivalent circuit of the capacitor can be decreased to the one showed up in Fig. 3(b).

The trade limit addressed by has a post that depends on upon the estimations of C and r and a zero dependent upon the estimations of C, rp, and esr. Considering a sensible circumstance where $rp \ll esr$, it is possible to improve the model given by , disregarding the estimation of esr.

III. CONTROL SCHEME:

Fig. 4 exhibits the square graph of the proposed control plan for the SAPF in view of the approach. In this block diagram, the dc-join voltage is directed by a DSM –PI controller. It is finished by producing the reference current i_{e*sd} , which decides the framework dynamic force part. The stage edge of the force lattice voltage vector θ is dictated by utilizing a PLL. In this manner, the dqreference stage streams in a stationary reference outline dqscan be acquired by $i_{s*sd} = i_{e*sd} \cos(\theta_s)$ and $i_{s*sq} = i_{e*sd} \sin(\theta_s)$, individually.

The reference current i_{e*sd} is characterized to ensure the dynamic force equalization of the SAPF framework. The stage streams of the force matrix are in a roundabout way managed by two DSCs, in which the IMP is utilized to maintain a strategic distance from reference outline changes. The DSCs create legitimate dynamic channel stage voltages v_{s*fd} and v_{s*fq} . These DSC current controllers will be portrayed next. The unmodeled aggravations I_{sd} and I_{rd} can be estimated and brought into the calculation of DSC current controllers.

However, hypothetical studies and trial articles have shown that this control plan has the capacity of compensating such unmodeled unsettling influences. Square $x_{sdq}/123$ performs the orthogonal change from the dq reference edge to the three-stage framework, i.e., from v_{s*fd} to v_{s*123} . Taking into account these reference voltages, an appropriate PWM procedure decides the duty cycle of V SI power switches.

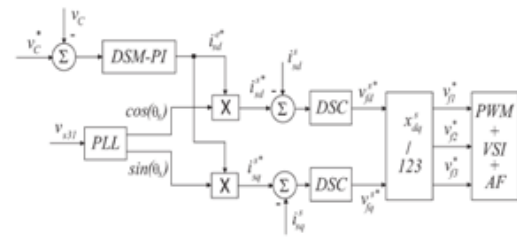


Fig. 4. Block diagram of the proposed control strategy. x_{edq} denotes voltage vector reference frame variables, whereas x_{sdq} denotes stationary reference frame variables.

A. Grid Currents Control Strategy:

The control system utilized in this paper for controlling the network streams (see square DSC in Fig. 4) depends at once arrangement control plan, which utilizes one controller for the positive succession and another for the negative grouping [32]. In addition, this controller has the benefit of utilizing the IMP as a part of its displaying that evades the reference outline change while ensures invalid unflinching state mistake.

B. DC-Link Voltage Controller:

The proposed control plan for the dc connection is executed by a nonstandard strong SM – PI, which is actualized by a proportional–integral (PI) controller in which its controller additions are figured by utilizing the SMC approach taking into account the sliding surface made by the control circle blunder and its subordinate. The prattling due to the SMC plan is lessened by a move plan, which alters the controller picks up when framework relentless state is come to. The incorporation of this move plan in the SM – PI controller brings about another controller that is named here as DSM – PI.

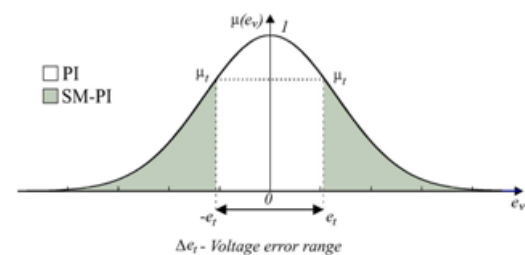


Fig. 5. Graph of the transition criterion μ .

2) DSM – P I Control Scheme:

The SM – P I con-troller has a decent execution amid the transient state however has an undesired reaction when the consistent state is come to. It is the gabbing began by the SMC exchanging laws utilized for figuring the controller picks up. This can be alleviated if the controller increases can be altered in relentless state (which brings about a standard P I controller). It can be gotten by utilizing a move principle in the controller structure. For this, consider a Gaussian capacity characterized as where μ is the choice variable to choose between the exchanging and settled controllers, evis the dc-join voltage mistake, and λ is the parameter of the Gaussian capacity.

Characterizing a scope of qualities around the reference voltage of the dc join, i.e., Δe_t , it is conceivable to figure the estimation of $\mu_t = \mu(e_t)$, from which the controller additions of SM – PI are settled (i.e., $k_p = k_{pv}$ and $k_i = k_{vi}$), as exhibited in Fig. 5. In this chart, the quality μ_t represents the limit identified with voltage blunder etwhere the controller move must happen. In this manner, the move acts as takes after: By utilizing (20), the estimation of $\mu(e_v)$ is constantly ascertained for every mistake voltage e_v . On the off chance that this worth is littler than μ_t , the actualized controller is the SM – PI; else, it is utilized a standard PI with antiwindup (controller SM – PI with settled increases). To make this move smooth, it is important to satisfactorily alter parameter λ .

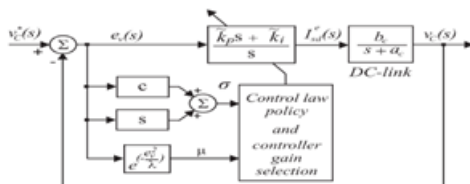


Fig. 6. Block diagram of the DSM–P I control scheme. The k_p and k_i gains updating policy is as follows: for $\mu(e_v) < \mu_t$, the gains change according to (23) and (24), and for $\mu(e_v) \geq \mu_t$, the gains are kept constant.

The block diagram of the proposed DSM–P I controller is shown in Fig. 6.

In which, the DSM–P I controller gains obtained from the sliding surface determined by blocks c and s.

3) Design Criteria of the DSM:

The configuration crite- rion utilized in this paper is situated in the shaft task that requires the arrangement of the Diophantine condition. Along these lines, consider the exchange elements of dc connection [see (3)] and the voltage controller DSM–P I [see (11)] can be composed where $A\eta^*(s)$ is a craved symphonious Hurwitz polynomial, and superscript $\eta \in \{fs(\text{fast}), av(\text{average}), sl(\text{slow})\}$ alludes to the execution criteria utilized for deciding coveted poly-nomials. Once the reasonable polynomials $A\eta^*(s)$ are characterized, the voltage controller parameters can be acquired from the arrangement of the Diophantine condition. The outline foundation first decides the moderate polynomial ($A sl^*(s)$) from the ostensible parameters of the plant [see (3)], considering the execution files of most extreme overshoot $M_p = 5\%$ and the damping coefficient of $\xi = 0.707$. In this manner, the accompanying polynomial can be acquired:

TABLE I: SYSTEM PARAMETERS

$k_p^+ = 0.033$	$k_p^- = 0.022$	$k_p^{av} = 0.11$
$k_i^+ = 2.145$	$k_i^- = 0.88$	$k_i^{av} = 2.75$
$c = 100$	$\lambda = 500$	$\mu_t = 0.98$

where $a_m^{sl} = 4/t_{ss(2\%)}^{sl}$, and $t_{ss(2\%)}^{sl} = t_{ss(2\%)}^n$ is the nominal settling time of system steady state. To determine the amplitudes of the switching laws given by (18) and (19), two other polynomials (i.e., $A^{av^*}(s)$ and $A^{fs^*}(s)$) are also defined, which correspond to a reduction of 40% and 62.5% of the nominal steady-state time ($t_{ss(2\%)}^{sl}$), respectively. Taking into account these three polynomials and solving the Diophantine equations for each case, the following gains can be obtained.

IV. EXPERIMENTAL EVALUATION OF THE PROPOSED SAP F:

The proposed control framework introduced in Fig. 4 has been tentatively assessed by utilizing a 10-kW three-stage dynamic force channel research facility

model. It is made by a three-stage power framework sustaining a nonlinear burden. The V SI is connected to the P CC by utilizing info channel inductors $L_f = 1.0$ mH. The dc connection is made by capacitors out of $2200 \mu\text{F}$ with an evaluated voltage of 410 V . The nonlinear burden is actualized by a three-stage rectifier, bolstering a RL load (i.e., $r_l = 40 \Omega$ and $l_l = 30$ mH). The subordinate of the heap current achieves 16.32 kA/s , with aggregate symphonious twisting ($\text{THD} = 21.5\%$) and a slacking power element of 0.89 . The proposed control framework was executed on a TMS28335 DSP stage. The A/D converters of the DSP card are associated with an estimation unit, created by Hall impact voltage and current sensors. The sign taken from these sensors goes through a first-arrange low-pass channel with cutoff recurrence of $\text{fLPF} = 2.5$ kHz for antialiasing purposes. The control calculation is actualized in C++ and executed with an inspecting time of $100 \mu\text{s}$. The SAP F parameters of the research facility model are given in Table I. Different conditions with hard transient and sudden load variations were considered in order to validate the theoretical studies developed in this manuscript. In addition, a comparison

The following scenarios were investigated: a) start-up charging the dc-link capacitor; b) transient of the dc-link reference voltage with both step-up and step-down variations; c) hard load transient variation by increasing and reducing the load power; d) unbalanced grid voltage; and finally e) reactive power compensation. The parameters of the DSM-P I controller employed in the experimental tests are presented in Table II.

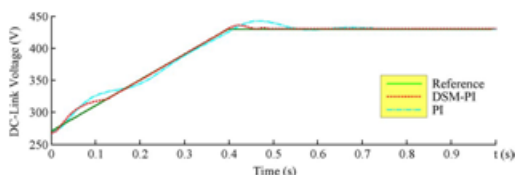


Fig. 7. Experimental result for dc-link voltage v_C during startup.

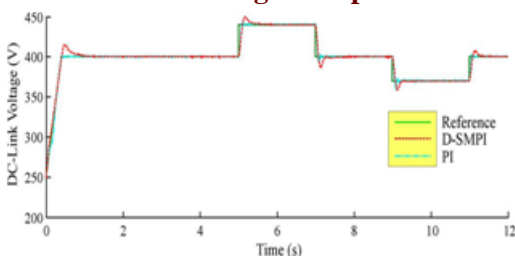


Fig. 8. Experimental result for dc-link voltage v_C during step transient of its reference voltage.

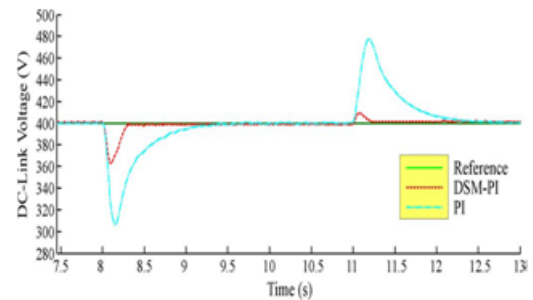


Fig. 9. Experimental result for dc-link voltage (v_C) during load transients.

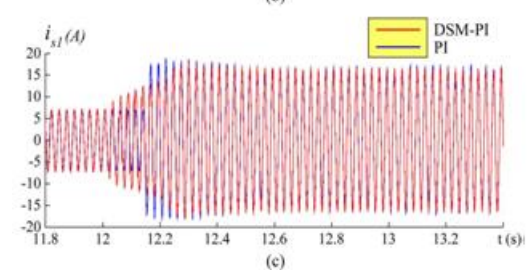
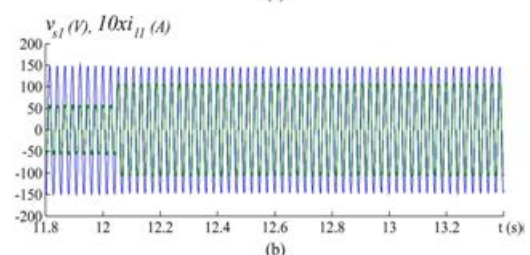
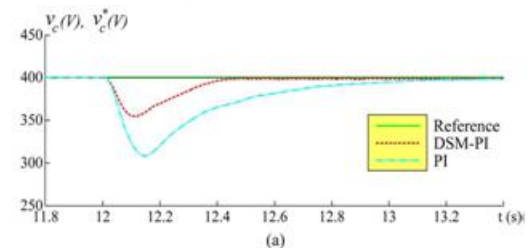


Fig. 10. Experimental result during load transients (a) for dc-link voltage v_C , (b) for source voltage v_{s1} and the load current i_{l1} multiplied by 10, and (c) for source current i_{s1} .

With a conventional P I controller was done to highlight the benefits of the proposed technique.

As aforementioned, the first test employed to verify and compare the controllers was the starting-up procedure for the dc-link voltage. Fig. 7 depicts the experimental outcome comparing both controllers following a reference ramp. Such a ramp waveform has a slope of 347 V/s. Notice in Fig. 7 that the performance of the proposed converter is smoother and the response time is smaller; the overshoot values of the proposed and conventional converters are given respectively by 0.53% and 4.37%. Although the comparison shown in Fig. 7 brings up the benefits of the DSM-P I strategy, additional tests have been considered to highlight its advantage under operating regimes

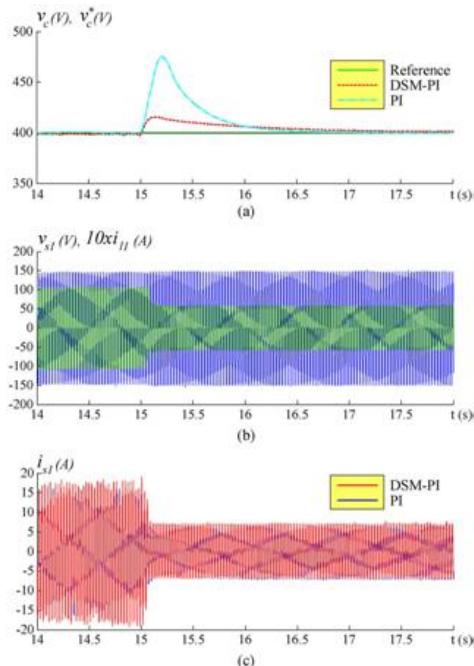


Fig. 11. Experimental result during load transients (a) for dc-link voltage v_c , (b) for source voltage v_{s1} and the load current i_{l1} multiplied by 10 times, and (c) for source current i_{s1} .

Case in point, Fig. 8 introduces a correlation for both controllers for varieties of the dc-join reference voltage. The proposed approach (DSM-P I) performed better for all progression homeless people (either venture up or venture down) introduced in this figure. A zoom of the transient at $t = 5$ s is displayed in Fig. 9, while Fig. 10 demonstrates a zoom of the progression

down transient at $t = 9$ s. Notwithstanding expecting that the outcomes displayed in Figs. 8–10 don't speak to a functional requirement for dynamic force channels, those outcomes are imperative figures of legitimacy to demonstrate the benefits of the proposed controllers. Then again, Figs. 11–13 demonstrate a run of the mill sort and ever-introduce transient in dynamic force channel applications, i.e., transitory of burden force. Two sorts of varieties are viewed as; the first (see Fig. 12) at $t = 12$ s demonstrates the heap power increment with an extra three-stage resistor (30Ω) associated in parallel with the plan of straight and nonlinear burdens. For this load transient, the parameters of the controllers are given as follows: 1) conventional P I, undershoot: 22.9% and accommodation time (2%): 0.84 s; and 2) proposed DSM-P I, undershoot: 11.35% and accommodation time (2%) 0.344 s. The DSM-P I controller also performs better than the conventional approach with load power reduction (see Fig. 13), as observed at $t = 15$ s. Such a transient was obtained by disconnecting the resistive load.

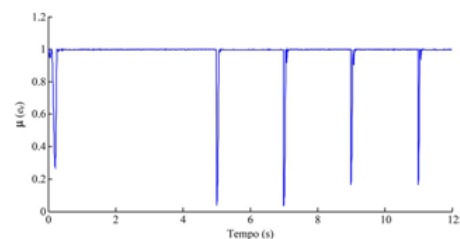


Fig. 12. Experimental result for function μ used for commutation between the controllers PI and DSM – PI.

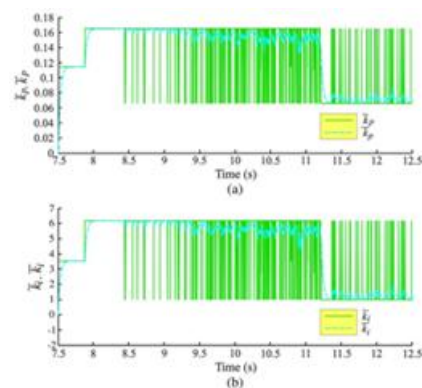


Fig.13. Experimental result (a) for switching proportional gain k_p and its average value k_p and

(b) for the switching integral gain k_i and its respective average value \bar{k}_i during load transient.

It is evident that the transition function of the proposed controller [see (20)] plays an important role to improve the performance of the dc-link voltage control. Fig. 14 shows the behavior of $\mu(e_v)$ for the results presented in Fig. 8. Fig. 15 shows, in turn, the gains behavior for the results in Fig. 11, in which switching gains of the controllers and their average values can be observed. Notice that they have been adjusted amid the load transient. Fig. 16 demonstrates another arrangement of test results to push the additions conduct through the start-up charging of the dc-link capacitor voltage. Figs. 17–19 demonstrate the oscilloscope screenshots with the results for the situation where unequal voltages were gotten at the network side, as saw in Fig. 17. Figs. 18 and 19 show burden and matrix streams, individually. Notice that notwithstanding accepting this case, the dynamic force channel with DSM-P I controller operates not surprisingly. This can be additionally watched when the THDs previously, then after the fact the remuneration are assessed, as appeared in the recurrence spectra of network stage current is1 introduced in Fig. 20. After the pay executed by the SAP F, the consonant mutilation is THD_{3.6%}.

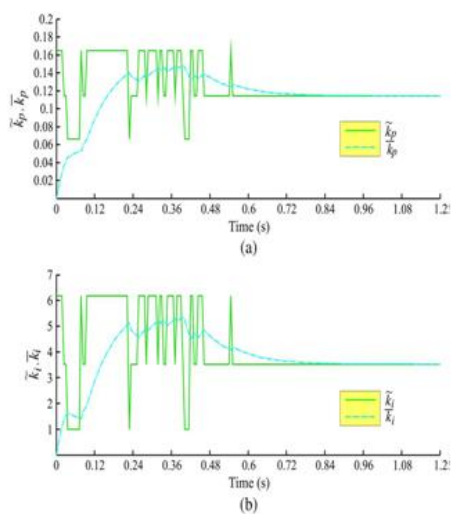


Fig.14.Experimental result (a) for switching proportional gain_ kpd and its average value kpd (b) for the switching integral gain _ki and its

respective average value \bar{k}_i during start-up charging of the dc-link capacitor.

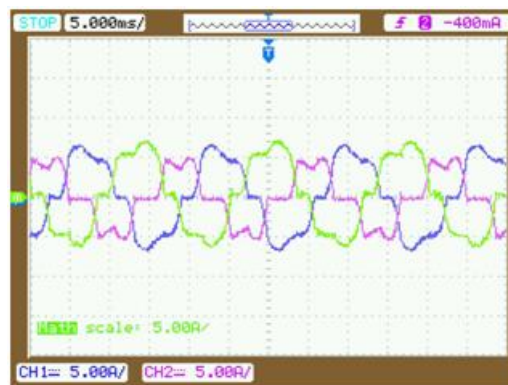


Fig. 15. Experimental results of the grid phase currents under unbalanced grid phase voltages before the compensation scheme.

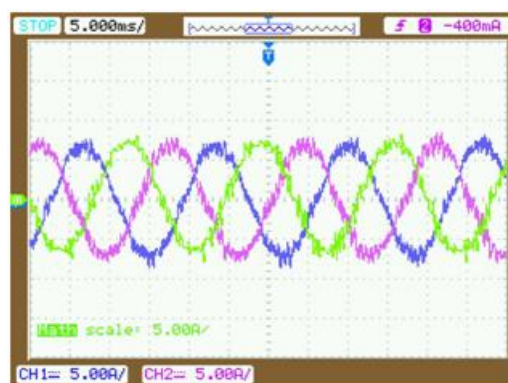


Fig. 16. Experimental result of the grid phase currents under unbalanced conditions of grid after the compensation scheme.

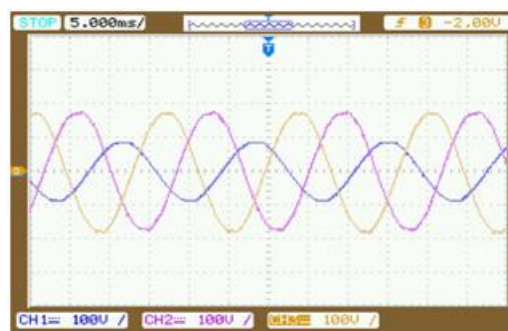


Fig. 17.Experimental result of unbalanced grid phase voltages.

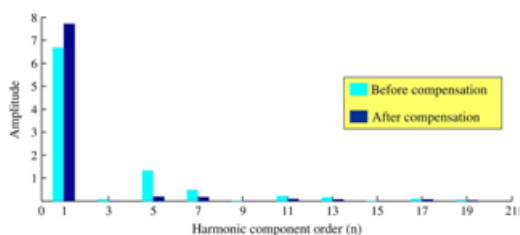


Fig. 18. Frequency spectra of the grid phase current i_{s1} before and after the compensation scheme.

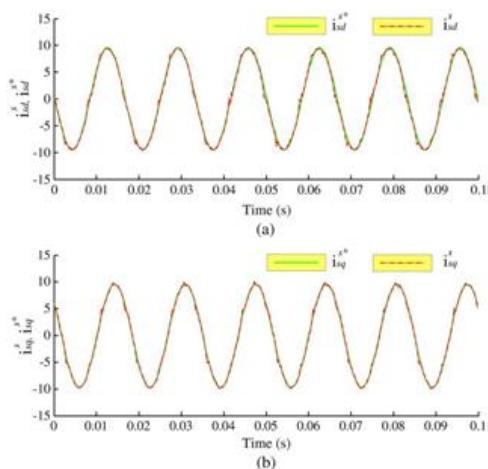


Fig. 19. Experimental result for the controlled current i_{sdq}^* in the dq reference frame.

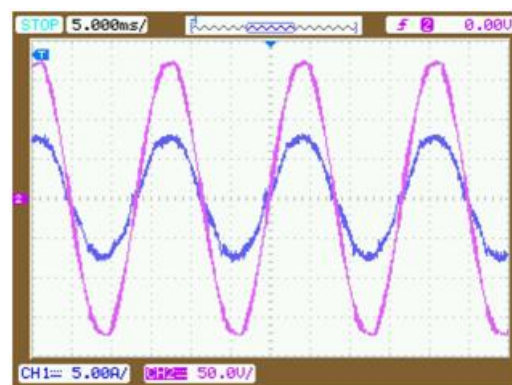


Fig. 21. Experimental result of the grid phase voltage v_{s1} superimposed by grid phase current i_{s1} after the compensation.

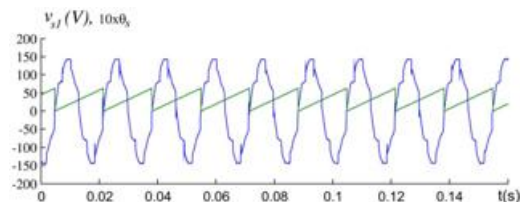


Fig. 22. Experimental result for distorted source voltage v_{s1} and the respective PLL angle.

Fig. 21 shows the steady-state results highlighting the current control actions with the measured dq currents following their reference. The performance of the SAP F when the reactive power is compensated can be verified in Figs. 22 and 23. Fig. 22 presents the experimental result of the grid phase voltage v_{s1}

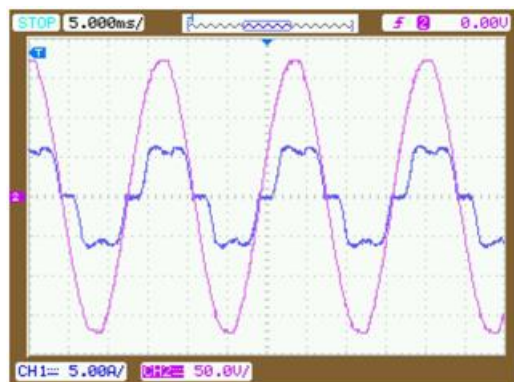


Fig. 20. Experimental result of the grid phase voltage v_{s1} superimposed by grid phase current i_{s1} before the compensation.

superimposed by its grid phase current i_{s1} before enabling the compensation scheme. Fig. 23 presents the same graphs when the compensation is effected by the SAP F. The last experimental result demonstrates that the reactive power demanded by the nonlinear load is full compensated. Figs. 24 and 25 present experimental results for the SAP F under distorted source voltage. In Fig. 24, it is possible to verify the source voltage V_{s1} and its respective PLL angle θ_s . Fig. 25 presents the source voltage v_{s1} and the respective source current i_{s1} before and after compensation imposed by SAP F.

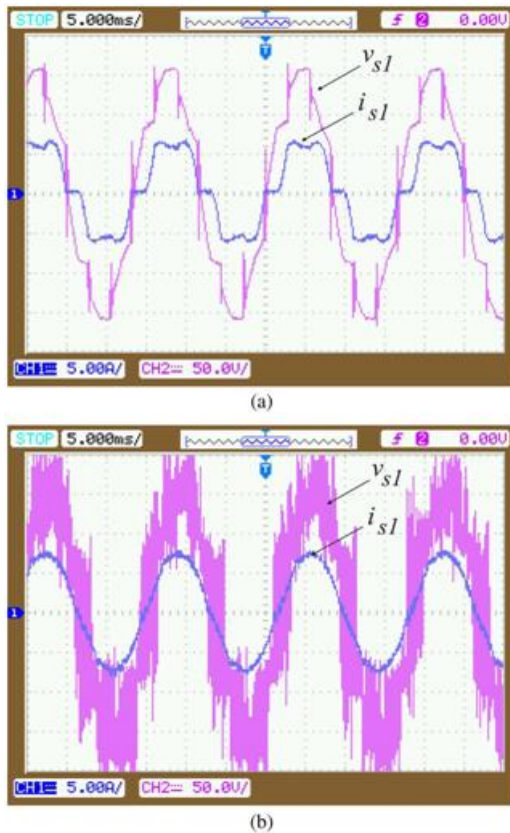


Fig. 23. Experimental result for distorted source voltage v_{s1} and the source current i_{s1} (a) before and (b) after SAP F compensation.

V. CONCLUSION:

Paper has proposed a control approach for enhancing the execution of SAP F without burden current estimations. In this control approach, the dc-link voltage is managed by a double control plan actualized by proportional-integral (P I) controller with the additions figured by utilizing a SMC approach. The babbling because of the SM can be alleviated by utilizing a move standard as a part of the controller structure. The hypothetical bases of the SM-P I was presented, and the strength evidence was displayed. In addition, the move plot that outcomes in DSM - P I was additionally talked about. With this control strategy, the execution of the dc-link control circle amid the heap varieties is upgraded. The stage streams of the force matrix are in a roundabout way directed by two free controllers (DSCs), in which the IMP is utilized to maintain a strategic distance from reference

outline transformations. This shows there are noteworthy increases in the SAP F in view of the BEBS since the present control strategy is less complex and the channel control technique is actualized with diminished number of current sensors. An extensive arrangement of test results exhibits the viability of the genius postured control technique notwithstanding amid framework load variety while giving all the while framework reactive power compensation and harmonic mitigation.

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