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Design & Implementation of DDFS Using VLSI Technology

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Abstract

CORDIC algorithms have long been used in digital signal processing for calculating trigonometric, hyperbolic, logarithmic and other transcendental functions. The algorithm requires only shift and add operations and this simplicity encourages its implementation in hardware. Traditional CORDIC architectures have focused on radix-2 implementations because of their higher accuracy. However these architectures are slow, requiring a lot of iterations to converge to a given solution. Radix-4 and higher radix architectures have been proposed to speed up the process by reducing the number of iterations, but they suffer from poor accuracy. In this paper a hybrid-radix approach to CORDIC implementation is proposed. By using this approach the algorithm can be implemented with higher speed, lower power and lesser area utilization and at the same time a good accuracy can be achieved. Further the hybrid-radix architecture has been retimed resulting in an increase in the overall throughput which is particularly important in DSP applications.

Keywords: ***CORDIC, DSP, Hybrid arithmetic, VLSI, Retiming, Unfolded structures, Folded Structures.***

INTRODUCTION

A Software Defined Radio (SDR) is defined as a radio in which the receive digitization is performed at some stage downstream from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages - with a reverse process occurring for the transmit digitization. In an SDR, Digital Signal Processing in flexible and reconfigurable functional blocks define the characteristics of the radio. As technology progresses, an SDR can move to an almost total Software Radio (SR), where the digitization is at (or very near to) the antenna and all of the processing required for the radio is performed by software residing in high-speed digital signal processing elements. The SDR will occur in the near term, migrating to the SR in the longer term, subject to the progression of core technologies. The need for such progression will be a function of the application. For example, a base station application may require and/or be able by virtue of technology advances and design latitude to move to an SR. But a handset or portable terminal, because of numerous constraints, may not need or be able to progress beyond an SDR.

Existedcordic (CO-ordinate Rotation Digital Computer) [1] [2] is a simple shift and add algorithm that has been used in Digital Signal Processing (DSP) systems [3] for calculating various linear and transcendental functions. Conventional implementations of CORDIC have been software oriented.However, the development in the design of high speed Very Large Scale Integration (VLSI) architectures has provided the designers with significant impetus to map the algorithm into architecture [4]. This has enabled the designers to assess the performance in terms of some realistic parameters like throughput, area and power.Typically, CORDIC algorithm has been implemented as a sequential structure [5]. This implementation, although area efficient has large iteration periods and is not, therefore, preferred for DSP applications. Sequential structures have been used for Application Specific

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Integrated Circuits (ASIC) implementations where area is of concern.

However, with Field Programmable Gate Arrays (FPGAs) the underlying platform provides a huge logic capacity [6] [7] [8] [9] that can be utilized to develop architectures that are optimized for speed and power. This has enabled designers to exploit the concurrencies [10] within the algorithm and develop unfolded architectures that map well on FPGAs [11] [12]. The unfolding process results in parallel structures where each processing element performs the same iteration.

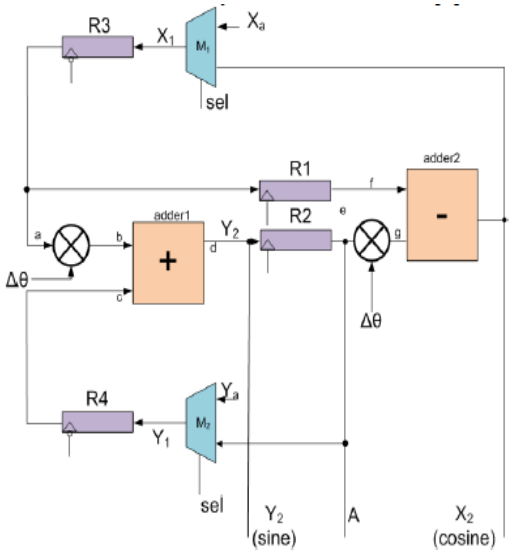

Fig-1: Architecture proposed

This work contains simulation and Verilog HDL implementation of OFDM based transmitter and receiver system. After floating point simulation of the framework, Verilog HDL has been used for fixed point simulation and description of hardware details. The transmitter first converts the input data from a serial stream to parallel sets. Each set of data contains one information bit for each carrier frequency. Then, parallel data are modulated to the orthogonal carrier frequencies. The IFFT converts the parallel data into time domain waveforms. Finally, these waveforms are combined to create a single time domain signal for transmission.

DIRECT DIGITAL FREQUENCY SYNTHESIS (DDFS):

The DUC is a digital circuit which implements the conversion of a complex digital baseband signal to a real pass band signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The Digital Down Converter (DDC) is the counter-part on the receiver end. The detailed description on DUC and DDC can be found in [25][26]. This section focuses on the efficient hardware implementation of DDFS, which is backbone of the DUC and DDC.*Mathematical Representation*.Based on the differential relationship between Sine and Cosine
i.e.

$$\frac{d}{d\theta}(\sin\theta) = \cos\theta$$

And

$$\frac{d}{d\theta}(\cos\theta) = -\sin\theta$$

Khan et al. [23] has suggested the equation (3) and (4), and then proposed the architecture, as shown in Fig. 1.

$$Y_c = Y_p + \Delta\theta X_p$$

The existed architecture for VLSI implementation of the DDFS is shown in Fig. 7.

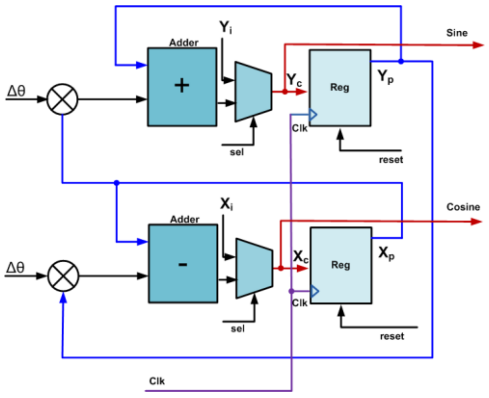

Fig-2 The Proposed Architecture for DDFS

This architecture utilizes two adders, two multiplexers, two multipliers and two registers. The presentation is general and applicable to any bit length. The data path elements are 32 bits wide. As compared to the architecture proposed in [23], the required number of

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registers has been reduced to two, instead of four. Depending upon the number of bits used, it results in considerable reduction of hardware resources. Initially ***Yi*** and ***Xi*** are fed to the Registers because ***sel*** is 1. On the next positive edge of ***clk***, these seed values are used to compute the values of Sine and Cosine. After the first clock cycle, ***sel*** is 0 and now the multiplexers only act as simple wires for rest of the clock cycles.

The previous value of Cosine is multiplied by $\Delta\theta$ and added with the previous value of Sine to generate the current value of Sine, ***Yc***. Similarly, the previous value of Sine, ***Yp*** is multiplied by $\Delta\theta$ and subtracted from the previous value of Cosine, ***Xp*** to generate the current value of Cosine, ***Xc***.

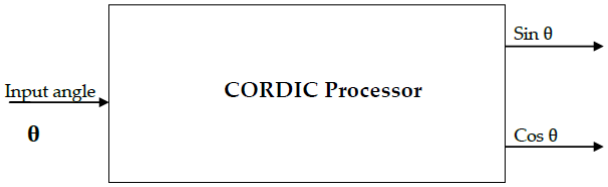
CORDIC ALGORITHM

The basic functions such as trigonometric, inverse trigonometric, logarithmic, exponential, multiplication and division functions are used in many of the DSP algorithms [1] some of the software solutions are the traditional approach to implement these functions. The exploitation of look-up tables, power series includes in software solutions, however they suffered from huge drawbacks. Although Look-up tables are fast they require hefty amount of memory for high precision results. To achieve desired precision the use of power series was time consuming as it was too slow.

One of the digital signal processing algorithms is CORDIC, it came into existence to present efficient hardware solutions [2]. x sin ø + y cos ø = y' (1)
x cos ø - y sin ø = x' (2)

This Cartesian plane rotates by the angle ø, as shown in Figure 1.
The above equations can readjust as:
[y + x tan ø] cos ø = y' (3)
[x - y tan ø] cos ø = x' (4)

The CORDIC algorithm provides an iterative approach that involves the rotation of a vector in a linear, circular or hyperbolic coordinate system [1].



The choice of coordinate system depends on the function to be evaluated [4]. The vector rotations are performed using a series of specific incremental rotation angles. The rotation angles are restricted so that;

$$\tan\theta = \pm 2^{-i}$$

This ensures that the multiplication operation is decomposed into simple shift operation such that the algorithm involves only shift and add operations. The generalized equations for CORDIC algorithm when operated in circular coordinate system are:

$$x_{i+1} = x_i - \sigma_i y_i p^{-i}$$
$$y_{i+1} = y_i - \sigma_i x_i p^{-i}$$
$$z_{i+1} = z_i - \sigma_i \alpha_i$$

Where σ_i represents the direction of rotation in each iteration, ρ represents the radix of the number system and α_i gives the amount of shift in each iteration. The iteration process increases the length of the vector in each iteration. The magnitude of the rotating vector in (i+1)th iteration is given as structure will become slow.

PROPOSED ARCITECTURE

In proposed architecture we implemented parallel unfolded CORDIC architecture . which is a multiple bit. The advantage of this design is it acts in parallel nature based on swapping bcause of this swappings the power consumption and power dissipation will gets reduced so that delay will gets decreases and efficiency increases.

Here, in order to overcome the constraints in existed we came to implement this design (area,delay, power,efficiency).Here, swapping of bits means if it contains two stages means the first stage input is given to the second stage as another input and the second stage input is given to the first stage as the

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another input.so, because of this based on shiftings i.e, one shift, two shift, three shift, four shift..the clock pulses will gets reduced for the bits because it generates intermediate patterns so that low power will get generated and delay gets reduces so that efficiency increases.

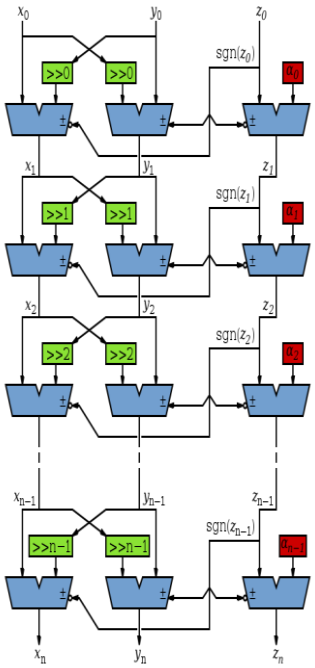


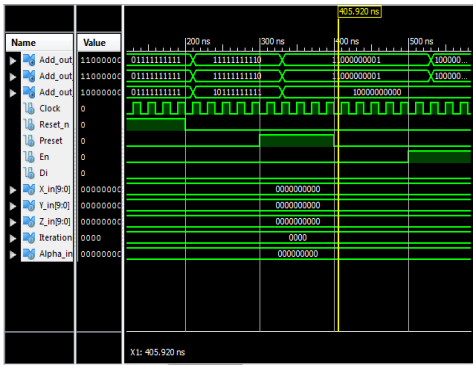
Fig-3: Parallel unfolded cordic architecture

Here we have to compare the area, delay, power and efficiency between the existed and this proposed methods in order to prove which one is efficient even though bit length increases.

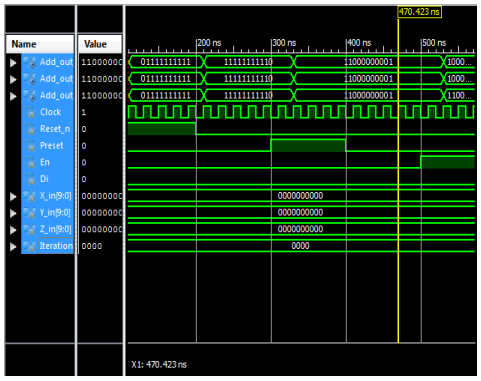
RESULTS

Simulation Results:

Unfolded Simulation Waveform:



Folded CORDIC Waveform:



Synthesis Report:

Unfolded Area Report:

```
Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              86  out of  18224     0%
 Number of Slice LUTs:                  256  out of   9112     2%
    Number used as Logic:               256  out of   9112     2%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    259
   Number with an unused Flip Flop:     173  out of    259    66%
   Number with an unused LUT:             3  out of    259     1%
   Number of fully used LUT-FF pairs:    83  out of    259    32%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                          81
 Number of bonded IOBs:                  81  out of    232    34%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%
```

Folded CORDIC Area Report:

```
Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              97  out of  18224     0%
 Number of Slice LUTs:                  273  out of   9112     2%
    Number used as Logic:               273  out of   9112     2%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    276
   Number with an unused Flip Flop:     179  out of    276    64%
   Number with an unused LUT:             3  out of    276     1%
   Number of fully used LUT-FF pairs:    94  out of    276    34%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                          72
 Number of bonded IOBs:                  72  out of    232    31%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%
```

Unfolded CORDIC Timing Report:

```
Timing Summary:
---------------

Speed Grade: -3

   Minimum period: 4.115ns (Maximum Frequency: 243.013MHz)
   Minimum input arrival time before clock: 5.094ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found
```

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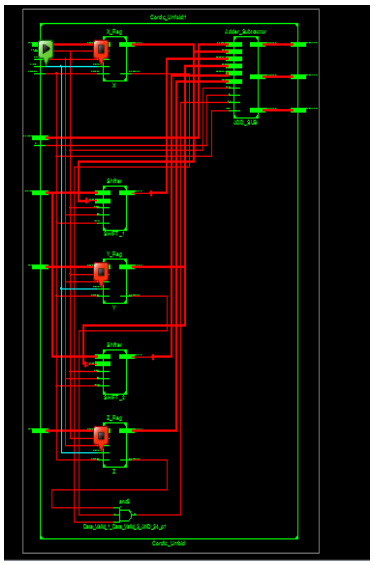
Folded CORDIC Timing Report:

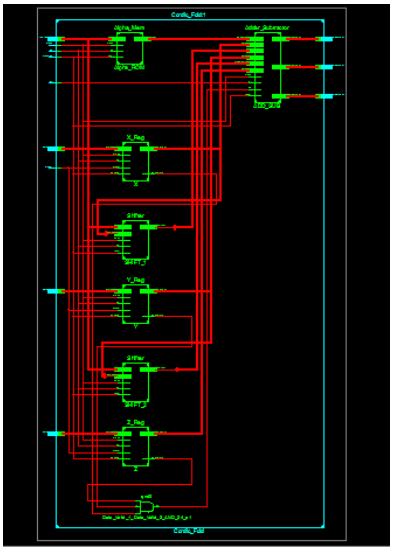
```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.999ns (Maximum Frequency: 250.091MHz)
   Minimum input arrival time before clock: 5.352ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found
```

Unfolded CORDIC RTL Schematic:



Folded CORDIC RTL Schematic:



CONCLUSION

Here, in this paper the design and implementation of both Folded and Unfolded CORDIC structures using hybrid-radix arithmetic is done. The implemented structures were compared in terms of area, speed, power and accuracy of the simulated results.CORDIC is a powerful algorithm, and a popular algorithm of choice when it comes to various Digital Signal Processing applications. Implementation of a CORDIC-based processor on FPGA gives us a powerful mechanism of implementing complex computations on a platform that provides a lot of resources and flexibility at a relatively lesser cost. Further, since the algorithm is simple and efficient the design and VLSI implementation of a CORDIC based processor is easily achievable. In this project a CORDIC module is designed and simulated using Xilinx ISE using Verilog as a synthesis tool. The output of the CORDIC core is analyzed and verified on the test-bench. The device utilization summary showed that minimum resources were consumed.

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