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Implementation of LTE Systems using FIFO

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Abstract:
Focuses on Design and Implementation of Long Term Evolution (LTE) front end modules to synchronize time and frequency with the help of Fast Fourier Transform (FFT). LTE is an emerging standard for high-speed wireless communications.The synchronizer proves to have an outstanding performance with less delay time with simple circuitry for all defined communication modes in LTE.

Existing Method:
Synchronizer is used when two systems operate in different frequencies. As a design FFT works on parallel data and inputs will be in terms of serial-data. Therefore we need to convert serial data into parallel data to the input of FFT. External Input frequency, design input frequency and output frequency are synchronized by using reset, preset and enables. If frequency variation is high, it really makes complex to design with SIPO and PISO.

Proposed System:
In this system, we proposed to use FIFO based synchronizer for LTE network. In this design FFT works on post-FIFO data and inputs will be in terms of pre-FIFO data. There is no essential for converting the input data frequency into the other form of data to the input of FFT. External Input frequency, design input frequency and output frequency are synchronized by using pre-clock, clock and post-clock. If variation is high, it will be possible by using pre-FIFO and post-FIFO. The following difficulties are attempted to be addressed during this project work:

- Reducing circuit complexity.
- Replacing the SIPO/PISO Synchronizer modules with FIFO Synchronizer.
- Design of modules like FIFO synchronizer that generates necessary timing needed for interfacing to FFT.
- Reducing the of delay data processing.

Keywords:
LTE, Synchronizer, SIPO, PISO, FFT, FIFO

I. INTRODUCTION

1.1 An Introduction to LTE

Mobile broadband is becoming a reality as Internet generation accustomed to access broadband wherever they go, mobile broadband, instead of only at home and in the office, has become a reality. Therefore, the Global System for Mobile Communications family constantly develops new mobile technologies to achieve better performance, such as higher speed, larger capacity and so forth. LTE is a step beyond 3G and towards the 4G Evolution. The contributions of LTE make sure that the users are able to request more mobile applications like interactive TV, mobile video blogging, advanced games or professional services.

Long Term Evolution (LTE) is a significant project of 3rd Generation Partnership Project (3GPP), initially proposed on the Toronto conference of 3GPP in 2004 and officially started as LTE work item in 2006. LTE, as a transition from the 3rd generation (3G) to the 4th generation (4G), has achieved great capacity and high speed of mobile telephone networks without doubt. In addition, it is combined with top-of-the-line radio techniques in order to gain better performance than Code Division Multiple Access (CDMA) approaches. LTE provides scalable carrier bandwidths from 1.4 MHz to 20 MHz and frequency division duplexing (FDD), as well as time division duplexing (TDD).

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LTE is composed of many new technologies compared with the previous generation of cellular systems. These new technologies are

1. **OFDM** (Orthogonal Frequency Division Multiplex: In order to gain high data bandwidth when transmitting packets, LTE integrates OFDM technology which can provide high-degree resilience to reflections and interference at the same time.
2. **MIMO** (Multiple Input Multiple Output): MIMO operations include spatial multiplexing as well as pre-coding and transmit diversity. These operations addressed the problems of multiple signals arising from many reflections, which were encountered by previous telecommunications systems.

1.2 An Introduction to Synchronizer

Synchronizer is used when two designs operate in different frequencies. The synchronizer allows the transfer of wide vectors across clock domain with minimal timing requirements and no meta-stability issues. This block ensures that there is no metastability for a target MTBF i.e., Mean Time between Failures.

How do I synchronize the system?

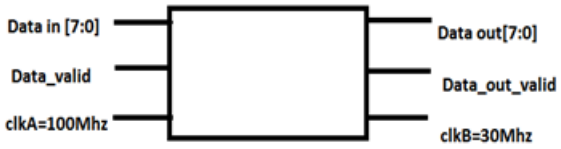

Figure 1: Example for simple synchronizer

General Definition: process of precisely coordinating or matching two or more activities, devices, or processes in time. Computing Definition: process of making two or more data storage devices or programs (in same or different computers) having exactly the same information at a given time. Asynchronous signals are those that run from different clocks or at a different transition rate.

II. EXISTING SYNCHRONIZER METHOD

In this system a design FFT works on parallel data and inputs will comes in terms of serial-data. Therefore we need to convert serial data into parallel data to the input of FFT. Input frequency, design input frequency and output frequency are synchronized by using reset, preset and enables. If variation will be high, it is not possible to do using SIPO and PISO.

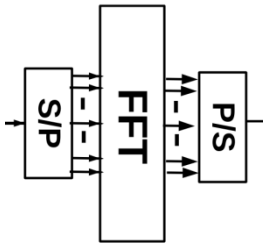

Figure 2: Existing synchronizer using Serial-In-Parallel-Out and Parallel-in-Serial-out

This design is having certain limitations.
They are
-Frequency variation is high, it is not possible to process data.
-Complex circuitry.
-Delay will be high.

1.1 Serial-in to Parallel-out (SIPO) Shift Register

The operation is as follows. Lets assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level "0" ie, no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

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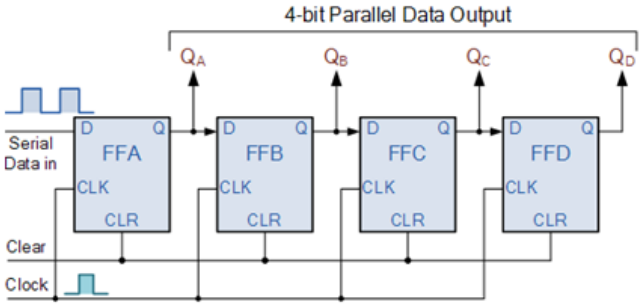
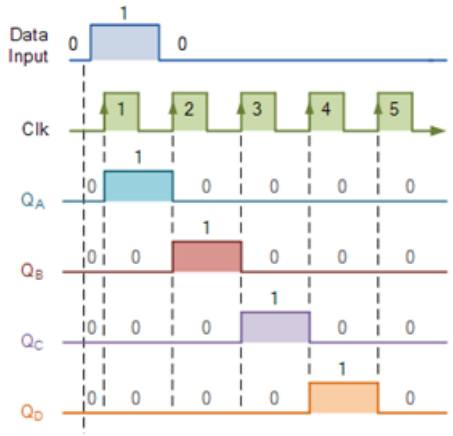


Figure 3: Serial-in Parallel Out

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and Q_B HIGH to logic "1" as its input D has the logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_A. When the third clock pulse arrives this logic "1" value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of $Q_A$to Q_D. Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from left to right as follows.

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0



Note that after the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic "1" and "0".

1.2. Parallel-in to Serial-out (PISO) Shift Register

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present atP_A to P_D. This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

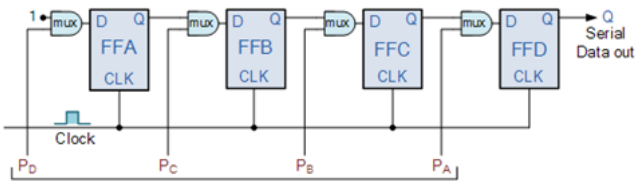


Figure 4: Parallel-in Serial Out

As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial DATA stream which can be sent directly to a computer or transmitted over a communications line.

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III. PROPOSED SYNCHRONIZER METHOD

In this system, we proposed to use FIFO based synchronizer for LTE network. In this design FFT works on post-FIFO data and inputs will be in terms of pre-FIFO data. There is no essential for converting the input data frequency into the other form of data to the input of FFT. External Input frequency, design input frequency and output frequency are synchronized by using pre-clock, clock and post-clock. If variation is high, it will be possible by using pre-FIFO and post-FIFO.

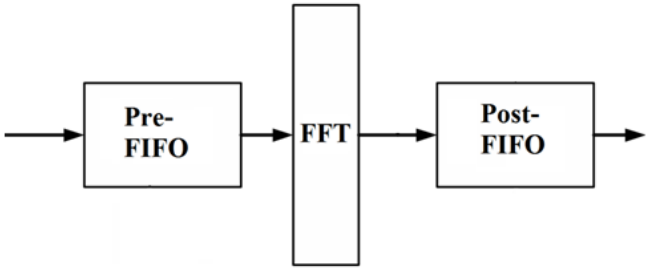


Figure 5: Proposed synchronizer using Pre-FIFO and POST-FIFO

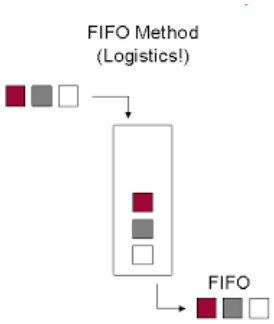
The following difficulties are attempted to be addressed during this project work:

- Reducing circuit complexity.
- Replacing the SIPO/PISO Synchronizer modules with FIFO Synchronizer.
- Design of modules like FIFO synchronizer that generates necessary timing needed for interfacing to FFT.
- Reducing the of delay data processing.

Fist in First Out:

FIFOs are commonly used in electronic circuits for buffering and flow control between hardware and software. In its hardware form, a FIFO primarily consists of a set of read and write pointers, storage and control logic. Storage may be SRAM, flip-flops, latches or any other suitable form of storage. For FIFOs of non-trivial size, a dual-port SRAM is usually used, where one port is dedicated to writing and the other to reading.

A synchronous FIFO is a FIFO where the same clock is used for both reading and writing. An asynchronous FIFO uses different clocks for reading and writing. Asynchronous FIFOs introduce metastability issues. A common implementation of an asynchronous FIFO uses a Gray code (or any unit distance code) for the read and write pointers to ensure reliable flag generation. One further note concerning flag generation is that one must necessarily use pointer arithmetic to generate flags for asynchronous FIFO implementations. Conversely, one may use either a "leaky bucket" approach or pointer arithmetic to generate flags in synchronous FIFO implementations.



First-In, First-Out (FIFO) is one of the methods commonly used to calculate the value of inventory on hand at the end of an accounting period and the cost of goods sold during the period. This method assumes that inventory purchased or manufactured first is sold first and newer inventory remains unsold. Thus cost of older inventory is assigned to cost of goods sold and that of newer inventory is assigned to ending inventory. The actual flow of inventory may not exactly match the first-in, first-out pattern.

The proposed architecture is shown in Fig where the main steps of synchronization in LTE are implemented. In the pre-FFT blocks, coarse time and frequency synchronization is performed where the symbol timing is detected, CP type is recognized and fractional CFO is estimated and compensated in a loop with an adaptive coefficient (at). This loop consists of a first-order filter, sine and cosine estimator, and a complex multiplier.

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As the coarse time synchronization finishes, the CP length and the CP location are known and the CP could be easily removed. Therefore, symbols can pass through the FFT block to enter the post-FFT domain. In the post-FFT domain, the cell search block determines the cell ID as well as the integer CFO and the frame timing through the detection and analysis of the PSS and SSS signals. Moreover, the PSS is detected simultaneously with the coarse frequency synchronization. This concurrency is safe as the PSS detection technique is not affected by the presence of the fractional CFO. By detecting the PSS, the SSS signal is also located and can be analyzed. The last step of the synchronization is frequency tracking. For this aim, the CFO estimation block estimates the residual CFO with a high accuracy, then the estimated error is compensated in the post-FFT domain through the selected loop in Section VI. This architecture is explained in detail in the following sections.

III. IMPLEMENTATION RESULTS

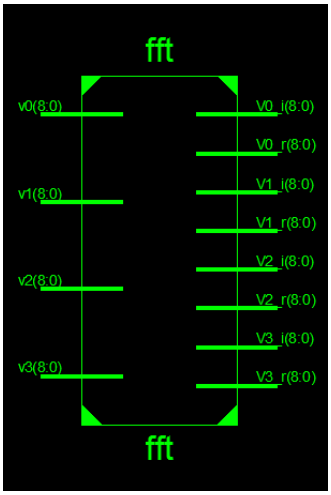

Fig.7. Block Diagram for FFT

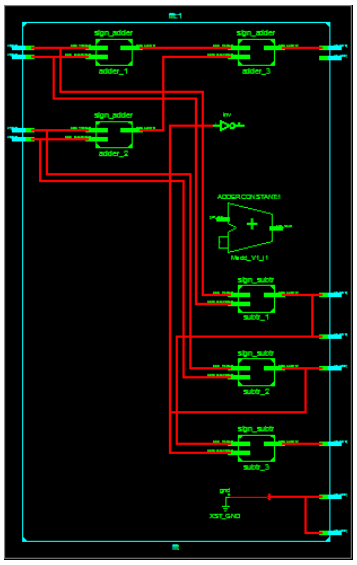

Fig.8. RTL Schematic for FFT

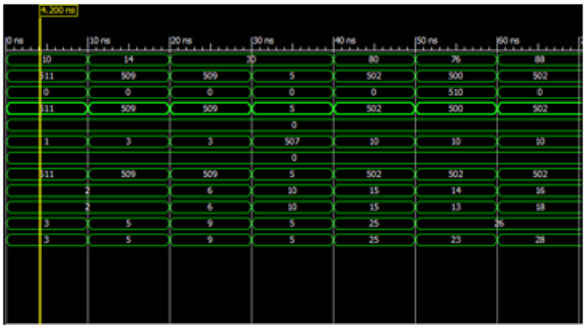

Fig. 9. Simulation for FFT

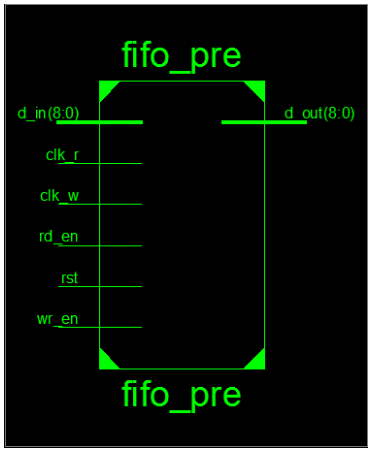

Fig.10. Block Diagram for Pre-FIFO

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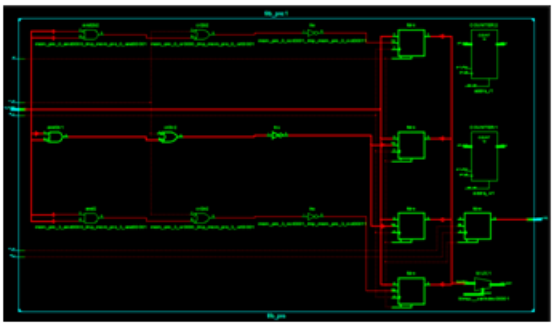

Fig.11. RTL Schematic for Pre-FIFO

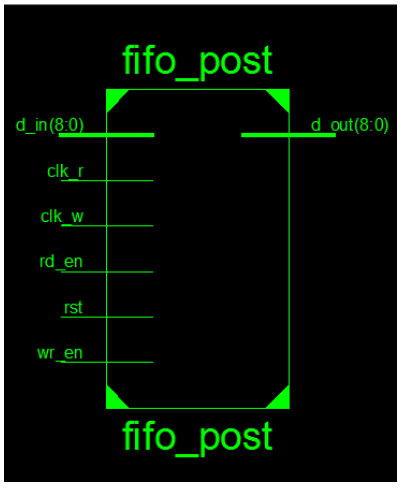

Fig.12. Block Diagram for Post-FIFO

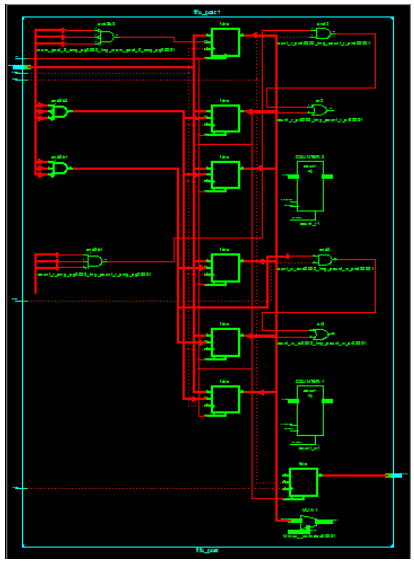

Fig.13. RTL Schematic for Post-FIFO

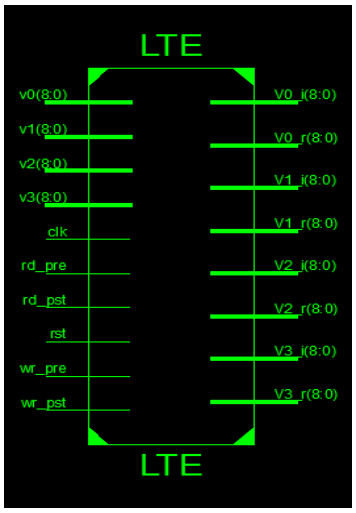

Fig.14. Block Diagram for LTE

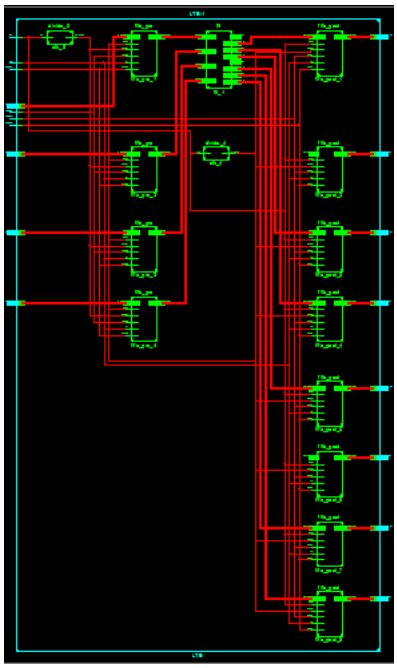

Fig.15. RTL Schematic for LTE

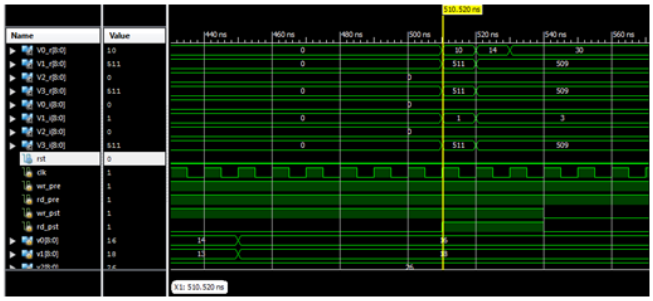

Fig.16. Simulation for LTE

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REFERENCES:

[1]Technical Specification Group Radio Access Network; Requirements for Further Advancements for Evolved Universal Terrestrial Radio Access (E-UTRA)(LTE-Advanced) (Release 9), 3GPP TR 36.913 V9.0.0, Dec. 2009.

[2]P.-Y. Tsai and H.-W. Chang, "A new cell search scheme in 3GPP long term evolution downlink, OFDMA systems," in Proc. IEEE WCSP, Nov. 2009, pp. 1–5.

[3]K. Manolakis, D. M. Gutierrez Estevez, V. Jungnickel, W. Xu, and C. Drewes, "A closed concept for synchronization and cell search in 3GPP LTE systems," in Proc. IEEE WCNC, Apr. 2009, pp. 1–6.

[4] M. J. Shim, J. S. Han, H. J. Roh, and H. J. Choi, "A frequency synchronization method for 3GPP LTE OFDMA system in TDD mode," in Proc. 9th IEEE ISCIT, Sep. 2009, pp. 864–868.

[5]C.-C. Lee, C.-F. Liao, C.-M. Chen, and Y.-H. Huang, "Design of 4 × 4 MIMO-OFDMA receiver with precode codebook search for 3GPP-LTE," in Proc. IEEE ISCAS, May/Jun. 2010, pp. 3957–3960.

[6]C.-W. Chu, C.-C. Lee, and Y.-H. Huang, "Design of an OFDMA baseband receiver for 3GPP long-term evolution," in Proc. IEEE VLSI-DAT, Apr. 2008, pp. 196–199.

[7]N. Ding, C. Chen, W. Fan, Y. Chen, and X. Zeng, "An improved coarse synchronization scheme in 3GPP LTE downlink OFDM systems," in Proc. IEEE ISCAS, May 2012, pp. 1516–1519.

[8] W. Xu and K. Manolakis, "Robust synchronization for 3GPP LTE system," in Proc. IEEE GLOBECOM, Dec. 2010, pp. 1–5.

[9] I. Diaz, L. Wilhelmsson, J. Rodrigues, J. Lofgren, T. Olsson, and V. Öwall, "A sign-bit auto-correlation architecture for fractional frequency offset estimation in OFDM," in Proc. IEEE ISCAS, May/Jun. 2010, pp. 3765–3768.

[10]Y. Kim and K. Chang, "Complexity optimized CP length pre-decision metric for cell searcher in the downlink of 3GPP LTE system," in Proc. IEEE 20th Personal, Indoor Mobile Radio Commun., Sep. 2009, pp. 895–899.

[11]J. I. Mazarico, V. Capdevielle, A. Feki, and V. Kumar, "Detection of synchronization signals in reuse-1 LTE networks," in Proc. 2nd IEEE WD, Dec. 2009, pp. 1–5.

[12]Y.-C. Lin, S.-L. Su, and Y.-J. Fan, "Joint sector ID and ICFO detection by using partial correlation scheme in LTE cell search process," Wireless Personal Commun., vol. 70, no. 4, pp. 1603–1621, 2013.

[13]C. Ma, H. Cao, and P. Lin, "A low-power low-cost design of primary synchronization signal detection," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 7, pp. 1161–1166, Jul. 2012.

[14]A. Golnari, G. Sharifan, Y. Amini, and M. Shabany, "A low complexity architecture for the cell search applied to the LTE systems," in Proc. 19th IEEE ICECS, Dec. 2012, pp. 300–303.

[15]B. M. Popovic, "Generalized chirp-like polyphase sequences with optimum correlation properties," IEEE Trans. Inf. Theory, vol. 38, no. 4, pp. 1406–1409, Jul. 1992.

[16]F. Wang, Y. Zhu, and Z. Wang, "A low complexity scheme for S-SCH detection in 3GPP LTE downlink system," in Proc. IEEE GMC, Oct. 2010, pp. 1–6.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[17] M. Speth, S. A. Fechtel, G. Fock, and H. Meyr, "Optimum receiver design for wireless broad-band systems using OFDM. I," IEEE Trans. Commun., vol. 47, no. 11, pp. 1668–1677, Nov. 1999.

[18]J. González-Bayón, C. Carreras, and A. Fernández-Herrero, "Comparative evaluation of carrier frequency offset tracking schemes for WiMAX OFDM systems," in Proc. IEEE ISSPIT, Dec. 2007, pp. 479–484.

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