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Implementation of an Efficient Multiplier Using Adaptive Hold Logic

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ABSTRACT:
Digital multipliers are among the most critical arithmetic functional units. The overall performance of these-systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occur swhen a pMOS transistor is under negative bias (Vgs = −Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature in-stability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- orrow-bypassing multiplier.

I.INTRODUCTION:
Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The through put of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (Vgs = −Vdd).

In this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaks the Si–H bond generated during theoxidation process, generating H or H2 molecules. When these molecules diffuse away, interface traps are left[1]. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (Vth),reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTIeffect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and Vth is increased in the long term. Hence, it is important to design a reliable high-performance multiplier. The corresponding effecton an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/ polygate transistors, and therefore is usually ignored.

However, for high-k/metal-gate nMOS transistors with significant charge trapping, the PBTI effect cannot longer be ignored. In fact, it has been shown that the PBTI effect is more significant than the NBTI effect on 32-n-mhigh-k/metal-gate processes [2]–[4]. A traditional method to mitigate the aging effect is overdesign, including such things as guard-banding and gate oversizing; however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI-aware methodologies have been proposed.An NBTI-aware technology mapping technique was proposed in [7] to guarantee the performance of the circuit during its lifetime.

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In [8],an NBTI-aware sleep transistor was de-signed to reduce the aging effects onpMOS sleep-tran-sistors, and the mlifetime stability of the power-gated circuits under consideration was improved. Wu and-Marculescu [9] proposed a point logic restructuring and pin reordering method, which is based on detecting functional symmetries and transistor stacking effects. They also proposed an NBTI optimization method that considered pathsensitization. [12]. In [10] and [11],dynamic voltage scal-ing and body-basing techniques were proposed to reduce power or extend circuit life.These techniques, however, require circuit modification or do not provide optimization of specific circuits.

Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. How-ever, theprobability that the critical paths are activated is low. In most cases, the path delay is shorter than the critical path. For thesenoncritical paths, using the criti-cal path delay as the overall cycle period will result in significant timing waste. Hence, thevariable-latency design was proposed to reduce the timing waste of traditional circuits. The variable-latency design di-videsthe circuit into two parts: 1) shorter paths and 2) longer paths. Shorter paths can execute correctly in one cycle, whereaslonger paths need two cycles to execute. When shorter paths are activated frequently, the average latency of variable a tencydesigns is better than that of traditional designs.

For example, several variable-latency adders were proposed usingthe spec-ulation technique with error detection and recovery [13]–[15]. A short path activation function algorithm was proposed in [16] to improve the accuracy of the hold logic and to op-timize the performance of the variable-latency circuit. An instruction scheduling algorithm was proposed in to schedule the operations on non uniform latency func-tional units and improve the performance of Very Long Instruction Word processors. In a variable-latency pipe-lined multiplier architecture with a Booth algorithm was proposed.

In process-variation tolerant architec-ture for arithmetic units was proposed, where the ef-fect ofprocess-variation is considered to increase the circuit yield. In addition, the critical paths are divided into two short-er pathsthat could be unequal and the clock cycle is set to the delay of the longer one. These research designs were able to reducethe timing waste of traditional cir-cuits to improve performance, but they did not consid-er the aging effect and could notadjust themselves dur-ing the runtime. A variable-latency adder design that considers the aging effect was proposed.However, no variable-latency multiplier design that considers the ag-ing effect and can adjust dynamically has been done.

II.PAPER CONTRIBUTION:

In this paper, we propose an aging-aware reliable multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve re-liable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are sum-marized as follows: 1) novelvariable-latency multiplier architecture with an AHL circuit. The AHL circuit can decide whether the input patterns requireone or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation aftercon-siderable aging occurs; 2) comprehensive analysis and comparison of the multiplier's performance under dif-ferent cycleperiods to show the effectiveness of our proposed architecture; 3) an aging-aware reliable mul-tiplier design method that issuitable for large multipli-ers. Although the experiment is performed in 16- and 32-bit multipliers, our proposed architecturecan be easily extended to large designs.

III.PRELIMINARIES:

Row-Bypassing Multiplier:

A low-power row-bypassing multiplier is also pro-posed to reduce the activity power of the AM. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing

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multiplier, but the selector of themultiplexers and the tristate gates use the multiplicator.

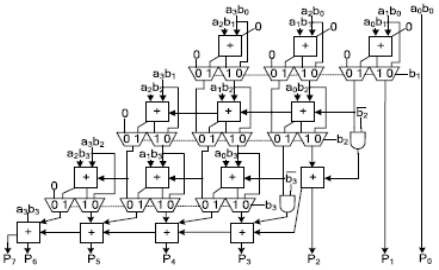

Figure 1 : 4 × 4 Row-Bypassing Muliplier

Fig. 1 is a 4 ×4 row-bypassing multiplier. Each input is connected to an FA through a tristate gate. When the inputs are11112 * 10012, the two inputs in the first and second rows are 0 for FAs. Because b1 is 0, the multi-plexers in the first rowselect aib0 as the sum bit and select 0 as the carry bit. The inputs are bypassed to FAs in the second rows, and the tristategates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similar-ly, becauseb2is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row becausethe b3 is not zero.

Cloumn-Bypassing Multiplier:

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). . The multiplier array consists of (n−1) rows of carry save adder (CSA), in which each row contains (n − 1) full adder (FA) cells.

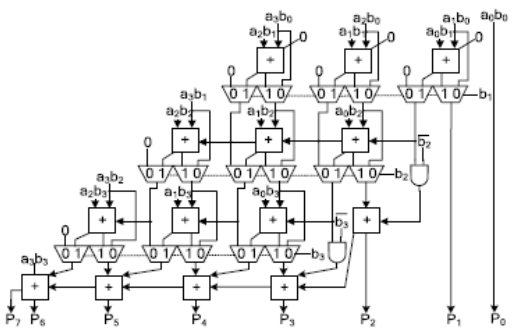

Figure 2 : 4 × 4 column-bypassing multiplier.

Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation. The FAs in the AM are always active regardless of input states.A low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 2 shows a 4×4 column-bypassing multiplier. Supposing the inputs are 10102 * 11112, it can be seen that for the FAs in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product aibi . Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.

IV.PROPOSED AGING-AWARE MULTIPLIER:

The proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of eachcomponent and also describes how to design AHL that adjusts the circuit when significant aging occurs.

Proposed Architecture:

Proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multipli-er, 2m 1-bit Razor flip-flops, and an AHL circuit.

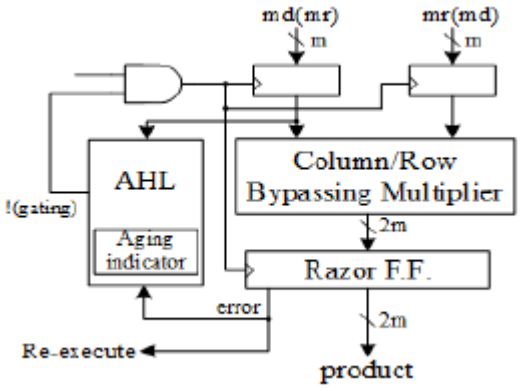

Figure 3: Proposed architecture (md means multiplicand; mr means multiplicator).

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Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution resultusing a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result.

If errors occur, the Razor flip-flop will set the error signal to 1 to notify the sys-tem to reexecute the operation and notify the AHL circuit that an error has occurred. We use Razor flip-flops to detect whether anoperation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is re executed with two cycles. Although the re execution may seem costly, the overall cost is low because the reexecution frequency is low. More details for the Razor flip-flop can be found. The AHL circuit is the key component in the aging-ware variable-latency multiplier. Fig. shows the details of the AHL circuit. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect.

The aging indicator is implemented in a simple counter that counts the number of errors over a certain amount of operations and is reset to zero at the end of those operations. If the cycle period is too short, the column- or row-bypassing multiplier is not able to complete these operations successfully, causing timing violations.

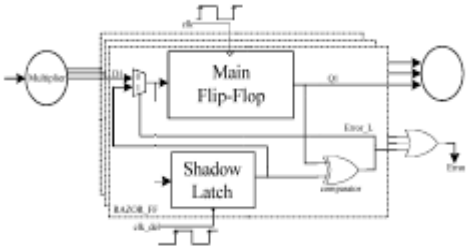

Figure 4 : Razor flip flops.

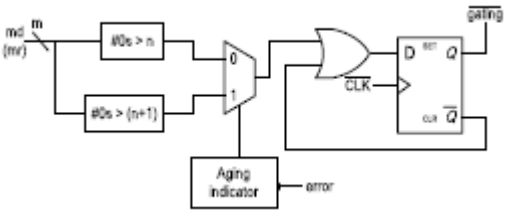

Figure 5: Diagram of AHL (md means multiplicand; mr means multiplicator).

The setiming violations will be caught by the Razor flip-flops, which generate error signals. If errors happen frequently and exceed a predefined threshold, it means the circuit has suffered significant timing degradation due to the aging effect, and the aging indicator will out-put signal 1; otherwise, it will output 0 to indicate the aging effect is still not significant, and noactions are needed. The first judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand(multiplicator for the row-bypassing multiplier) is larger than n and the second judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (multiplicator)is larger than n + 1.

They are both employed to decide whether an input pattern requires one or two cycles, but only one ofthem will be chosen at a time. In the beginning, the aging effect is not significant, and the aging indicator produces 0, so thefirst judging block is used. After a period of time when the aging effect becomes significant, the second judging block ischosen. Com-pared with the first judging block, the second judging block allows a smaller number of patterns to become-one-cycle patterns because it requires more zeros in the multiplicand (multiplicator).

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The details of the operation of the AHL circuit are as follows: when an input pattern arrives, both judging blocks will decide whether the pattern requires one cycle or two cycles to complete and pass both results to the multiplexer. The multiplexer selects one of either result based on the output of the aging indicator. Then an OR operation is performed between the result of the multiplexer, and the Q signal is used to determine the input of the D flip-flop. When the pattern requires one cycle, the output of the multiplexer is1. The !(gating) signal will become 1, and the input flip flops will latch new data in the next cycle. On the other hand, whenthe output of the multi-plexer is 0, hich means the input pattern requires two cycles to complete, the OR gate will output 0to the D flip-flop. Therefore, the (gating) signal will be 0 to dis-able the clock signal of the input flip-flops in the next cycle.Note that only a cycle of the input flip-flop will be disabled because the D flip-flop will latch 1 in the next cycle.

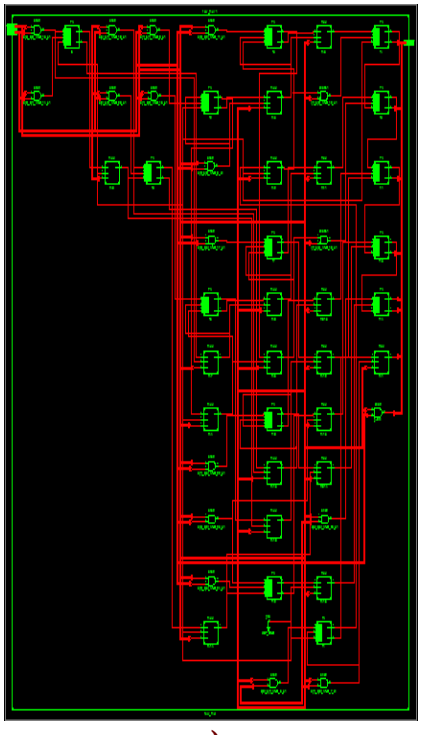
The overall flow of our proposed architecture is as follows: when input patterns arrive, the column- or row-bypassing multiplier, and the AHL circuit execute simultaneously. Accord-ing to the number of zeros in the multiplicand (multi-plicator), the AHLcircuit decides if the input patterns require one or two cycles. If the input pattern requires two cycles to complete, the AHLwill output 0 to disable the clock signal of the flip-flops. Otherwise, the AHL will output 1 for normal operations. When thecolumn-or row-bypassing multiplier finishes the operation, the result will be passed to the Razor flip-flops.

The Razor flipflopscheck whether there is the path delay timing violation. If timing violations occur, it means the cycle period is not longenough for the current operation to complete and that the execution result of the multipli-er is incorrect. Thus, the Razorflip-flops will output an error to inform the system that the current operation needs to be reexecuted using two cycles toensure the operation is correct.

In this situation, the extra reex-ecution cycles caused by timing violation incurs a pen-alty tooverall average latency. However, our proposed AHL circuit can accurately pre dict whether the input patterns require oneor two cy-cles in most cases. Only a few input patterns may cause a timing variation when the AHL circuit judgesincor-rectly. In this case, the extra reexecution cycles did not produce significant timing degradation. In summary, ourproposed multiplier design has three key features. First, it is a variable-latency design that minimizes the timing waste ofthe noncritical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flopsdetect the timing violations and reexecute the operations using two cycles. Finally, our architecture can adjust thepercentage of one-cycle patterns to minimize performance degradation due to the aging effect. When the circuit is aged, andmany errors occur, the AHL circuit uses the second judging block to decide if an input is one cycle or two cycles.

V.SIMULATION RESULTS:

RTL FOR PROPOSED 8X8 ROW-BYPASSING & COLUMN BYPASSING MULTIPLIER



a)

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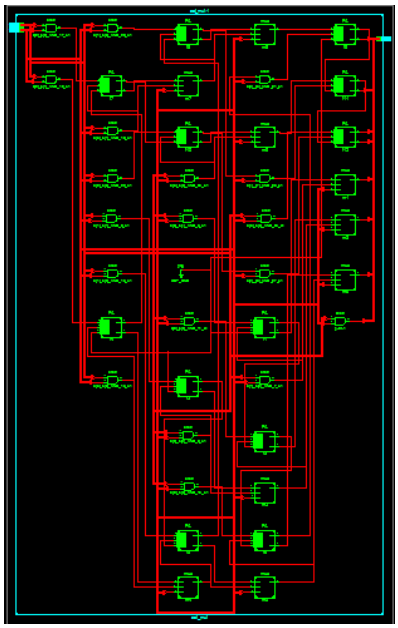
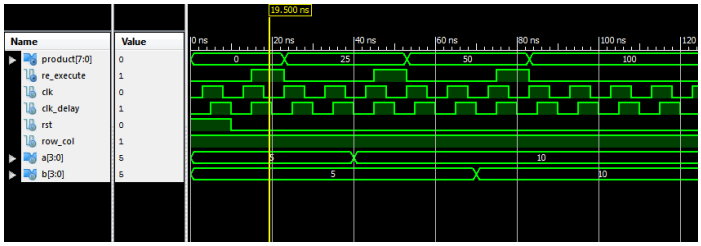
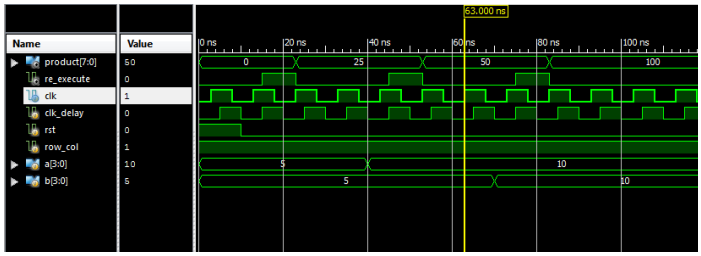


b)

Figure 6 : a) 8X8 Row bypassing multiplier, b) 8X8 Column bypassing multiplier



a)



b)

Figure 7: Simulation result of a) Existing, b) proposed

Area & Delay Reports

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	22	9112	0%
Number of fully used LUT-FF pairs	0	22	0%
Number of bonded IOBs	16	232	6%

a)

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 10.725ns
```

b)

Figure 8: a) Area & b) Delay for Existing

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	44	18224	0%
Number of Slice LUTs	67	9112	0%
Number of fully used LUT-FF pairs	18	93	19%
Number of bonded IOBs	21	232	9%
Number of BUFG/BUFGCTRLs	3	16	18%

a)

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 5.392ns (Maximum Frequency: 185.460MHz)
   Minimum input arrival time before clock: 5.518ns
   Maximum output required time after clock: 6.949ns
   Maximum combinational path delay: No path found
```

b)

Figure 9: a)Area & b) Delay for Proposed

VI.CONCLUSION:

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that our proposed architecture with 8x8 multiplication with Bypass multipliers as last stage instead of Normal RCA adder it will decrease the delay and improve the performance compared with previous models.

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