ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Modified Carrier Based PWM for Quasi-Z-Source Inverter-Based Grid-Tie Single-Phase Photovoltaic Power System

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Abstract

In single-phase photovoltaic (PV) system, there is double-frequency power mismatch existed between the dc input and ac output. The double-frequency ripple (DFR) energy needs to be buffered by passive network. Otherwise, the ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, electrolytic capacitors are usually used for this purpose due to their high capacitance. However, electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. In this paper, a capacitance reduction control strategy is proposed to buffer the DFR energy in single-phase Z-source/quasi-Z-source inverter applications.This paper also presents an effective control method, including system-level control and Carrier based pulse width modulation for quasi-Z-source inverter (qZSI) based grid-tie photovoltaic (PV) power system. A new method carrier PWM strategies is also proposed and compared with different conventional carrier PWM technique. Reduction of total harmonics distortion (THD) and improvement of the harmonic spectrum of inverter output voltage are some advantages of the proposed control method. The simulation results based on the MATLAB/SIMULINK software are presented to validate the capabilities of the proposed modulation method.

Keywords: ***photovoltaic (PV) power system, quasi-Z-source inverter, space vector modulation (SVM).***

1. Introduction

The extensive use of fossil fuel in power plants will make it rare in the near future. Renewable Energy (RE) is considered as an alternative energy source (sustainable energy source) and has experienced one of the largest growth areas (a rate higher than 30% per year) in the last decennia [1-5], compared with the development of oil and gas energy. The RE based power generation systems have several advantages compared with the conventional ones such as sustainability, pollution-free operation, and possibility of being installed closer to the end users. One of the important potential sources of RE is solar energy due to its large availability, no emission ability, and easy buildings integration [6-9]. The PV power capacity is experiencing all over the world a growth due to the price reductions and technology enhancements that are mostly dominated by grid-connected applications. Consequently, to support the use of green solar electricity, many governments and agencies have sponsored installation costs and purchase of electricity produced by grid-tie distributed generation systems.

THE voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) have been considered for photovoltaic (PV) application in recent years [1]–[13]. These inverters feature single-stage buck–boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1]–[5]. The singlephase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance [6]–[12]. In three-phase applications, the Z-source (ZS)/quasi-Z-source (qZS) network only needs to be designed to handle the highfrequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present

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the proposed control strategy. A single-phase qZSI system is shown in Fig. 1. Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency.

The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which has higher voltage rating than C2 . The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance. As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion. This process is accelerated with higher temperature, eventually leading to performance degradation over time [14]. Therefore, electrolytic capacitors are considered to be the weak component regarding to lifetime, especially under outdoor operation conditions.

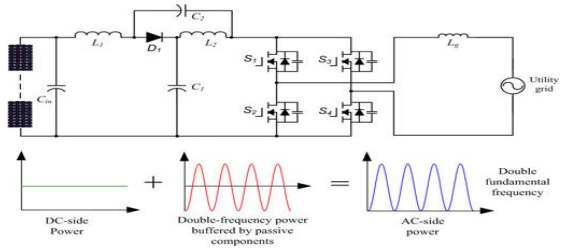

Fig. 1. Diagram of a single-phase qzsi-based PV system.

2. DESCRIPTION OF QZSI-BASED GRID-TIE PV POWER SYSTEM

Accurate analytical models to calculate the DFR for qZSI have been developed in [8], [15], and [16] and the design guidelines for selecting the capacitance to limit the DFR are also provided. Nevertheless, the required capacitance is still large.

In [17], two additional smoothing-power circuits are employed to reduce the DFR of dc-link voltage in ZSI.

However, the added circuits increase the system cost and complexity. In [18], a low frequency harmonic elimination PWM technique is presented to minimize the DFR on Z-source capacitors. However, the method is used for application with constant voltage input source and DFR current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels. In some reported single-phase two-stage system which is composed of a dc–dc converter and H-bridge inverter, the dclink capacitance can be significantly reduced by using dedicated control [14], [19]. However, the qZSI does not have the dc–dc stage, so the reported capacitance reduction methods cannot be applied in the qZSI.

2.1 qZSI

The qZSI combines the qZS network into each HBI module. When the Kth qZS-HBI is in non shoot-through states, it will work as a traditional HBI. There are

$$\hat{v}_{\mathrm{DCk}} = \frac{1}{1-2D_k} v_{\mathrm{PVk}} = B_k v_{PVk} \qquad v_{Hk} = S_k \hat{v}_{\mathrm{DCk}} \quad (1)$$

While in shoot-through states, the qZS-HBI module does not contribute voltage. There are

$$\hat{v}_{\mathrm{DCk}} = 0 \quad v_{Hk} = 0. \qquad (2)$$

For the qZSI, the synthesized voltage is

$$v_H = \sum_{k=1}^{n} v_{Hk} = \sum_{k=1}^{n} S_k \hat{v}_{\mathrm{DCk}} \qquad (3)$$

Where vPVk is the output voltage of the th PV array; vDCk is the dc-link voltage of the th qZS-HBI module; Dk and Bk represent the shoot-through duty ratio and boost factor of the Kth qZS-HBI, respectively, vHk is the output voltage of the Kth module, and Sk belongs to {-1,0,1} is the switching function of the Kth qZS-HBI.

2.2 Control Strategy

The basic principle of the proposed capacitance reduction method can be explained by

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International Journal & Magazine of Engineering, Technology, Management and Research
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$$\Delta E = \frac{1}{2} C \left(v_{C\_\max}^2 - v_{C\_\min}^2 \right)$$

where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and vC max and vC min are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE. One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented.

Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, grid connected current controller, qZS capacitor voltage controller, and input DFR suppression controller. The MPPT controller provides the input voltage reference v∗ IN . The error between v∗ IN and vIN is regulated by a PI controller and its output is the magnitude of the grid current reference. The grid current ig is reg lated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency.

The qZS capacitor voltage is regulated by controlling dSH. The shoot through lines can be generated as v∗ p = 1− dSH and v∗ n =−1 + dSH. It is noted that vC2 is used for the capacitor voltage control. This is because vC2 signal will be used for the qZS network oscillation damping. As will be explained in Section III-A, the oscillation is mainly caused by the resonance among the C2 and inductors. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and vC2 information is required for the implementation.

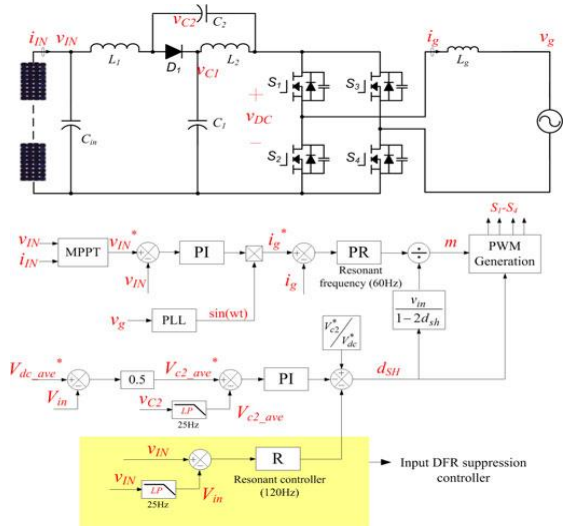

Fig. 2. Diagram of the proposed control system.

3. SYSTEM MODELING AND CONTROL

Fig. 2 shows block diagram of the proposed grid-tie control with the system model for the qZSI based PV power system. The details will be explained as follows.

Grid-Tie Current Loop

After that the current loop of Fig. 2 is simplified to Fig. 3

Fig. 3 Simplified block diagram of the grid-current closed loop

PV Voltage Loop

The block diagrams of total and separate PV voltage loops can be obtained in Figs. 4 and 5.

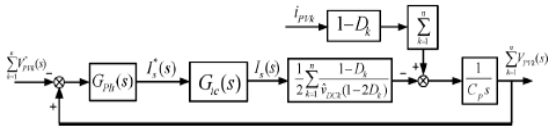

Fig. 4 Block diagram of total PV voltage loop

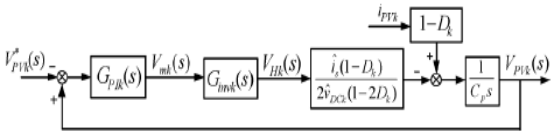

Fig. 5 Block diagram of separate PV voltage loop

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International Journal & Magazine of Engineering, Technology, Management and Research
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DC-Link Voltage Control

The independent dc-link peak voltage control based on the inductor-L2 current and the capacitor-C1 voltage is performed for each qZS-HBI module, as Fig. 1(b) shows. With the employed proportional regulator at the coefficient for the inductor current loop, as the block diagram of KdPk Fig. 6

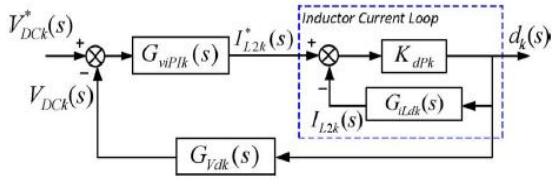

Fig. 6 Block diagram of the Kth module's dc-link peak voltage control

A PI regulator with the transfer function of GviPIk(s)=KVdPk+(KVdIk/s) is cascaded to the inductor current loop for controlling the dc-link peak voltage, as shown in Fig. 6.

4. MODIFIED CARRIER PWM FOR QZSI

Here a delay of the switching times for upper switches or a lead of the switching times for lower switches are employed at the transition moments, as Fig. 7(a) shows. To generate the step-like ac output voltage waveform from the qZSI, a 2pi/(nK) phase difference, in which K is the number of reference voltage vectors in each cycle, is employed between any two adjacent voltage vectors, as Fig. 7(b) shows.

4.1 CONTROL PARAMETER DESIGN

The prototype specifications of qZSI based PV power system are shown in Table I. The design results are shown in Table II, and all of the Bode plots are shown in Figs. 8–10. Fig. 8 shows the Bode plots of the grid-tie current loop transfer functions Gio(s) and Gicom(s), which are before and after compensation, respectively.

TABLE I
PROTOTYPE SPECIFICATIONS

Parameters	Value
Minimum PV array voltage, $V_{PV,min}$	60 V
Maximum PV array voltage, $V_{PV,max}$	120 V
qZS inductance, L_1 and L_2	1.8 mH
qZS capacitance, C_1 and C_2	3300 μF
PV array parallel capacitance, C_p	1100 μF
Filter inductance, L_f	1 mH
Carrier frequency, f_c	5 kHz

TABLE II
CONTROL PARAMETERS

Parameters	Value	Parameters	Value
k_{iP}	5.15e-3	k_{iR}	0.1592
k_{Pf}	1.1464	k_{ft}	10.854
k_{PK}	0.015	k_{fk}	0.05256
k_{dPk}	0.0068		
k_{VdPk}	0.0281	k_{VdIk}	2.5254

Fig. 9(a) shows the Bode plots of total PV voltage control loop transfer functions Gvot(s) and –Gvcomt(s), which correspond to before and after compensation, respectively. Similarly, the Bode plots of separate PV voltage control are shown in Fig. 9(b). From Fig. 9(b) and (25), we know that the Gvok(s) is not stable. Compensated by the PI regulator GPIk(s), an 87.5 phase margin is shown in –Gvcomk(s). The closed-loop transfer function Gvck(s) also confirms its stable feature. Fig. 10 shows the Bode plots of transfer functions for each module's dc-link peak voltage control loop. When using a proportional gain KdPk, the inductor L2 current shows a faster response without loss of the stability, as shown in Fig. 10(a). From Fig. 10(b), the dc-link peak voltage closed-loop's stability is greatly improved by decreasing the crossover frequency. As a result, the closed-loop transfer function GVdck(s) presents a fast and robust characteristic.

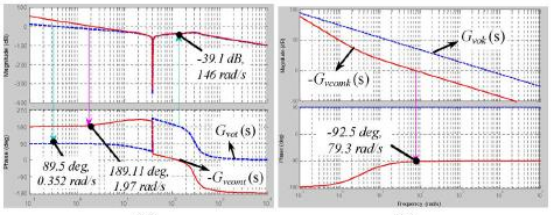

Fig. 9. Bode diagrams of (a) $G_{vot}(s)$ and $-G_{vcomt}(s)$; and (b) $G_{vok}(s)$ and $-G_{vcomk}(s)$.

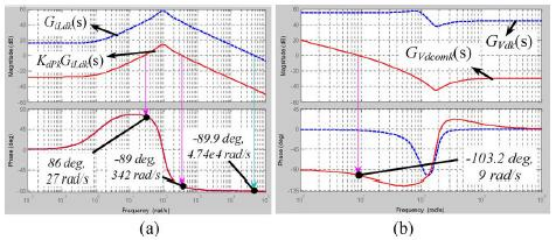

Fig. 10. Bode diagrams of (a) $G_{iLdk}(s)$ and $K_{dPk}G_{iLdk}(s)$ and (b) $G_{Vdk}(s)$ and $G_{VdcomK}(s)$.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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4.2 CONVENTIONALCARRIER-BASED PWM METHODS

Multicarrier PWM techniques entail the natural sampling of a single modulating or reference waveform typically being sinusoidal, through several carrier signals typically being triangular waveforms [9].In order to describe the different multi-carrier PWM methods the following definitions should be considered:

- The frequency modulation index is defined as mf = fc / fr, where fc is the frequency of carrier signals and fr is the frequency of the reference signal.
- The amplitude modulation index is defined as ma = Ar / Ac, where Ar is the amplitude of reference signals and Ac is the peak to peak value of the carrier signal [8].

The methods are

- PD-PWM method
- POD-PWM method
- APOD-PWM method

4.3 PROPOSED MODULATION METHOD

For reducing the number of carrier signals and also improvement of the THD and harmonic spectrum of inverter output voltage, a new modulation strategy is proposed in this paper. The proposed multi-carrier PWM method uses (N -1) / 2 carrier signals to generate the N - level at output voltage. The carrier signals have the same amplitude, Ac and the same frequency, fc, and are in phase. The sinusoidal reference wave has a frequency fr and an amplitude Ar. In the proposed method, the sinusoidal reference and its inverse are used for generating the required gate signals. The frequency of the output voltage is determined by the frequency of the sinusoidal reference waveform. The amplitude of the fundamental component of the output voltage is determined by the amplitude modulation index, ma .Fig. 1 shows the proposed multicarrier PWM method for a single-phase 5-level inverter. As this figure shows, the proposed method uses two reference signals and two carrier signals. This method is based on a comparison of the sinusoidal reference waveforms with carrier waveforms. For even and odd values of frequency modulation index, mf, the significant harmonics are located in two sidebands around the frequency, 2 fc. As a result, the frequency spectrum of the output voltage is improved. So, the size of the required filter will be small. It is important to note that the design of filter is not the objective of this work. Reduction of the THD of the output voltage is other important advantage of the proposed method. It is noticeable that the conventional modulation methods generate the significant harmonics in two sidebands around the carrier frequency, fc.

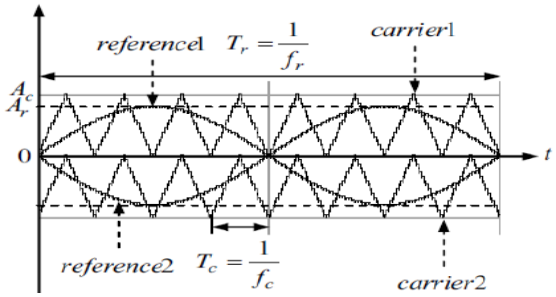

Fig. 7 Proposed modified-carrier PWM method for a single-phase qZS inverter

5. SIMULATION RESULTS

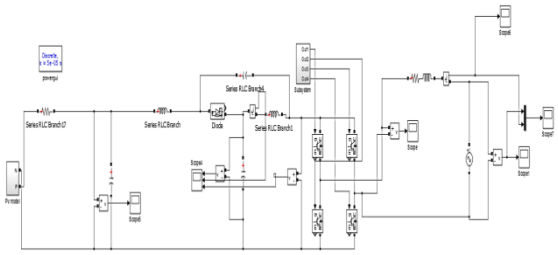

Fig. 12 Simulation of the qZSI

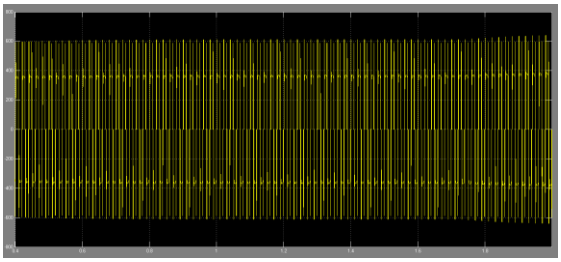

Fig. 13 Output Voltage of qZSI

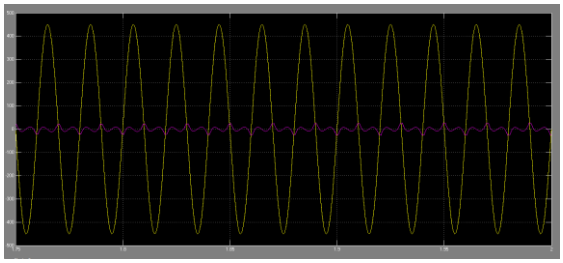

Fig. 14 Grid Voltages and Currents

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6. CONCLUSION

In this paper, a new control strategy that is modified carrier PWM is proposed to minimize the capacitance requirement in single-phase qZSI PV system. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the DFR energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability much. For the developed 1-kW quasi-Z-source PV system, 2 mF capacitor can be replaced with a 200 μF capacitor by using the proposed method. This control strategy can also be applied in single-phase ZSI applications. The proposed modified carrier PWM is verified with the simulation results.

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