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A Novel Design Architecture for Folded Configurable IIR Filter

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Abstract:
Filters are the basic circuit in any Digital Signal Processing (DSP) applications. An efficient IIR Filter is designed with folded configuration which can be used in real time DSP applications. Proposing a new configurable 6th order IIR filter design by cascading three 2nd order IIR filters. The same design can also used as one 6th order IIR filter or one 4th order and one 2nd order filter or three 2nd order IIR filter operations in parallel. Each 2nd order IIR filter is designed using floating point Multiply Accumulate Circuit (MAC). An improved performance is obtained by proposed 6th order IIR filter using three 2nd order filters compared to conventional MAC based architecture.

Keywords:
IIR Filter, Floating point, Multiply Accumulate Circuit (MAC).

1. Introduction:

Filters are the widely used circuits in digital signal processing for many applications. Filters are mainly preferred to remove undesirable part of the signal, which is floating point series. IIR filters are more effectual compare to FIR filter due to feedback system. The general form of digital filter is the series of multiplication and repeated addition.

$$y[n] = \sum_{k=1}^{N} a_k y[n-k] + \sum_{k=0}^{M} b_k x[n-k]$$

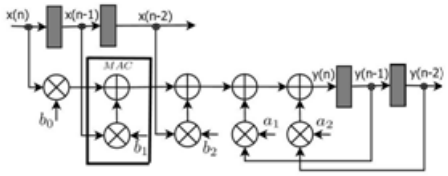

Figure 1: Architecture for second order IIR filter

The digital Infinite Impulse Response (IIR) filter is represented in Figure 1. Here x(n) and y(n) are the input and output signal sequences respectively. IIR filter design for second order is detailed in 2. The operation of multimode filtering is described in 3, here the cascaded second order FIR filter is applied to change the filter order depending on the constraint. Multiplier next to accumulator is used to design each second order FIR filter. The parameters like Critical path delay, power & Area are analysed to observe the performance of the circuit. The performance of the Circuit is improved by providing appropriate optimization in these parameters. The configurable sixth order IIR filter is designed using three series of IIR filters which is second order, where each second order IIR filter is designed by Floating point Multiply-Accumulate-unit (MAC). Arithmetic and multiplier concept are detailed in 5,6. The use of this filter is to execute single sixth order or three second order or one fourth order and one second order in parallel. This proposed architecture for the design of filter gives improved performance compared to the existing filter design.

2. IIR Filter Design:

Floating point values are used for the design of IIR filter. Two things are integrated together for the design of filter. First thing is the design of second order IIR filter using modified multiply-accumulate-circuit, here addition is performed using present multiplication so the depth of modified multiply-accumulate-circuit is reduced compared with conventional MAC design. Figure 2(a) shown is the design of conventional multiply-accumulate-circuit (MAC).

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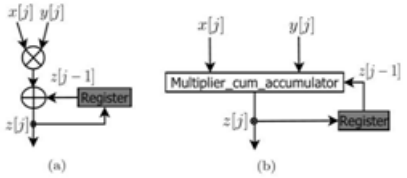

Figure 2: Multiply Accumulate Circuit (a) conventional (b) modified

In conventional MAC, a separate adder is used for adding the result of present multiplication with previous MAC result. This additional adder circuit for addition is avoided in modified multiply-accumulate-circuit. Figure 2(b) shows the modified MAC circuit and it is called as multiplier-cum-accumulator. The Second thing is multimode operation is performed with IIR filter it follows the series of second order IIR filter.

3. Multiply Accumulate Circuit:

Multiplier cum accumulator using floating point contains three sections, they are Mantissa alignment, Multiplication-cum-accumulation and Normalization. In floating point multiply-cum-accumulation operation, Let [As, Ae, A], [Bs, Be, B] are the two input operands and [Ps, Pe, P] is denoted as result of prior MAC. Here, As, Bs, Ps are sign bits, Ae, Be, Pe are exponent bits and A, B, P are the normalized mantissas. Based on the select line (sel=0), the operation starts performing. Then multiplication operation is performed using complete design which is floating point. If sel=1 it performs MAC operation. The two n-bit input numbers are multiplied and resulting value will be 2n or 2n-1 bit large. Here Ri[msb] is the most significant bit of multiplication result and Ri[lsb] is the least significant bit of multiplication result. Similarly the most significant and least significant bits of preceding MAC result will be Ri-1 [msb] and Ri-1 [lsb]. In floating point MAC Operation Ri [msb] and Ri [lsb] will be aligned. Where the mantissas are Ri, Ri-1, here the least significant bit is 0 and most significant bit is 47 or 46. In modified floating point multiply-accumulate-circuit the partial invention of current multiplication is added with the mantissa of preceding MAC result.

The most significant bit of mantissa of preceding MAC result is align with result of msb bit of the current multiplication which is not attained. So the mantissa of P and B are single place shifted right ({0,P}, {0,B}) the corresponding exponent value will not change and the prevision of most significant bit of multiplication result is avoided. In following step, the result of unbiased exponent value of preceding MAC is related with the sum of balanced exponent. When (Ae + Be) > Pe, by using barrel shifter the mantissa of P is shifted right upto (Ae + Be) – Pe time using rounding pro-cess. Similarly, if (Ae + Be) is less than Pe, mantissa of A is shifted right upto Pe – (Ae + Be). Hence pe will be equal to (Ae + Be). The msb of current multiplication product of aligned A x B is equal to msb of P. Here three more bits for rounding process are (Guard bit (G), Sticky bit (S) and Round off bit (R)) are used right to the most significant bit of the mantissa. Then Wallace tree multiplier is used for multiplication of A and B, where the partial products values are added with P. After that, Normalization is processed in last step of floating point MAC.

4. IIR Filter Design using modified MAC:

Design of IIR filter for modified second order is show in Figure 3. Here the filter coefficients are b0, b1, b2 and a1, a2. Here y(n) denoted as output. x(n) is denoted as input signal sample value. The multiplexer used to select the filter coefficients and value of inputs, outputs for every clock cycle. Equation for 2nd order IIR Filter is given as:

$$y[n] = a1y[n-1] + a2y[n-2] + a3y[n-3] + a4y[n-4] + a5y[n-5] + a6y[n-6] + b0x[n] + b1x[n-1] + b2x[n-2] + b3x[n-3] + b4x[n-4] + b5x[n-5] + b6x[n-6]$$

Design of IIR filter for configurable sixth order is shown in Figure 4. Here three 2-quad IIR filters are cascaded to achieve the IIR filter operations of three second order or one sixth order. It can also be used to perform one fourth order and single second order. Figure 4 shows the mode of operation in IIR filter is performed by using the select line of the multiplexer.

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The IIR filter for sixth order is denoted as shown in figure. Figure 5 shows the 2-quad IIR filter for sixth order design. se2=5 and se22=5, s7=1 the expressions from 2-quad F1 b0x(3)+b1x(2)+b2x(1)+a1y(2)+a2y(1) is add with b3x(0)+a3y(0).Now 2-quad F2 produce a result of y(3) at clock cycle 16.likewise all the output values are get from IIR filter for sixth order.

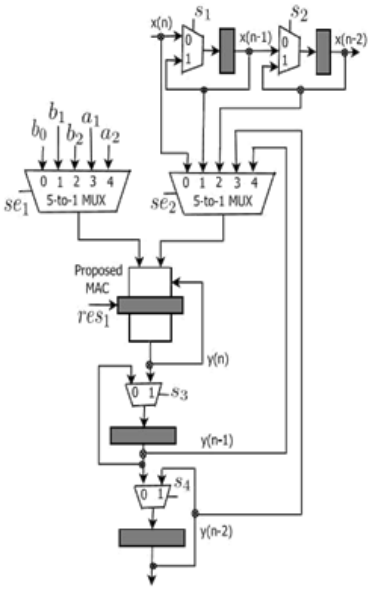


Figure 3: Design of IIR filter for modified second order.

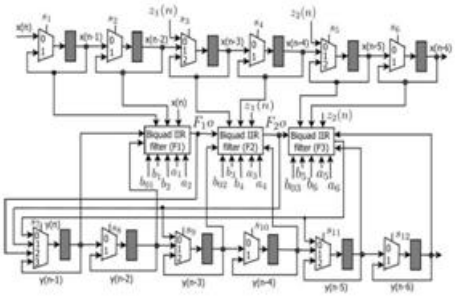
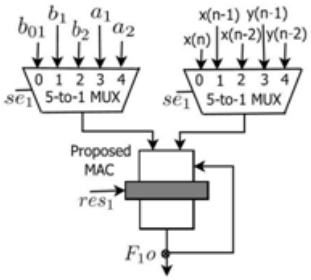
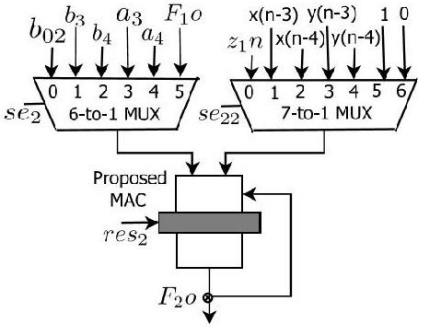


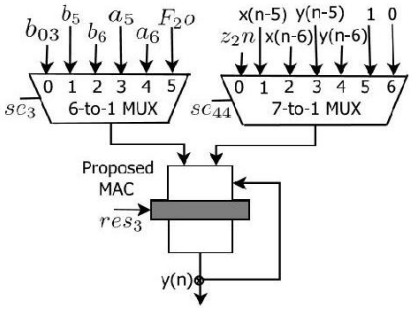
Figure 4: Design of IIR filter for Configurable sixth order.



(a)



(b)



(c)

Figure 5: 2-quad IIR filter for sixth order design (a) 2-quad IIR filter F1, (b) 2-quad IIR filter F2 (c) 2-quad IIR Filter F3.

5. Simulation Results:

Configurable 6th order IIR filter is designed by cascading three 2nd order IIR filters. Floating point Multiply-Accumulate-Circuit (MAC) is used to design 2nd order IIR Filter. This method is used to improve the performance of the filter. Simulation results shows the output of IIR filter for second order and sixth order.

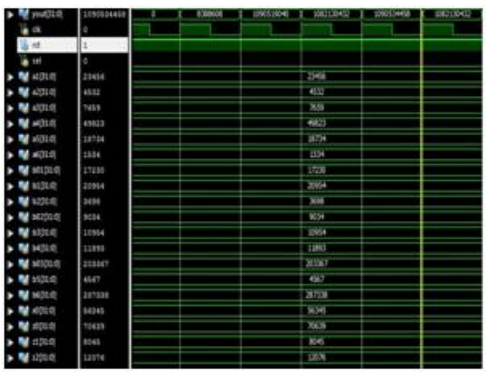


Figure 6: Simulation results for Configurable 6th order IIR Filter

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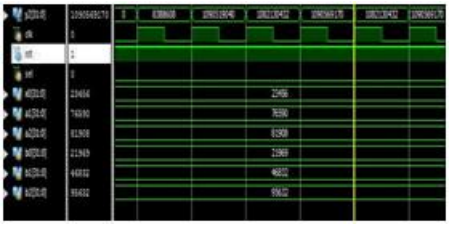

Figure 7: Simulation Results for configured 2nd order filter

6. Conclusion:

Proposing an efficient method for the design of configurable folded IIR Filter using second order filter with a modified Multiply-Accumulate-Circuit (MAC). This design can be used to carry out three second order or one sixth order filter. It can also perform one fourth order and single second order filter in parallel. The proposed configurable design of IIR filter for second order using pipelining achieves high throughput and can also reduce the critical path delay.

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