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## Grid Connected Single-Phase PV inverter with Novel Control Strategy of Suppressing DC Current Injection to the Grid

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#### Abstract

PV inverters without the isolation transformer become more attractive due to higher efficiency and lower weight. However, it may exist DC offset current problem and is critical to the power system. In this paper a novel control strategy of suppressing DC current injection to the grid for PV inverters is investigated. It is based on the idea of accurately sensing the DC offset voltage of PV inverter output. Since DC component of the inverter output can be eliminated, DC injection to the grid can be effectively suppressed. Finally the control scheme is verified by the experiment.

*Index Terms*—*DC current injection, PV inverter, DC offset voltage, DC suppression loop, Grid* 

#### **1. INTRODUCTION**

Due to higher efficiency and smaller size, PV inverters without isolation transformers become more attractive in grid-connected photovoltaic systems [1]-[4], [25]-[36]. However, generally they are unable to automatically suppress DC current injection [5], which may cause the saturation of distribution transformers in the grid and result in poor power quality, higher loss, overheating in the power system [1], [6]-[7], [18]. Consequently, standards and regulations have been formulated to limit PV inverter DC injection to the grid [9]-[11].

To suppress DC injection, some control methods have been proposed [1], [6]-[7], [12]-[17], [23]. The methods of DC current injection suppression can be mainly classified into four categories: blocking DC current with the capacitor, novel inverter topology with DC current suppression ability, current-detection control and voltage P. Mahmood Khan Assistant Professor, Department of EEE VVIT Engineering College, Nambur, Guntur.

detection control. The method of blocking DC current with the capacitor uses a capacitor serially connected between the inverter and the grid [12]. It requires a bulky and expensive capacitor and may cause extra loss. [22] developed a method to block DC current by using virtual capacitor, however, the dynamic response of the closed loop control system was affected by the virtual capacitor.

The method of applying inverter topology with DC current suppression ability uses inherent structure of the inverter topology which can prevent DC current from injecting into the grid, e.g. the half bridge inverter [13]. However, few practical topologies exist. The method of current-detection control uses current sensors to detect the DC current injection to the grid, but its effectiveness is limited by the accuracy of sensor due to the inherent significant zero-drift characteristic of Hall-effect current sensors. To solve the zero-drift problem, an autocalibrating inverter has been proposed by Armstrong [14]. However, this method requires determining the switch state of the H-bridge in order to measure the inherent zero-drift of the system.

Sharma first introduced a detecting method of DC offset voltage in reference [21]. A small 1:1 voltage transformer and an RC circuit were used to detect the DC offset voltage at the inverter output in the full-bridge grid-connected inverter. And the DC offset in the grid current was eliminated by feeding back the DC offset voltage to the PI controller. Alfock and Bowtell [19] continued studying this method by establishing the mathematical model and verified it. [17] uses a voltage sensor at the inverter output consisting of a differential amplifier and a low pass filter.



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DC offset detected at the output of the low pass filter is fed back to the controller. A mathematical model is provided in the paper. However, the experimental results under grid mode were not given. The voltage-detection control method uses sensors to detect the DC voltage offset across the ripple filter [15]. This method implies that very low DC voltage across the filter is measured, which is sensitive to noise. A DC offset detection method is proposed by Giampaolo Buticchi [16]. However, this method needs a nonlinear inductor. Hence, a customized inductor should be designed according to specific systems.

#### 2. PHOTO VOLTAIC SYSTEM

A photovoltaic also photovoltaic system, power system, solar PV system, PV system or casually solar array, is a power system designed to supply usable solar power by means of photovoltaics. It consists of an arrangement of several components, including solar panels to absorb and directly convert sunlight intoelectricity, a solar inverter to change electrical current from DC to AC, as the well as mounting, cabling and other electrical accessories to set-up a working system. It may also use a solar tracking system to improve the system's overall performance or include an integrated battery solution, as prices for storage devices are expected to decline.

Strictly speaking, a solar array only encompasses the ensemble of solar panels, the visible part of the PV system, and does not include all the other hardware, often summarized as balance of system (BOS).

PV systems range from small, roof-top mounted or building-integrated systems with capacities from a few to several tens of kilowatts, to large utilityscale power stations of hundreds of megawatts. Nowadays, most PV systems are connected to the electrical grid, while stand-alone or off-grid systems only account for a small portion of the market. Operating silently and without any moving parts or environmental emissions, PV systems have developed into a mature technology that has been used for fifty years in specialized applications, and grid-connected

systems have been operating for over twenty years. A roof-top system recoups the invested energy for its manufacturing and installation within 0.7 to 2 years and produces about 95 percent of net clean renewable energy over a 30-year service lifetime.

As new installations are growing exponentially, prices for PV systems have rapidly declined in recent years. However, they vary by markets and the system's size. In the United States, prices for utility-scale systems were around 2.50-4.00 per watt in 2012,<sup>[4]</sup> while prices for smaller roof-top systems in the highly penetrated German market fell below  $\in 1.40$  per watt in 2014.<sup>[5]</sup> In that market, solar panels make up for 40 to 50 percent of the overall cost, leaving the rest to installation labor and to the PV system's remaining components.<sup>[6]</sup>

Solar power based on thermal energy, such as concentrated solar power or panels for water heating, are not components of a photovoltaic system.

#### 3. NOVEL DC CONTROL STRATEGY

The Full-Bridge PV inverter without output isolation transformer is shown in Fig. 1. From Fig.1, the grid current reference iref can be expressed as

$$i_{ref} = I_{ref} \cos \theta \tag{1}$$

where Iref is the amplitude of grid current command, and  $\theta$  is the phase angle of grid current which is synchronized with grid voltage by Phase Locked Loop (PLL). PV inverter output generally has DC offset voltage component, which results from disparity of power modules, asymmetry of driving pulses, detection error of current etc. Traditionally a transformer is inserted between the PV inverter and the grid. Although the PV inverter output may have DC voltage component, there is no DC current injection to the grid. However, in the case of the PV inverter without isolation transformer, the inverter output DC offset may cause a significant DC current injection to the grid, which may violate the grid connection standards and cannot be neglected [20]. In order to effectively restrain DC current injection to the grid, a control strategy for a single-phase PV inverter without the isolation transformer is shown in Fig. 2 [17],[24].



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Fig. 1. The original scheme diagram of PV gridconnected inverter



Fig. 2. The novel scheme diagram of PV grid-connected inverter

Compared with Fig.1, an extra DC offset voltage suppression loop is added to the previous control scheme. The DC suppression loop is composed of a differential amplifier, a low pass filter and a DC controller. The input of DC suppression loop is uAB, which is a high-frequency PWM waveform sampled between the point A of inverter bridge-leg 1 and the point B of inverter bridge-leg 2. DC offset voltage of uAB is accurately extracted by a differential amplifier and a low pass filter. Then it is compared with inverter DC voltage reference Udc\_ref which is set to zero, and DC offset voltage error is obtained. The error is regulated by the integral controller. Finally the output of DC controller  $\square$ Udc, which is also the output of DC suppression loop, is added to the grid current reference iref of the grid current control loop.

The novel control strategy has two significant features. The first is that the differential amplifier is used to sample the DC offset voltage between the two bridge-leg middle points of Full-Bridge inverter. To accurately detect the DC offset voltage of the inverter switch-side output voltage uAB, a high-precision differential amplifier with low offset and high CMRR (Common-Mode Rejection Ratio) is needed. The using of differential amplifier can not only reduce the cost, but also avoid the zero-drift by using Hall-effect sensors.

The second one is that DC suppression loop can suppress inverter output disturbances. Therefore the DC current injected to the grid can be effectively suppressed.

# 4. ANALYSIS OF DISTURBANCE SUPPRESSING EFFECT

The control block diagram of PV grid-connected inverter is shown in Fig.3, which is derived from Fig.1. where Iref(z) is current reference of the inverter, Gc(z) is digital controller of current loop, and KG is the gain from the output of current controller Gc(z) to inverter switch side voltage, respectively. Udis(s) represents the disturbance caused by the turn-on and turn-off difference of the four switches, the saturation voltage difference of the four switches, the gate drive signal delay difference of the four switches, and so on. L is the output filter inductor. r is the equivalent resistance of output filter inductor L. Ig(s) is the grid current of the inverter. K1 is the feedback gain of current loop. ADC is the analog to digital converter which converts the analog sampling value of Ig(s) to digital one. ZOH is zero-order holds which is connected in series between the output of digital controller and KG.



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Fig.3. Control diagram for PV grid-connected inverter

From Fig.3, the transfer function in s-domain from disturbance source Udis(s) to grid current Ig(s) with the original control scheme can be derived as follows:

$$\frac{I_g(s)}{U_{dis}(s)} = \frac{s \cdot e^{-(T_s \cdot s)}}{s(sL+r) + K_1 K_G (K_{pi}s + K_{ii})}$$
(2)

where Kpi and Kii are the proportional and integral coefficient of current controller, respectively. e-(s·Ts) is the delay effect considering time delay caused by ADC, digital computation and ZOH, where Ts is the duration of sampling period [38], Ts=1/fs, fs is switching frequency of PV inverter. In theory, if both the feedback gain of current loop K1 and ADC are accurate enough, the DC offset of grid current can be eliminated with PI regulator. However, it is actually limited by ADC resolution and accuracy of the current sensor. The maximum grid DC current detecting error  $\square$ Ig can be calculated as

$$\Delta I_g = \Delta I_{g1} + \Delta I_{g2} \tag{3}$$

where 🛛 Ig1 represents error caused by ADC resolution. 🖓 Ig2 represents error caused by the error of current sensor and conditioning circuit.

#### A. Analysis of Detecting Error Caused by ADC

When N-bit ADC is adopted, the DSP sampled digital value Igs of the grid current Ig for the PV grid inverter can be expressed as

$$I_{gs} = I_g \times \frac{2^N}{(1+\beta) \times I_{p_p}} \tag{4}$$

where Ip\_p is peak to peak value of the rated grid current, and  $\beta$  represents the overload coefficient of the grid current. From (4), the detecting error of the grid DC current  $\mathbb{Z}$ Ig1 caused by the ADC resolution is given by

$$\Delta I_{g1} = \frac{\left(1+\beta\right) \times I_{p_p} \times \Delta I_{gs}}{2^N} \tag{5}$$

where Igs is ADC error of the DSP.

## **B.** Analysis of Detecting Error Caused by Current Sensor and Conditioning Circuit

The grid DC current detecting error 🛛 Ig2 caused by the error of the current sensor and conditioning circuit is given by

$$\Delta I_{g2} = \frac{\Delta I_{Lem}}{K_1'} + \frac{\Delta I_{Con}}{K_2'} \tag{6}$$

where ILem and ICon represent the error caused by current sensor and conditioning circuit, respectively. K1 .rosnes therruc eht fo oitar noisrevnoc therruc si 'K2 si ' gain of the conditioning circuit. Therefore, by substituting (5) and (6) into (3), the maximum gird DC current detecting error Igg can be calculated as

$$\Delta I_g = \frac{(1+\beta) \times I_{p_p} \times \Delta I_{gs}}{2^N} + \frac{\Delta I_{Lem}}{K_1'} + \frac{\Delta I_{Con}}{K_2'}$$
(7)

Let's take a PV grid inverter as an example with parameters listed as follows. Rated power Pe=3 kW, rated grid voltage Ug=220V rms, peak to peak value of the rated grid current Ip\_p=38.6A, overload coefficient of the grid current  $\beta=0.2$ , the current sensor accuracy □ILem=±0.1mA, conversion ratio of the current sensor K1 0.0015 =' . The conditioning circuit error □ICon=±0.2mA, the gain of conditioning circuit K2 0.25 ='. The ADC error **Z**Igs=±1.5LSB. By substituting the above parameters into (7), the relationship between the ADC bit N and the total grid DC current detecting error Ig is drawn in Fig. 4. The solid line shows the relationship between the ADC bit N and the grid DC current detecting error Ig with the original control scheme. The dotted line is the DC current limit standard [9]-[11]. It can be seen from Fig. 4 that the grid DC



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current detecting error is larger than the standard value with traditional control.



Fig. 4. Relationship between the ADC bits and the grid DC current detecting error, with original control scheme, and with the novel control scheme

### C. Analysis of Detecting Error with the Novel Control Strategy

In order to realize that the grid DC current detecting error is less than the standard value, the new control scheme is introduced in this paper. As shown in Fig.5, an extra DC suppressing loop is introduced to the original control scheme of PV grid-connected inverter. UAB(s) is the voltage between the two bridge-leg middle points of Full- Bridge inverter, GPI(z) is digital controller of DC suppression loop in z-domain, respectively. Gdc(s) is the feedback gain of DC suppression loop. Ig uc dirg eht si (s)'rrent of the converter under the new control scheme.



Fig. 5. Control block diagram with novel control scheme

From Fig.5, The relationship between the UAB(s) and the grid current Ig sa devired eb nac (s)'

$$U_{AB}(s) = U_g(s) + (sL + r) \cdot I'_g(s) \tag{8}$$

where L is filter inductor and r is equivalent resistance of the filter inductor. For the DC c

$$I'_{g\_dc} = \frac{U_{AB\_DC}}{r} \tag{9}$$

where UAB\_DC is the DC component of UAB(s). The DC suppression loop in Fig.5 is designed to detect the DC component of the converter switch-side output voltage UAB(s). The relationship between the DC component of UAB(s) and the DSP sampling value UABs can be derived as

$$U_{ABs} = U_{AB_{DC}} \cdot \frac{2^{N}}{U_{dc_{max}}}$$
(10)

where Udc\_max is maximum DC offset voltage. By combining equation (9) and equation (10), we obtain

$$I'_{g\_dc} = \frac{U_{dc\_max}U_{ABs}}{2^{N}r}$$
(11)

Furthermore, the grid DC current detecting error  $\Delta Ig_dc$  with the novel control strategy can be given by

$$\Delta I'_{g\_dc} = \frac{U_{dc\_max} \times \Delta U_{ABs}}{2^N \times r}$$
(12)

where  $\Delta UABs$  is ADC error of the DSP we used. Considering the PV grid inverter system: the value of  $\Delta UABs$  is ±1.5LSB, maximum DC voltage Udc\_max is 0.5V, r is 0.26 $\Omega$ . The relationship between the ADC bits and the grid DC current detecting error with the novel control scheme is shown in Fig. 4. The solid line is the relationship between the ADC bits and the grid DC current detecting error with the original control scheme. The dash line is the relationship between the ADC bits and the grid DC current detecting error with the novel control scheme. The dotted line represents the DC current limited standard. It can be seen from Fig.4 that the grid DC current detecting error is lower than the standard value with the novel control scheme if the ADC number of bits is greater than 9.

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Volume No: 4 (2017), Issue No: 10 (October) www.ijmetmr.com



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### **D.** Comparison of DC Suppressing Effect

From Fig.5, the transfer function from disturbance source Udis(s) to grid current Ig s ni (s)'-domain with the novel control scheme can be derived as

$$\frac{I'_{g}(s)}{U_{dis}(s)} = \frac{s^{2} \cdot e^{(-sT_{s})}}{s^{2} (sL+r) + K_{G} \cdot G_{dc}(s) (K_{pi}s + K_{ii}) (K_{pd}s + K_{id}) (sL+r) + K_{1} \cdot K_{G} \cdot s (K_{pi}s + K_{ii})}$$
(13)

From (2) and (13), the DC current suppression effect is shown in Fig.6, here parameters are presented in Table I. It can be seen from Fig.6, low frequency of DC current suppression effect with the novel control scheme is much better than that with the original control scheme.



## 5. TUNING OF PI CONTROLLER IN THE DC OFFSET SUPPRESSION LOOP

Fig. 7 shows the equivalent control diagram with DC offset suppression loop, which is derived from Fig. 5. From Fig. 7, the open loop uncompensated transfer function of equivalent DC suppression loop can be expressed as

$$G_{dc\_offset}(s) = \frac{K_G \cdot G_{dc}(s) \cdot \left(K_{pi}s + K_{ii}\right) \cdot \left(sL + r\right) \cdot e^{\left(-sI_s\right)}}{Ls^2 + \left(r + K_G \cdot K_1K_{pi}\right)s + K_G \cdot K_1K_{ii}}$$
(14)

where Kpi and Kii are the proportional and integral parameters of current loop, respectively, which are designed as: Kpi=1.2, Kii=1560 (The bandwidth of current loop is designed as 800 Hz). Gdc(s) is the feedback gain which includes differential amplifier and low pass filter, which can be expressed as

$$G_{dc}\left(s\right) = \frac{2}{\left(1 + \frac{s}{2\pi f_{LP}}\right)^2}$$
(15)

where fLP is the cut-off frequency of the second-order low pass filter for the DC suppression loop, which has been designed at 3 Hz.

The bandwidth of DC suppressing loop is designed as 1 Hz, which is much smaller than the bandwidth of current loop. The zero-point frequency of PI controllers of DC suppression loop is designed as 5 Hz. Therefore, the proportional coefficient Kpd and integral coefficient Kid of DC suppression loop can be calculated from the following equations [37],

$$\left| \frac{K_{id}}{2\pi K_{pd}} = 5 \right|$$

$$\left| G_{dc\_offset}(s) \cdot \frac{\left(K_{pd}s + K_{id}\right)}{s} \right|_{s=2\pi \cdot 1} = 1$$

$$(16)$$

From (16), the parameters of the DC suppression loop are finally chosen as: Kpd=0.015, Kid=0.473.



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Volume No: 4 (2017), Issue No: 10 (October) www.ijmetmr.com



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### 6. SIMULATION RESULTS



Fig. 8 Simulation Grid Connected Single Phase PV System



Fig. 9 Grid Voltages and Currents

#### 7. CONCLUSION

This paper investigated a novel control strategy to eliminate DC current injection to the grid for singlephase PV inverter without the isolation transformer. It is based on accurately sensing the DC offset voltage between the two bridge-leg middle points of Full-Bridge inverter. The novel control strategy is inherently free from offset measurement errors. Both analysis and experimental results show that the novel control strategy can effectively suppress DC injection current of photovoltaic system under grid-connected condition.

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