ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design Methodologies for Reliable Clock Networks

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Abstract:
A low-voltage/swing clocking methodology is developed through both circuit and algorithmic innovations. The primary objective is to significantly reduce the power consumed by the clock network while maintaining the circuit performance the same. The methodology consists of two primary components: 1) a novel D-flip-flop (DFF) cell that maximizes power savings by enabling low-voltage/swing operation throughout the entire clock network and 2) a novel clock tree synthesis algorithm to ensure that the same timing constraints (i.e., clock frequency, skew, and slew) are satisfied. The proposed methodology is integrated within an industrial design flow. Experimental results on ISCAS'89 benchmark circuits demonstrate that the overall power consumed by the clock tree can be reduced by up to 27% and 44% in, respectively, 32- and 45-nm technologies while satisfying the same timing constraints. Furthermore, the proposed low-swing DFF cell maintains the clock-to-Q delay the same while achieving up to 32% and 15% power savings in the overall flip-flop power of the benchmark circuits at, respectively, 1- and 1.5-GHz clock frequencies.

INTRODUCTION:

In synchronous digital circuits, clock distribution network is crucial part. The clocking networks consume large amount of power in some complex circuits around 20-50% of the whole circuit power, which is not worthy. If the clock power is reduce, it can reduce the total circuit power. The whole power dissipation in a clock network in any CMOS digital circuit, consists of three components: (a) leakage current (b) short circuit power and (c) dynamic power. The leakage current depends on its technology relatively negligible in clock circuit. Short circuit power occurs due to short circuit current through PMOS and NMOS transistors during logic changes, if we keep proper rise time and fall time throughout the clock network minimize the short circuit power component[1].The clock network has very high switching activity ,therefore dynamic power is the dominant factor of power consumption ,so leakage current and short circuit power are negligible. The dynamic clock power dissipation can be mathematically expressed by the relation

$$P=f\ CLVDDVSW \quad (1)$$

where f is the clock signal frequency, CL is the load capacitance, VDD is the supply voltage and VSW is the output swing. If output buffer swing from GND to VDD, then the equation of dynamic clock power becomes

$$P=fCLVDD \quad (2)$$

Frequency scaling, voltage scaling, both voltage and frequency scaling or load capacitance scaling are used at different design abstractions to reduce dynamic power. Supply voltage scaling has been the most adopted approach to power optimization, since it normally yields considerable amount of power savings due to the quadratic dependence of switching on supply voltage VDD[2]. Nowadays frequency is a fundamental parameter for the circuit, it cannot be change but its effects can be reduced by techniques like clock gating and obtain linear reduction in power consumption.

Cite this article as: Saraswathi Thanuja & Mr. S.Lakshmi Kanth Reddy, "Design Methodologies for Reliable Clock Networks", International Journal & Magazine of Engineering, Technology, Management and Research, Volume 5, Issue 10, 2018, Page 22-27.

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If we reducing the load capacitance, which is consistent to achieve the minimal wire length and the minimal buffer power dissipation. Reducing output swing of buffer without reducing supply voltage, which corresponds to a linear reduction in the power dissipation. According to this fact there are various techniques has been suggested for reducing clock distribution power In explain about VLSI scaling methods and low power CMOS circuits and these scaling methods are used to identify the effects of those scaling methods on the power dissipation and propagation delay of the CMOS circuit[3] .In suggest a new problem formulation for low power clock network design that takes rise time constraints imposed by the design into account and then obtain on significantly better result than previous approaches in terms of power dissipation and area.

In discussing about reduced swing clock network and multiple supply voltage schemes for low power applications. In proposed voltage scaling and frequency as well as voltage scaling schemes for reducing power consumption and temperature fluctuations. In describe a buffered H-tree topology technique to distribute the clock signal and to de-skew a clock network .In proposed a half swing clock distribution scheme that allows them to reduce power consumption of clocking circuitry as 76%, because all the clock signal swings are reduced to half of the supply voltage[4] .

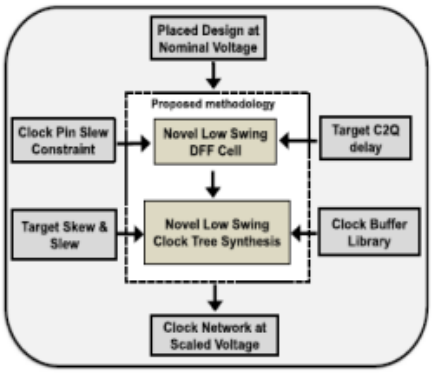

Fig. 1. Summary of the proposed methodology to achieve LS clocking while maintaining the performance requirements.

SUMMARY OF PREVIOUS WORK

Pangjun and Sapatnekar developed a low voltage/swing clock network by utilizing level converters. Both single voltage and dual voltage converters were considered. A theoretical framework was proposed to appropriately position the low-to high level converters throughout the clock tree. The primary limitation of this approach is the conversion of the clock signal back to FS at the last stage of the clock tree. This practice significantly reduces the power savings due to high switching capacitance at the sink nodes. In addition, the slew constraint is considered as a secondary design objective after the merging points are determined during CTS[5]. As observed in this paper, this approach generates a no optimal LS clock tree with reduced power savings. Asgari and Sachdev proposed an LS clock network design methodology using a single supply voltage.

In this approach, single voltage buffers are used to adjust the clock swing throughout the clock network. Similar to, clock voltage is restored to FS at the last stage, thereby significantly reducing the overall power savings. In addition, the clock swing is tuned by relying on the delay of an inverter chain. Thus, the clock swing is highly dependent upon the output load capacitance, limiting the proposed approach to only highly symmetric clock networks, such as H-trees. More recently, low voltage clock networks have been investigated for near-threshold systems that aim enhanced energy efficiency. Seok et al. Investigated the skew characteristics of various clock networks operating at low voltages[6]. The primary emphasis is on symmetric networks, such as H-trees. Automated CTS algorithms were not considered. Tolbert et al. and Zhao et al. proposed a deferred merge embedding (DME)-based CTS method for low-voltage clock networks with an emphasis on clock slew. The proposed technique relies on a computationally expensive procedure of storing multiple solutions in a bottom–up fashion, followed by selecting an optimum solution for each node in a top– down fashion [7].

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The proposed methodology in this paper alleviates all of these issues while targeting low-power systems that still require high-performance capability. Furthermore, the methodology is demonstrated using the existing design automation tools for feasible integration into typical design flows.

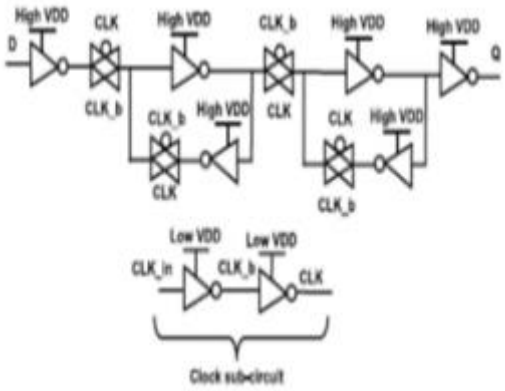

Fig. 2. Typical transmission gate-based DFF topology driven by an LS clock signal.

A. Effect of Low-Swing Operation on Flip-Flop A conventional DFF cell designed for FS operation cannot be used when the clock voltage swing is reduced due to degradations in reliability and power consumption. 1) Reliability: In a typical DFF cell, clock signals drive both nMOS and pMOS transistors. If the same DFF topology is used with an LS clock signal (whereas the data signal is still at FS to maintain performance), the pMOS transistors driven by the clock signal fail to completely turn OFF when the clock signal is high. For example, consider a 45-nm technology with a nominal VDD of 1 V. If the clock swing is reduced to 0.7×VDD, the gate-to-source voltage of the pMOS transistors is −0.3 V, since the data signal is at FS and the inverters within the flip-flop are connected to nominal (FS) VDD. Since −0.3 V is sufficiently close to the threshold voltage of pMOS transistors in this technology, this behavior significantly affects the operation reliability of a traditional DFF cell driven by an LS clock signal. As an example, consider a risingedge triggered master–slave flip-flop. When the clock signal is high, the master latch should be turned OFF. However, due to the LS clock signal, the transmission gate (or tristate inverter) within the master latch cannot completely turn OFF. If the data signal is in a different state than the stored data within the master latch, a race condition occurs, which can producea metastable state. To better illustrate the unreliability of the conventional DFF cells operating with an LS clock signal, a traditional transmission gate-based DFF, as shown in Fig. 2, is simulated with a 45-nm technology node when the clock swing is 0.7 V. Note that the clock signal and the inverted clock signal are internally generated using two inverters. This circuit is referred to as the clock subcircuit, as also shown in Fig. 2. Note that the inverters within the clock subcircuit are connected to a low supply voltage to provide LS clock signals. Since the pMOS transistors driven by the clock signals are not completely turned OFF, internal nodes experience a glitch as high as 400 mV. Furthermore, at the slow corner, the DFF cell fails to correctly latch the data signal [10].

Thus, a new topology is required that can reliably operate with an LS clock signal and an FS data signal. Note that an alternative solution is to integrate a level shifter within the DFF cell to restore an FS clock signal [9]. Thus, the clock signal is restored to FS operation before reaching transmission gates. This approach is similar to the existing level shifting DFF cells for dual voltage systems [8], but the level of the clock signal is shifted rather than the data signal. This approach, however, significantly increases the overall power consumption of the DFF cell due to the integrated level shifter. Thus, the power saved at the last stage of the clock network is lost within the DFFs, making this approach impractical for the primary objective of this paper. 2) Power Consumption: The reliability issue described in Section III-A1 can be fixed by connecting the inverters within the clock subcircuit of a conventional DFF to the nominal VDD, producing a single voltage flip-flop driven by an LS clock signal. In this case, these inverters also function as single voltage, low-tohigh level shifters, and the transmission gates receive FS clock signals.

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The primary limitation of this approach is an unavoidable increase in power consumption due to significant static current drawn by the inverters within the clock subcircuit To better illustrate this behavior, a conventional DFF is simulated when an LS clock signal is applied to the clock pin while the clock subcircuit is connected to a nominal VDD.

PROPOSED SYSTEM

In this work we have used the idea of supply voltage scaling technique for reduce power consumption in clock distribution network. To analyse and compare the performance of clock network with scaled supply voltage and without scaled supply voltage on power dissipation, used two methodologies ie,Case1 and Case2.In Case1 Clock signals are distributed with full scale supply voltage and in Case2 Clock signals are distributed with reduced supply voltage and converted to full scale supply by using some level converters.

TEST SETUP FOR CLOCK CIRCUIT

The main objective of this work is to analyse and compare the power consumption in two clock networks, (a) clock signals are distributed with full scale supply voltage to load and (b) clock signals are distributed with scaled supply voltage.Fig.1 and Fig.2 are shown the setup used for clocknetworks. Case1 is shown in Fig.1 i.e. clock signal is distributed with full scale supply voltage. Most of the clock distribution networks are using H-tree topology for distributing clock signal thought circuit as it reduce the effect of clock skew. Here we took a portion of such H-tree type clock distribution network, which has two loads in the form of D latches, namely DL1(D latch1) and DL2(D latch2).Assume the first load DL1 is nearer toclock source so there is only negligible amount clock skew. But the second load DL2 is far from clock source, since long interconnect length clock skew will be present. During the simulation of such clocking circuit clock skew is made as the form of Resistance Capacitance (RC) network between DL2 and clock source.

The clock distribution network in Case2 is shown in Fig2, here the clock load which is far from clock source i.e. clocking signal to DL2 is distributed with reduced supply voltage for interconnect power reduction .Supply voltage of clock signal is reduced by using H.L.L.C (High to Low Level Converter) at clock source and converted back to original form by using L.H.L.C (L.H.L.C) at clock load. The clock load which is near to clock source, i.e. clock signal to DL1 is distributed with full scale supply voltage, means the supply voltage of clocking signal to DL1 is not reduced.

Here the clock distribution circuits are designed simulated in 180nm technology with 1.8V supply. The clocking signal is given to DL2, i.e.the clock load which is far from clock source is reduced to 1.2V for interconnect power reduction. This reduced value of supply voltage as 1.2V is due to design and operation of delay and power. In order to convert1.8V to 1.2V by using H.L.LC(High to Low Level Converter) shown in Fig.3.The reduced voltage ,ie.1.2V converted back to original form by using L.H.L.C(Low tobHigh Level Converter) Shown in Fig.4.

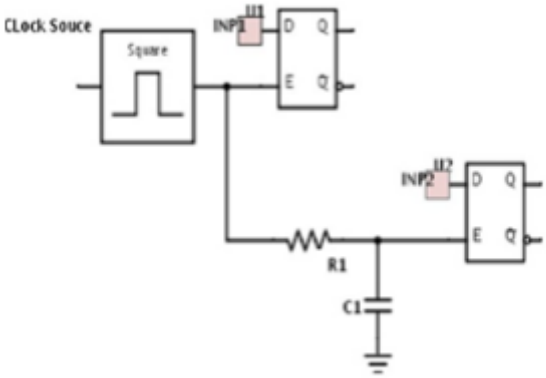

Figure 3: Test setup of clock distribution network with full scale supply voltage

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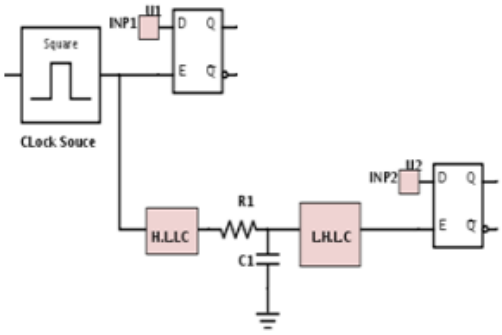

Figure 4: Test setup of clock distribution network with scaled supply voltage

DESIGN OF CLOCK CIRCUITS (CASE1 & CASE2)

Case 1: Clock Distribution Network with Full Scale Supply Voltage In Fig.1 shows the test setup of clock distribution network with full scale supply, here the clock source is used for generating clock signal with 1.8V ,since the loads such as DL1(D latch1) and DL2(D latch2) are operated on supply voltage with 1.8V.These two latches DL1 and DL2 are positive triggered D latches build by using transmission gates and inverters .The circuit of D latch is shown in Fig.3.Here these D latches are require clock signal as well as clock bar signal because D latches are constructed by using transmission gates. In order to develop clock signals we have to use two clock sources. One for clock signal generation and author for clock bar signal generation .The clocking signal which is distributed far from clock source, i.e. between clock source and DL2 have a skew of 40ps.Here this RC network is designed to give delay of 40ps with R=20Ω C=2pF.

Case 2: Clock Distribution Network with Scaled Supply Voltage In Fig.2 shows the test setup of clock distribution network with scaled supply voltage .The operation of this distribution network is also same like clock network with full scale supply voltage. Clockloads, i.e. D latches DL1 and DL2 are positive level triggered requires clock and clock bar signals for their operation.

Two clock signals are generated by using two clock sources. Pair of clock and clock bar signals is directly given to DL1, i.e.the load which is near to clock source. Second pairs of clock and clock bar signals are reduced to appropriate voltage and given to DL2, ie, the load which is far from clock source. Here we have to use two H.L.L.C (High to Low Level Converter) and two L.H.L.C (Low to High Level Converter),one for clock signal and author for clock bar signal .Fig.4 shows high to low level converter for scale down the clock signal from clock source ,this is an inverter circuit with supply voltage of 1.2V.The low to high level converter circuit is shown in Fig.5,which is used for convert and restore back cock signal with full scale supply voltage at load DL2.Both the clock circuits are simulated at different frequencies for power comparison. While simulating at different frequencies, the high to low level converters are designed at every frequency in order to maintain nature of clock signal.

CONCLUSION

A design methodology is proposed for voltage-scaled clock networks operating at a reduced swing. The primary objective is to achieve significant reduction in power consumption without degrading circuit performance. The proposed methodology consists of a novel LSDFF cell and a novel swing- and slew aware CTS algorithm. The proposed DFF cell can reliably operate with an LS clock signal, thereby enabling LS operation throughout the entire clock network. Thus, power savings are maximized. The proposed CTS algorithm ensures that the same clock frequency, skew, and slew as in FS/voltage operation are satisfied. Furthermore, the slew-aware CTS algorithm is sufficiently flexible to target various performance constraints while adapting to the differences in the transistor and interconnect technologies. The entire methodology is integrated into an industrial design flow for automation. Experimental results on largest ISCAS'89 benchmark circuits demonstrate significant reduction in clock power for both 45- and 32-nm technology nodes while satisfying all of the timing constraints.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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