A Novel Configuration for a Cascade Inverter-Based Dynamic Voltage Restorer With Reduced Energy Storage Requirements

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Abstract:

This paper introduces a new configuration for a cascade (H-bridge) converter-based dynamic voltage regulator in which the basic cascade converter is supplemented with a shunt thyristor-switched inductor.

The proposed topology is shown to posses the ability of mitigating a severe and long duration voltage sag with a significantly smaller energy demand from the cascade converter.

A suitable control system is designed, and the operation of the new device is analyzed using electromagnetic transients simulation as well as mathematical analysis.

Simulation and ex-perimental results are presented to demonstrate the feasibility and the practicality of the proposed novel dynamic voltage restorer topology.

Index Terms:

Cascade inverter, dynamic voltage restorer (DVR), multilevel converter, optimization, shunt inductor.

I. INTRODUCTION

VOLTAGE magnitude, waveform, and frequency are the major factors that dictate the quality of a power supply. Faults at either the transmission or distribution level may cause transient voltage sag or swell in the entire system or a large part of it. Also, under heavy load condition, a significant voltage drop may occur in the system. Such voltage variations are not desirable for sensitive loads.

A dynamic voltage restorer (DVR) [1]–[4] is a power-electronic-converter-based device capable of protecting sensitive loads from all supply-side disturbances. The basic operating principle of a DVR as shown in Fig. 1 is to insert a voltage (V_{dvr}) of required magnitude and frequency in series with a distribution feeder to maintain a desired amplitude and waveform for the load voltage (V_l) even when the source voltage (V_s) is offnominal, unbalanced, or distorted. A certain amount of voltage restoration is sometimes possible with purely reactive power injection; however, generally there is also the need to inject real power using a source of dc voltage, such as a battery. In many cases, the real power injection is needed only

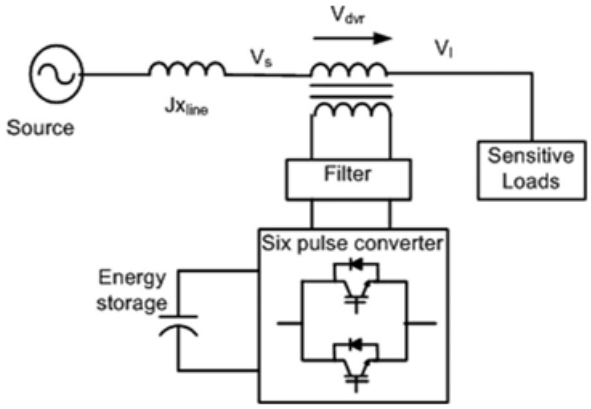

Fig. 1. Schematic diagram of a typical DVR

transiently (i.e., during system disturbances). It then becomes possible to use an energy storage device, such as a capacitor or superconducting inductor, for such energy storage.

Numerous circuit topologies are available for the DVR [5]–[8]. A widely used method is the two-level or multilevel three-phase converter which shares a dc capacitor between all phases. The purpose of this capacitor is mainly to absorb harmonic ripple and, hence, it has a relatively small energy storage requirement, particularly when operating in balanced conditions. The size of this capacitor has to be increased, if needed to provide voltage support in unbalanced conditions. Also, since the capacitor is shared between the three phases, a sag on only one phase may cause a distortion in the injected current waveforms on the other phases.

Another popular converter topology is the H-bridge cascade inverter [9] and [10], one phase of which is as shown in Fig. 2. Converters with this topology are suitable in high-voltage and power system applications due to their modular structure, their ability to synthesize waveforms with better harmonic spectra. The required high-voltage rating can be achieved by cascading (stacking) individual modules of a standardized low-voltage rating rather than custom building the power electronics for each application. The topology also permits the elimination of a converter transformer with further cost savings [6].

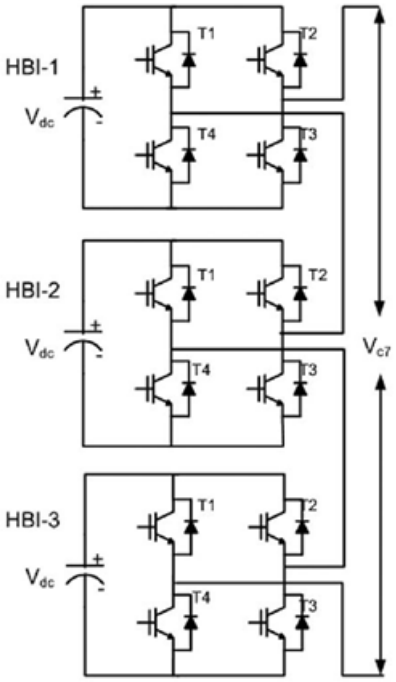

Fig. 2 Seven-level cascade inverter.

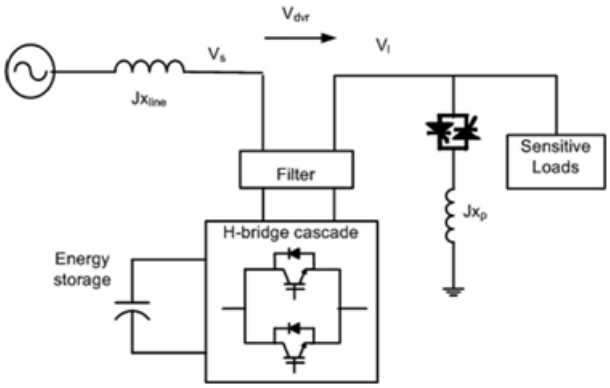

Fig. 3 Schematic diagram of a proposed new DVR.

(STATCOMs) of ratings up to +/- 75 Mvar and ac voltages up to 15 kV [11]. The separate energy storage capacitors in each phase permits efficient single-phase as well as three-phase compensation.

Earlier publications [3]–[7] and [12] have shown that with the appropriate control system, the device can mitigate longer dura-tion sags as the size of the capacitors (energy storage capacity) is increased. It is also known that the sag mitigation is achiev-able with less energy storage for a system with poorer power factor (pf) [8].

This paper introduces a novel modified topology which pro-vides similar performance benefits, but requires significantly less energy storage capability. The proposed DVR exploits the aforementioned property by intentionally decreasing the power factor during a sag with the introduction of a thyristor-switched inductor as shown in Fig. 3. With the means of an appropriate control system, the topology also lends itself to recharging the capacitors to their nominal voltages in a straightforward manner.

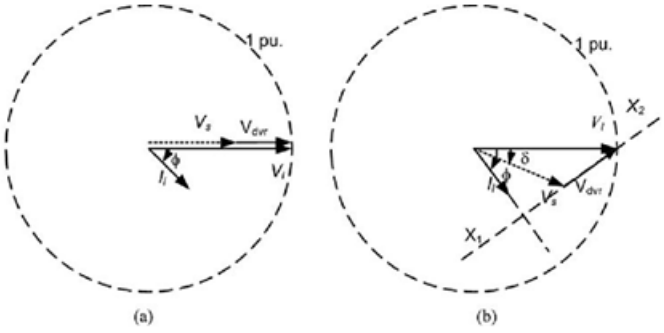

Fig. 4. Vector diagram for compensation of sag. (a) Inphase injection. (b) Zero active power injection.

The viability of the new design and its control is demonstrated in this paper using an analytical formulation combined with comprehensive transient simulation on the PSCAD/EMTDC simulation program. A laboratory hardware prototype of the proposed DVR topology has been built to verify the feasibility and the practicality of the proposed novel DVR topology.

II. DVR OPERATION

A typical DVR [1]–[3], as shown in Fig. 1, is used for voltage correction. When the supply-side voltage V_s changes, the DVR injects a voltage V_{dvr} in such a way that the desired load voltage magnitude can be maintained. The DVR is essentially a voltage-source inverter that produces an ac output voltage and injects it in series with the supply voltage.

Note that the voltage injection also typically results in the supply of real and reactive powers. Reactive power can be supplied without taking energy from the dc-side capacitor; how-ever, the active power must involve the transfer of stored energy. A strategy that permits voltage regulation while minimizing injected active power is attractive because it can prolong the duration over which voltage regulation can be performed.

The vector diagrams in Fig. 4 show the required injected voltage (V_{dvr}) for correcting a given amount of sag. The magnitudes of the supply voltage (with sag) and the load voltage (which is to be maintained constant) are, respectively, V_s and V_l. It is evident that the injected voltage is smallest when it is in phase with the supply voltage as in Fig. 4(a). However, this minimum injected voltage solution is usually not the minimum energy solution. As shown in Fig. 4(b), if the injection is carried out in quadrature with the load current I_l, the compensation is achieved with the injection of zero real power. This compensation is achieved at the cost of an increased magnitude for the injected voltage V_{dvr}. Unfortunately, the ability to provide complete compensation with zero real power is compromised if the voltage sag exceeds a certain maximum limit [8], also defined later by (4).

III. VOLTAGE SAG CORRECTION BY DVR

The series-injected voltage of the DVR (see Fig. 1) is

$$V_{dvr}\angle\alpha = V_l\angle 0 - V_s\angle -\delta \quad (1)$$

where α and δ are the angle of V_{dvr} and V_s, respectively, with the load voltage V_l as the reference. The complex power injection of the DVR is then

$$S_{dvr} = V_{dvr}\angle\alpha \times I_l\angle\phi. \quad (2)$$

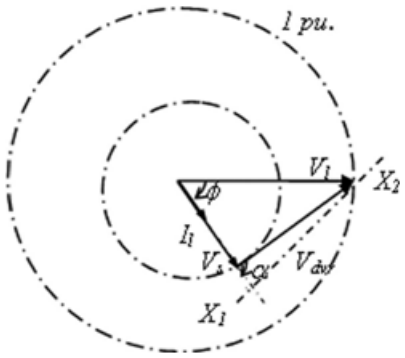

Fig. 5. Minimum real power injection with a violation of (4).

Here, $I_l\angle(\phi)$ is the load current with

$$I_l = \left|\frac{P_l + jQ_l}{V_l}\right| \quad \phi = -\tan^{-1}\frac{Q_l}{P_l}. \tag{3}$$

A. Mitigation Strategy

Earlier work [8] has shown that if the sag is within certain power-factor-dependent limits and the DVR ceiling voltage is large enough, it can be compensated with reactive power injec-tion only. If the ceiling voltage of the DVR is exceeded, the injected voltage angle has to be modified, and more real power is needed. The sag mitigation strategy proposed in this earlier work for the different operating regimes will be summarized. Following this strategy results in the injection of minimal real power.

1) Sag Within the Limit Identified by (4): As shown in Section II, if the DVR injects a voltage V_{dvr} in quadrature with the current I_l, sag compensation can be carried out with the aid of reactive power only. For example, in Fig. 4(b), any sagged supply voltage such as the one shown by V_s, whose magnitude is such that its tip lies on the perpendicular line X_1X_2 can be compensated. Note that the smallest magnitude that the sagged voltage can attain and yet be compensated purely with reactive power injection is the radius of the tangent circle to the line X_1X_2. Hence, the amount of sag (difference between the required line voltage and supply voltage) that can be so compensated is given by (4)

$$\Delta V_{\text{sag}} \le V_l\,(1 - \cos\phi). \tag{4}$$

2) Sag Larger Than the Limit (4): When the sag is larger than the limit from (4), for example, the sagged voltage V_s as shown in Fig. 5, sag correction with reactive power only is not possible. In order to achieve compensation with minimum real power, the projection of V_s on the current must be minimized. To achieve this, V_s must be made to lie along the direction of I_l. The corresponding voltage V_{dvr} injected by the DVR must be at the angle as shown in Fig. 5 which, by simple trigonometry, has a value given by

$$\alpha = \tan^{-1}\left(\frac{V_s\sin\phi}{V_l - V_s\cos\phi}\right). \tag{5}$$

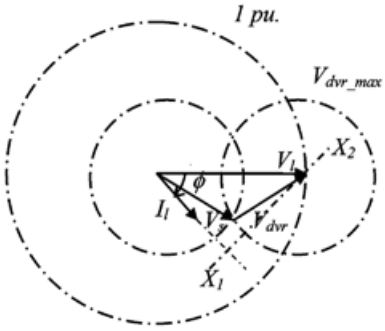

Fig. 6. Minimum real power injection with $V_{dvr\,max}$ 0.6 p.u.

3) Sag Compensation When DVR Voltage Rating is Breached: Although in theory, any sag smaller than the limit indicated in (4) can be compensated. In reality, a much smaller limit may apply due to the maximum-injected voltage rating $V_{dvr\,max}$ of the DVR. With this additional constraint, it can be shown [8] that the maximum sag compensatable by reactive power alone is given by

$$|\Delta V_{\text{sag}}|_{\max} = \min\left(V_l(1 - \cos\phi), \sqrt{V_l^2 - 2V_lV_{dvr\,max}\sin\phi}\right). \tag{6}$$

In this case, the load current I_l can no longer be in phase with the supply voltage V_{s} as shown in Fig. 6 (drawn for $V_{dvr\,max} = 0.6$ p.u.). In this case, the strategy requires some modification, with the injection angle α now being

$$\alpha = \sin^{-1}\left(\frac{V_s\sin\delta}{V_{dvr\,max}}\right). \tag{7}$$

B. Real Power as a Function of Power Factor

It is evident from (4) (with $V_l = 1$ p.u.) that if the voltage sag is less than $(1 - \cos\phi)$, no active power injection is required to correct the voltage. Curiously, this means that for a given sag magnitude, the poorer the power factor is, the easier it is to compensate without real power injection. The required DVR-injected active power is plotted against the voltage sag of the supply-side voltage (with $V_{dvr\,max} = 1.0$ p.u.) as shown in Fig. 7 for different power factors. The DVR's injected voltage rating is large enough (1.0 p.u.) so that this limit is not exceeded in the cases considered. Four different load power factors (0.5, 0.6, 0.8, and 0.9 p.u.) are considered in the plots.

Note that (4) and Fig. 7 show that it is possible to compensate larger sags with pure reactive power injection, for poorer power factor loads. The proposed new strategy will use this fact to temporarily reduce the power factor during compensation in order to extend the range of sags for which real-power-free sag compensation is possible.

IV. PROPOSED DVR CIRCUIT CONFIGURATION

As shown in (4) and Fig. 7, it is clear that the compensation can be done with smaller energy storage and with smaller injected real power for loads of poorer power factor. This suggests a strategy could be developed where the power factor is

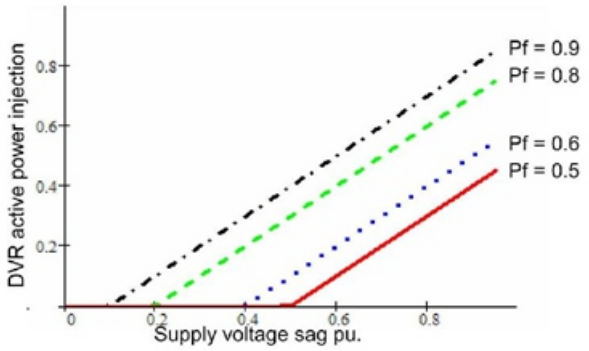

Fig. 7. Injected DVR active power versus the voltage sag for four different power factors.

deliberately reduced to achieve compensation with purely reac-tive power. As most industrial loads are lagging power factor loads, this would require placing shunt inductance at the load. Note that placing an in-ductor in parallel with a leading power factor load will actually improve the power factor if the magni-tude of the inductive impedance is smaller than the capaci-tive reactance. This is contrary to the requirement of deliberate re-duction of the power factor. However, reducing the load's power factor is contrary to proper distribution system practice. Hence, this reduction of power factor should only be carried out when the DVR is compensating sags.

The proposed approach to achieve this objective is shown schematically in Fig. 3. It can be seen that the proposed con-figuration differs from a typical DVR as shown in Fig. 1. The H-bridge inverter topology is em-ployed because of the advan-tages discussed earlier [6], [8]. In addition, a thyristor-switched inductance is added across the load. The thyristor switch can be turned on to connect an inductance in shunt with the load to lower the power factor seen from the system side. Note that the thyristor switch is off during nor-mal operation, thereby main-taining the normal (high-er) power factor during normal opera-tion.

A. Voltage Sag Correction by Proposed DVR

It can be also observed from Fig. 7 that for a system with poor power factor, the DVR can handle larger sags without injection of active power to the system. The proposed DVR sag correction is built on the afore-mentioned observations.

During the sag period, the shunt inductance is switched into the circuit and lowers the power factor as seen by the source side. Considering the inductor-load parallel circuit as the "new" load, the net power factor angle is

$$\phi_{\text{new}} = \tan^{-1}\left(\frac{R_l^2 + X_l\,(X_l + X_p)}{R_l + X_p}\right) \qquad (8)$$

where X_l , X_p , and R_l are the load reactance, the shunt reac-tance, and the load resistance, respectively. The maximum com-pensatable sag with pure reactive power injection is

$$\Delta V\text{sag} \le V_l\,(1 - \cos\phi_{\text{new}})\,. \qquad (9)$$

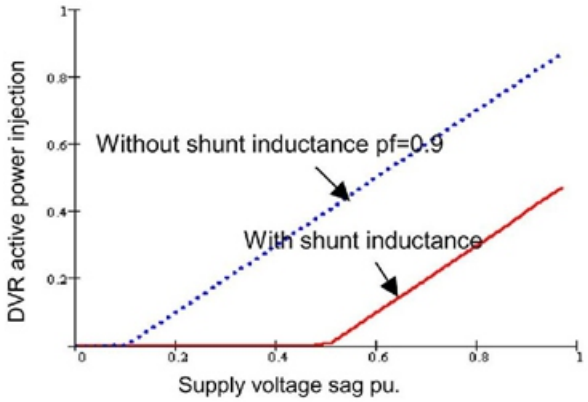

Fig. 8. DVR active power versus the voltage sag for the system without and with shunt inductance.

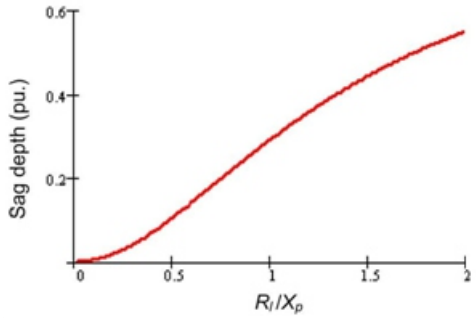

Fig. 9. Sag depth which can be mitigated without injecting real power for a different Ri=Xp ratio.

Note that this new approach mitigates larger sags without en-ergy injection, but in addition, those sags which require energy injection can be compensated over a longer duration as shown in Fig. 8.

In Fig. 8, the required DVR-injected active power is plotted against the voltage sag of the supply-side voltage (with $V_{\text{dvr max}}$ = 1.0 p.u.) for two cases, first for a system with 0.9 power without the shunt inductance and the second with the same system but with the shunt inductance added if the sag exceeds 0.1 p.u. The considerable real power savings from the proposed approach are clearly evident.

Fig. 9 considers the worst case of a purely resistive load Rl (unity power factor) load and shows the sag depth which can be mitigated without injecting real power for different Rl / Xp ratios. This information can be used to select the value of the required shunt compensation Xp. From Fig. 9, it is clear that as the Rl / Xp ratio goes higher, more severe sag can be mitigated without the injection of real power.

It should be noted that for a proper economic comparison, the tradeoff between the cost savings due to the reduced energy storage requirement and the additional cost of a shunt reactor and power-electronic switch must be properly considered.

V. CONTROL METHOD

The control system for the new configuration is easily adapted

(9)from the control system for the DVR proposed ear-lier in liter-

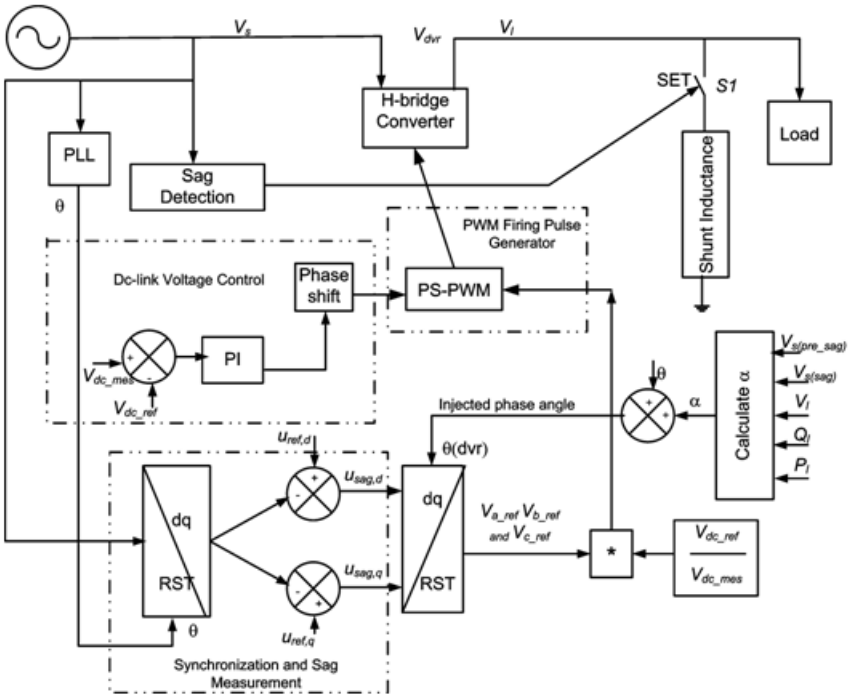

Fig. 10. Control structure of DVR with rotating dq reference.

ature [8]. The main aspects of the control system are shown in Fig. 10 and include the following blocks: synchronization and voltage measurement at sag detection, injected voltage phase-angle calculation, and firing pulse generation. These blocks are as discussed in [8]. The essential difference from the earlier work is the additional step of switching the shunt inductance and the dc-link control voltage on and off. The control opera-tion, including the aforementioned two modifications, will be discussed.

A. Sag Detection

The sag is calculated by comparing the long-term steady-state value (in d, q components) of the supply voltage with the instan-taneous voltage (d, q components). This allows for detection of symmetrical and nonsymmetrical sags, as well as the associated phase jump. In order to prevent undue control action, the un-dervoltage is only considered to be sag if it exceeds a certain threshold as in (10)

$$|u_{\mathrm{sag},dq}| \geq (u_{\mathrm{threshold}}) = 0.05 \text{ p.u.} \qquad (10)$$

where

$$|u_{\mathrm{sag},dq}| = \sqrt{(u_{\mathrm{ref},d} - u_{s,d})^2 + (u_{\mathrm{ref},q} - u_{s,q})^2}. \qquad (11)$$

$u_{\mathrm{ref},d}$ and $u_{\mathrm{ref},q}$ are the reference values for the d and q voltages. If sag is detected, $S1$ is closed. As a result of the introduction of the shunt inductance, the system will have a new load power factor as expressed by (8).

B. DC-Link Voltage Control

While not in sag-compensation mode, a secondary (slower) dc voltage regulation loop ensures that the capacitors are charged to the rated voltage. This is achieved by marginally phase shifting the carrier waveform of the individual H-bridge inverter so that real power is absorbed (for voltage increase) or delivered (for voltage decrease) as shown in Fig. 11. The phase shift was applied to the carrier waveform rather than to the modulating waveform because this simplifies the control as it permits the modulating waveform to be the same for all of the cascaded H-bridges in each phase.

VI. SIMULATION RESULTS

The proposed control system for the DVR is validated in this section via electromagnetic transients simulation using the PSCAD/EMTDC simulation program. The test system is a 115-kV transmission line that brings the power to the local distribution bus where it is stepped down to 13.8 kV with a 100-MVA transformer that has a leakage impedance of 10%. The DVR is connected between the distribution and supply buses. In this paper, the load is represented by a simple R-L series equivalent rated at 13.8 kV, 32 MVA at 0.98 load power factor. More complex loads have not been considered. Voltage regulation performance is simulated for a 40% voltage sag, which is applied by connecting a suitable resistance to ground on the source-side bus of the DVR (where voltage V_{s} is measured in Fig. 3). Note that applying a sag in this manner causes, in addition to the magnitude reduction in the source

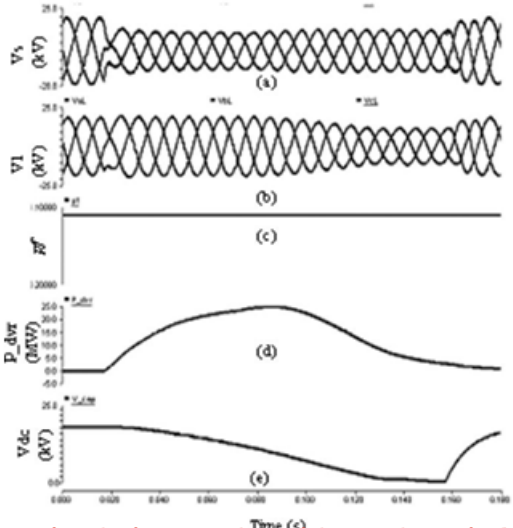

Fig. 11. Simulation results without shunt inductance in the circuit for 40% seven-cycles sag.

side voltage, a phase shift due to the additional current source inductance. Results are shown first for the method without shunt inductance and then for the new method which includes the shunt inductance.

Fig. 11 shows the sag compensation performance for the topology without the shunt inductance for a seven-cycle sag. The first two sets of curves [Fig. 11(a) and (b)] show the supply-and load-side voltages. It can clearly be seen that apart from a transient on sag application and removal, the load voltage is maintained at 1 p.u. during first five sag cycles. However, as this approach requires an amount of real power injection [Fig. 11(d)], the dc capacitor voltage rapidly decays as in Fig. 11(e). Note that for a sag duration longer than five cycles, the capacitor would discharge completely, thereby eliminating the DVR's ability to control the sag [Fig. 11(b)].

In contrast, Fig. 12 shows the corresponding curves for the proposed DVR configuration with the introduction of the shunt inductance ($Rl / Xp = 0.8$), which reduces the load power factor from 0.98 to 0.78 [Fig. 12(c)]. The sag in this case is maintained for 14 cycles. The ability of the proposed method to mitigate longer duration sags is evident. As can be seen, approximately 100% sag compensation is achieved for the first 12 cycles. Then, due to capacitor discharge, the compensation ability is compromised and only 85% sag compensation is possible at 14 cycles. As seen from Fig. 12(d) and (e), the sag compensation is achieved with the injection of reduced real power, resulting in slower discharge of the capacitor voltage.

Even longer sags can be compensated by increasing the inductance's Rl / Xp ratio. For $Rl / Xp = 1.3$ (load power factor 0.6) Fig. 13 shows that the same 14-cycle sag can be completely compensated with a very small amount of real power injection and, hence, an approximately constant dc voltage. Note that an additional control loop as described in Section V-B is used

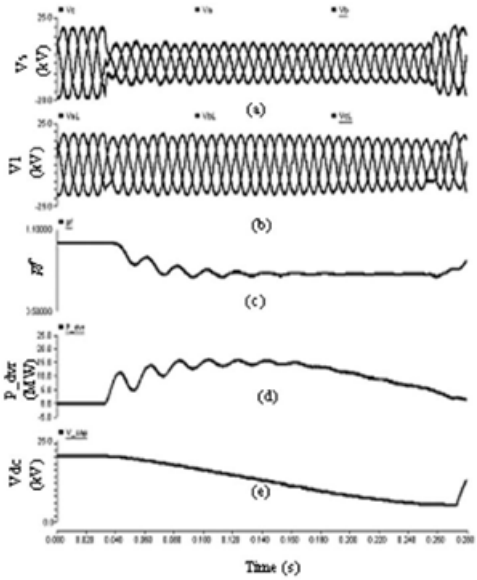

Fig. 12. Simulation results for the proposed DVR configuration for 40% seven-cycles sag correction with (Rl=Xp = 0:8).

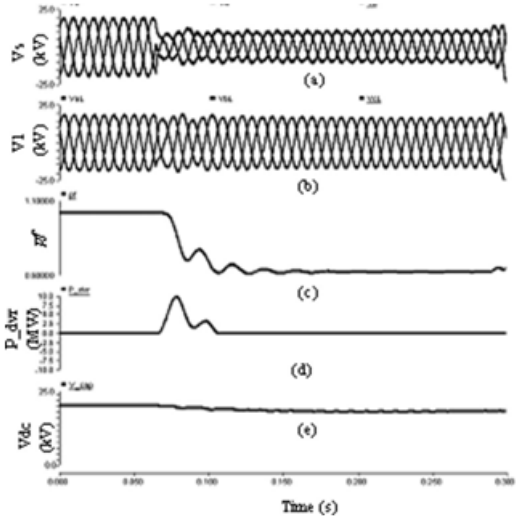

Fig. 13. Simulation results for the proposed DVR configuration for 40% seven-cycles sag correction with (Rl=Xp = 1:3).

to restore the capacitor voltage which was reduced during its compensation duty. Fig. 14 shows the restoration of the dc-link voltage due to this control action. In this case, an extreme sag of 80%, which is in excess of the compensation capability, was applied so as to totally drain the capacitor. After the sag was re-moved, even in this most extreme case, the control system was able to satisfactorily restore the voltage on the capacitor to its rated value.

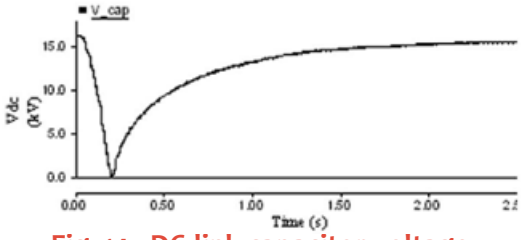

Fig. 14. DC-link capacitor voltage.

TABLE I
PARAMETERS OF THE TEST SETUP

Item	Values
Line voltage	40V /60 Hz
Line resistor R_{line}	1 ohm
Line inductance X_{Line}	0.5 ohm
Filter inductor L_f	2 mH
Filter capacitor C_f	15 μF
Load inductance L_l	(1 to 60) mH
Load resistor R_l	20 ohm
DC link capacitor (per H-bridge module)	2600 μF
Switching frequency	1950 Hz
Load power factor	(0.6 to 0.99)
Filter cut-off frequency	920Hz
Shunt inductance L_p	40 mH

VII. TESTS ON A LABORATORY PROTOTYPE

A laboratory prototype of the proposed DVR was con-structed for the experimental verification of the approach developed in this paper. Due to the limited hardware setup, only a single-phase five-level converter DVR system could be constructed. Each phase of a three-phase system operates independently of the other phases and, hence, the single-phase demonstration setup is completely adequate to demonstrate feasibility. The parameters of the test setup are given in Table I. The load in this case is a series R_L branch.

Fig. 15 shows the recorded oscilloscope voltage measure-ments for the supply and load sides for a 12-cycle sag appli-cation. In this case, the switched shunt inductance reduced the load power factor from 0.95 to 0.60 during the sag event. The voltage is entirely compensated during the entire sag interval.

Fig. 16 shows experimentally obtained results when the sag duration is extended to 60 cycles. A data-acquisition system was used to obtain synchronized measurements of all volt-ages and currents. Any other quantity of interest, such as the load's power factor, was then easily reproduced by postpro-cessing. It is confirmed that the sag is entirely compensated

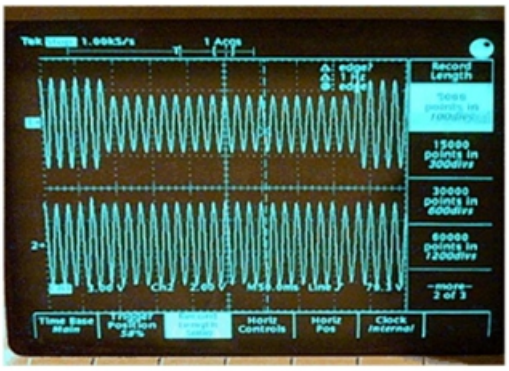

Fig. 15. Experimental results for 12-cycles 40% supply voltage sag and miti-gate load voltage waveforms.

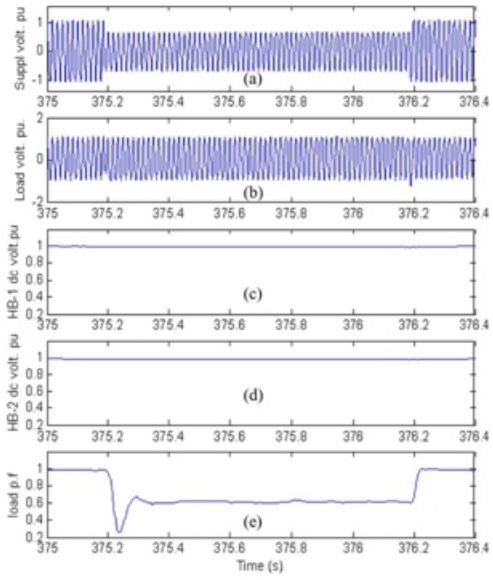

Fig. 16. Experimental results for compensation of a 60-cycle 40% sag.

[Fig. 16(a) and (b)]. By observing the capacitors' dc voltage across each H-bridge [Fig. 16(c) and (d)], it is evident that the sag mitigation was achieved with zero real-power injection and the controls were able to maintain equal and constant dc voltages across the two H-bridge of the five-level converter. Fig. 16(e) also clearly shows the load power factor change from 0.95 to 0.6 during the sag compensation process.

VIII. CONCLUSION

DVRs constructed using the cascade inverter topology are well suited to compensating sagged voltages at customer loads. The modular structure of the cascade inverter, together with some limited energy storage capacity available on its several capacitors, makes it suitable for single-phase as well as three-phase sag compensation.

For high power factor loads, sag compensation often requires real-power injection using the stored energy on the dc capaci-tors. However, for loads of sufficiently poor (low) power fac-tors, the compensation can be carried out with zero real power injection for a relatively large sag range. This property is ex-ploited in the method proposed in this paper which connects a thyristor-switched inductor branch during sags to intention-ally reduce the power factor. This permits the DVR's operating range and compensation interval to be considerably extended.

In addition, the proposed control system is able to minimize the real-power injection and, thus, extend the compensation range in situations where sag compensation does require real-power injection.

The sag compensation performance of the new topology is exhaustively confirmed through electromagnetic transients sim-ulation and through tests conducted on a laboratory prototype DVR.

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