STUDY OF VARIOUS LOW POWER AND LOW LATENCY CARRY SELECT ADDERS

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Abstract:

Adders are the most basic arithmetic digital operation to carry out two or more binary numbers and the results of that output addition is n+1. The optimally designed CSL sections interleaved evenly in the mixed-radix CLA network to boost the performance of the reverse converter well above those designed based on a homogeneous type of carry propagation adder. The logical effort characterization captures the effect of circuit's fan-in, fan-out and transistor sizing on performance, and the evaluation shows that our survey leads to the fastest design. This paper demonstrates the survey of various types of low power and low latency carry select adders.

Key words: Adders, low power, low latency, CSLA, CLA, RCA.

I.Introduction

In a hybrid CLA/CSL circuit, the selected carry signals and sum bits are generated simultaneously by the cooperative execution of CLA and CSL networks. The selected carries are generated by a CLA tree without back propagation.

The number of carry outputs to be generated is significantly reduced with regular interleaves of CSL sections. The sum bits are computed in sections by the CSL Conventionally, each section of a CSL is implemented with dual RCA blocks with the constant carry-in of 0 and 1, respectively.

Due to the anticipatory parallel computation, once the carry signal for the local section is generated by the CLA network, the corresponding carry-select adders will choose the correct sum and produce the output directly.

In electronics, adder is a digital circuit that performs addition of numbers. To perform fast arithmetic operations, carry select adder (CSLA) is one of the fastest adders used in many data- processing processors.

The structure of CSLA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate – level modification is used in order to reduce the area, delay and power of CSLA. Based on the modifications, 8-bit, 16-bit, 32-bit and 64-bit architectures of CSLA are designed and compared. in order to reduce the area, delay and power of CSLA. Based on the modifications, 8-bit, 16-bit, 32-bit and 64-bit architectures of CSLA are designed and compared.

In this paper, conventional CSLA is compared with Modified Carry select adder (MCSLA), Regular Square Root CSLA (SQRT CSLA), Modified SQRT CSLA and Proposed SQRT CSLA in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA.

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications.

Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design. Completely mixed-radix carry generation trees are analytically obscure to unification with the CSL sections for hybrid CLA/CSL due to the immense number of complex formations that could be enumerated. The use of mixed radix cells within the same stage can easily annihilate the regularity and unnecessarily complicate circuit and layout optimizations.

Therefore, it will only be considered on a sparse number of leave cells after the optimal regular mixed radix tree has been established and provided its use will reduce the depth of the tree with minimal impediment on layout regularity. The speed of the hybrid CLA/CSL architecture is minimized when the critical delay of the CLA network is commensurate with that of the CSL sections.

Therefore, for speed optimization, the block factor for the CLA complex gates at each stage of the hierarchy can be optimized to tailor to the optimal block length of CSL based on the implementations of the RCA and multiplexer logics. The RB encoding has been beneficially exploited in the RCA for the CSL circuit.

Transistor-level circuit design techniques have been applied to devise a new area and power-efficient add-one circuit for the CSL adder.

On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer.

Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but but longer delay of RCA and large area with small delay of Carry Look Ahead adder.

II.OBJECTIVES

1. In microprocessors, millions of instructions per second are performed. So, speed of operation is the most important constraint. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. In order to increase the speed of addition the delay has to be reduced.

2. Area is the most important factor that has to be considered while designing any digital circuit using VLSI technology. The area utilized by the circuit on VLSI chip depends on the number of gates used in the circuit. Hence, gate count must be as less as possible to have an area efficient adder circuit.

3. Energy is our limited resource, and power is the rate at which we consume that resource. Design of a digital circuit that consumes less power is one of the most challenging areas of research in integrated circuit design. Hence, there is a need to design an adder circuit that consumes low power.

4. Latency refers to a short period of delay (usually measured in milliseconds) that occurs during the propagation of the signal from one gate to other gate. This delay will be high if the number of gates increases. To increases the speed of circuit latency must be less.

III.PROBLEM IDENTIFICATION:

In VLSI system design area and power efficient high speed logic systems are most important factors. In digital systems, the speed of addition is limited by the time required to propagate a carry through the adder.

The sum of each bit position in an elementary adder is generated sequentially and after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many systems to overcome the problem of carry propagation delay by generating multiple carries and then select a carry to generate the sum.

But the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin = 0 and cin=1,then the multiplexers are used to get final sum and carry.

The following are the problems that are identified in existed adder circuit:

1)Area efficiency is less
2)Gate delay is increases
3) Latency is increases
4)Power consumption is more

IV.TYPES OF ADDERS

Basic Half-Adder

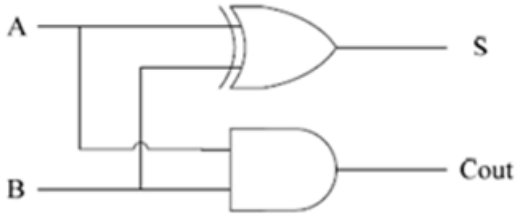

Fig-1: Half adder

Dual Half-Adder to form a full adder

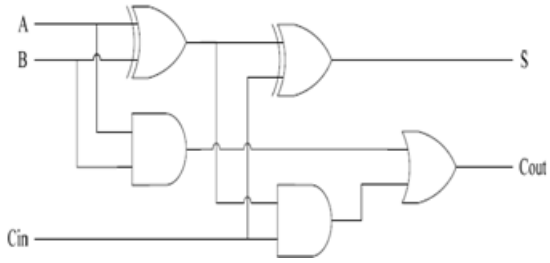

Fig-2: Full adder

If Cin is "slow" 2 gate delays to propagate to Cout.

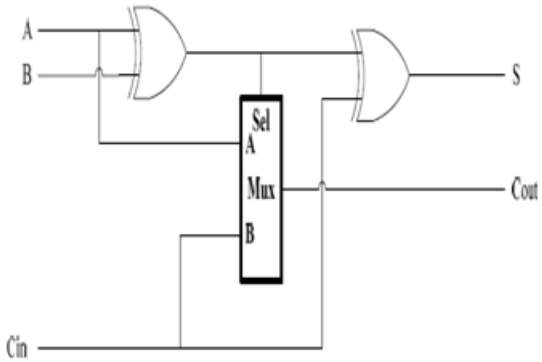

Fig-3: Full adder implemented with mux.

A full adder with a speed carry path as shown in figure below.

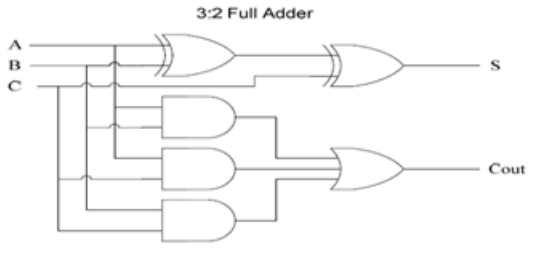

Fig-5: 3:2 Full adder.

Symmetrical propagation to Cout when A, and C inputs are simultaneous.

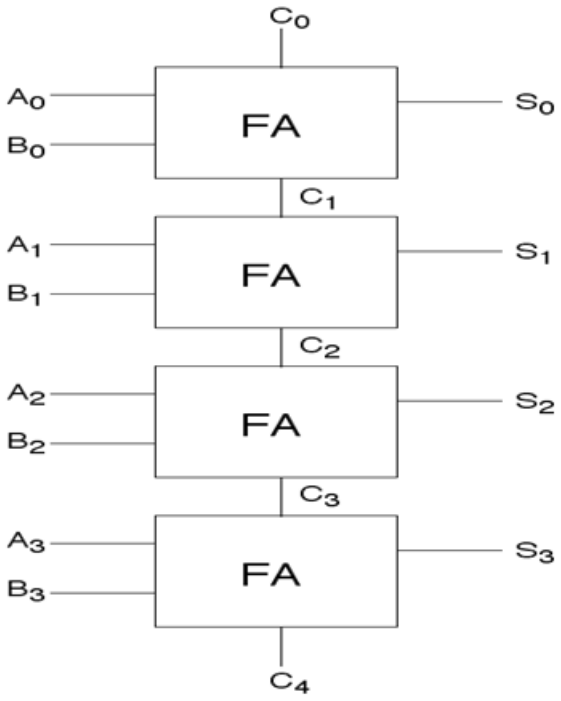

Fig-4: 4-bit Ripple Carry Adder

When Ao...An and Bo...Bn are presented at the inputs the output is not immediately valid. After some propagation delay the outputs of the first adder, So and C1 become valid. S1 and C2 do not become valid until some propagation delay after C1 becomes valid because they depend on C1. Likewise, S2 and C3 do not become valid until some propagation delay after C2 becomes valid. The carry ripples through each stage of the circuit until the outputs of the last full adder become valid. Block diagram of 8 bit regular carry select adder is shown in the fig: .It consist of three 4-bit ripple carry adders (RCA-1, RCA-2, and RCA-3)and one 2:1 multiplexer(Mux).

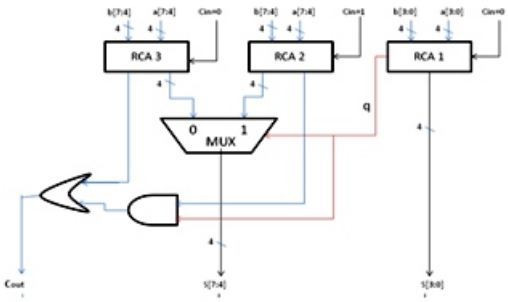

Fig-6: 8-bit CSLA

Inputs to all ripple carry adders are given at a time. RCA-1 is used to calculate the sums[3:0] of lower nibble bits of a, b i.e., a[3:0],b[3:0] as taking initial carry input cin=0. RCA-2 calculates the sum of upper nibble bits of a, b assuming carry to be zero i.e., C=0. RCA-3 calculates the sum of upper nibble bits of a, b assuming carry to be 1 i.e., C=1. The outputs from RCA-2 and RCA-3 are given as an input to the 2:1 multiplexer.

V.COMPARATIVE RESULTS:

Sl. No.	Adders		Delay (ns)	Area
1.	16-bit	Regular	16.27	43
		Modified	14.67	47
		Regular	20.96	90
2.	32-bit			
		Modified	18.83	102
3.	64-bit	Regular	33.85	189
		Modified	23.71	212
4.	128-bit	Regular	42.23	439
		Modified	35.29	441

VI.CONCLUSION

In this paper we demonstrate study of low power and low latency adders are listed and the above adder can implemented in any cadence tools. Finally we conclude that adders are the most important circuits in digital systems. Hence finally we have given some comparative results worked with different CAD tools.

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