ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Cadence Based Design of Channel Tapering Of Three Stage Amplifier for Maximum Gain

B. Jyothsna
M.Tech Student,
Sree Nidhi Institute of Science and Technology.

Dr. N.S. Murti Sarma
Professor,
Sree Nidhi Institute of Science and Technology.

Abstract:

A Low-noise amplifier (LNA) is typically the first active block in the receive path of communication transceivers. Since the signal received by the antenna is usually a weak signal, so it has to be amplified. In this work body biasing technique is introduced to improve the noise figure and channel tapering technique is used to increase the gain of a particular amplifier. Thus, two main characteristics of any LNA are its gain and its noise performance. Other important design parameters are input return loss, stability, frequency of operation, bandwidth, and in some systems linearity. Similar to any analog circuit, there are different trade-offs among these performance parameters which complicate the design of an LNA. A prototype 4 GHz LNA is implemented and simulated in cadence in 0.18um CMOS technology. The LNA achieves a noise figure of 10 dB and maximum gain of 21.4 dB while consuming 2.458 mW from a 1.8 V supply.

Key words:

Signal integrity, pre – layout simulation, noise figure, channel tapering, trade-off.

I.INTRODUCTION:

Low-noise amplifiers (LNAs) are one of the important building blocks of wireless receivers. LNA design parameters such as gain, noise figure, linearity, input matching, and stability are important metrics and typically affect the overall performance of the receiver. While many of these trade-offs are due to the nature of the circuit and are inevitable, it is desirable to decouple the effects of each parameter on the others.

In this work, body biasing is introduced as a technique to enhance the linearity, to improve the noise figure and to provide gain variation. These techniques are presented in the context of a three-stage LNA. By applying body biasing in each stage, noise figure, gain variation and linearity of the overall amplifier are adjusted almost independently.

II.MULTI STAGE LOW NOISE AMPLIFIER :

In general, in a receiver which is composed of several blocks in cascade, the first block has the dominant role on the noise performance of the systems their noise contribution is attenuated by the gain of their preceding stages (Friis' equation [3]). Gain variation is another important feature which is essential in many communication systems especially in wireless transceivers. The reason behind this is the received signal level can fluctuate a lot depending on the location of the receiver with respect to the transmitter. Usually the sinusoidal signal received by the antenna will be a weak signal so this signal has to be amplified.

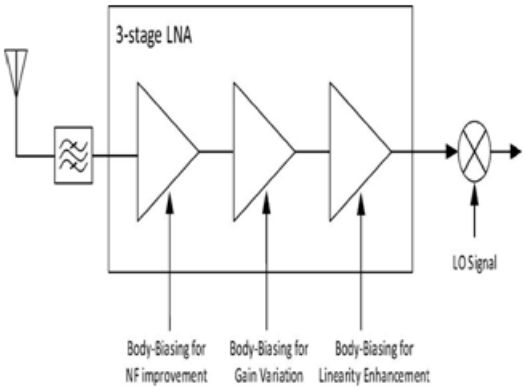

Figure 1) Block diagram of three stage LNA [1]

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

To maintain the signal integrity, the amount of noise that is introduced to the amplifier should be as low as possible. For typical LNA gain of 15 to 20 dB, usually 2 to 3 stages of amplification is required. In this project we have considered three stages of amplification.Here, three stages of amplification is done. First stage is for noise figure improvement, second stage is for gain variation and third stage is for linearity enhancement.

III.SCHEMATIC OF PROPOSED THREE STAGE LNA:

The existed schematic of three stage LNA has shown in figure3.1In this project, investigation of the application of body biasing in various stages of a three-stage LNA to improve noise figure, enhance linearity, and provide gain variation has been done. Here the approach in the context of a three-stage LNA in which body biasing is applied to the first, second and third stage of the LNA to improve the overall noise figure, provide gain variation, and enhance the linearity, respectively. Although the proposed approach is presented in the context of a three-stage LNA, it can be readily generalized to a multistage LNA with more than three stages.

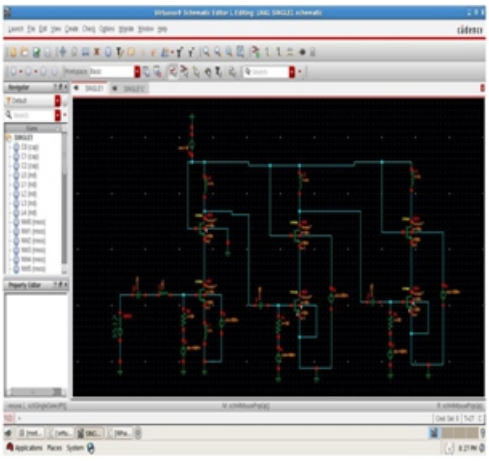

Figure 2) schematic of proposed three stage LNA In which body biasing is applied to the first, second and third stage of the LNA to improve the overall noise figure, provide gain variation, and enhance the linearity respectively.

IV.EXPERIENTAL RESULTS:

Three stages of Low Noise Amplifier has built in cadence tool in virtuoso platform in which body biasing and channel tapering techniques are introduced.

In this work the proposed schematic has been simulated in cadence tool in180nm technology in which each stage is simulated individually.

A. FIRST STAGE:

The existed schematic of three stage LNA has shown in figure3.1In this project, investigation of the application of body biasing in various stages of a three-stage LNA to improve noise figure, enhance linearity, and provide gain variation has been done. Here the approach in the context of a three-stage LNA in which body biasing is applied to the first, second and third stage of the LNA to improve the overall noise figure, provide gain variation, and enhance the linearity, respectively. Although the proposed approach is presented in the context of a three-stage LNA, it can be readily generalized to a multistage LNA with more than three stages.

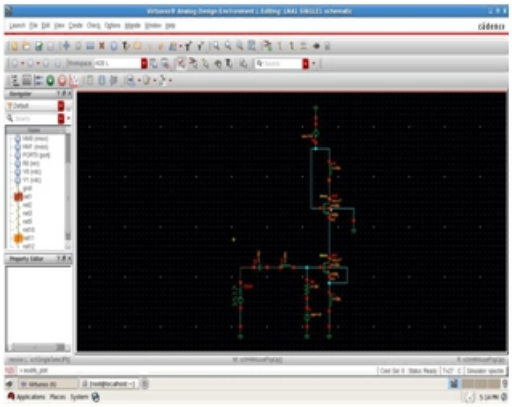

Figure 3) schematic of first stage of LNA

Figure 4) simulation process of first stage

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

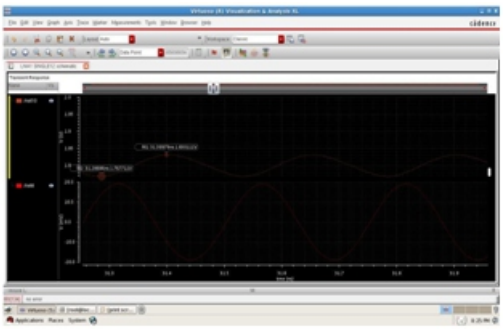

Figure 5) output voltage of first stage

The first stage of body biased three stage LNA is as shown in Fig 3, body biasing is applied at the below transistor where the body terminal of the particular transistor is applied to 300mv of voltage instead of connecting the terminal to ground. The operating frequency that has applied is 4GHz and the amplitude is -30db. Processing of simulation is as shown in Fig 4.The output waveform is observed in the window of visualization and analysis XL. Here, it is observed that the output voltage of the first stage of the LNA is approximately 9mv.

B. ADDING SECOND STAGE:

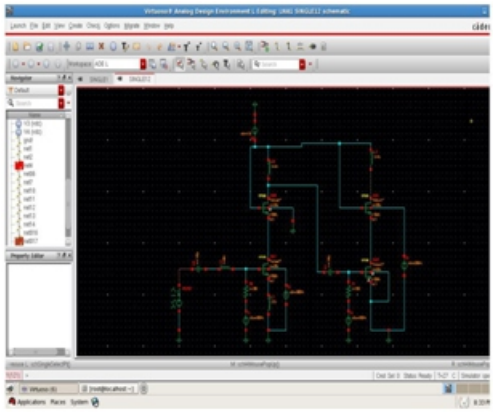

Figure 6) schematic of second stage of LNA

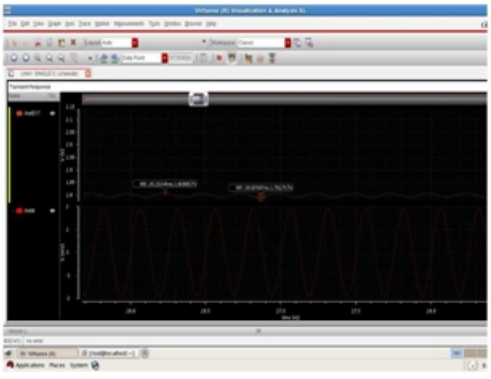

Figure 7) output voltage of second stage

Here, it is observed that the output voltage of the second stage of the LNA is approximately 16mv while the input voltage is 4mv.

C. THREE STAGES OF LNA:

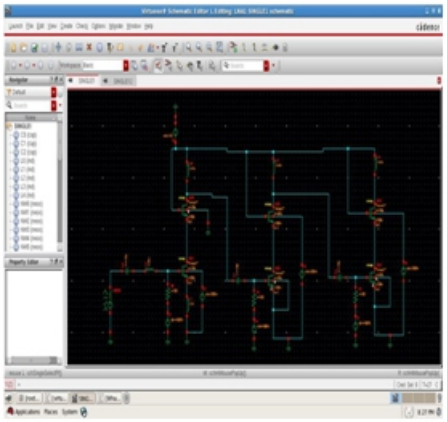

Figure 8) schematic of body biased three stage LNA

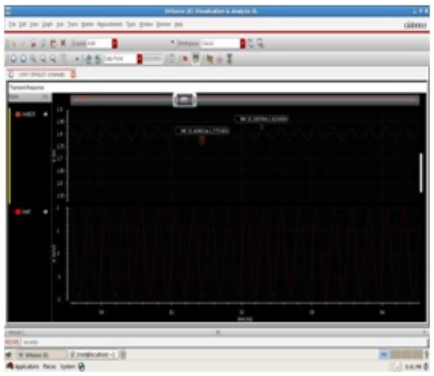

Figure 9) total output voltage of three stage LNA

Similarly the third stage is also added to the second stage, the total amplification of output voltage is approximately 47mv i.e almost ten times of the input voltage that is 4mv. This means that the applied input voltage has been amplified stage by stage and finally at the third stage the input voltage has amplified almost ten times nearly 47mv of the particular input voltage that is 4mv.

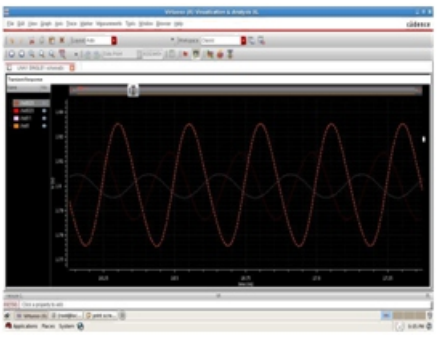

Figure 10) three output voltages

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Here, the input voltage that has been applied is 4mv. In the first it has been amplified up to 9mv, in the second stage it has amplified up to 16mv and similarly in the third stage that is last stage, the input voltage finally amplified to 47mv i.e. nearly 10times of the input voltage. Gain will be 20log (47/4) = 21.4 dB.

A. Noise figure:

Fig 11 shows the plot of the noise figure of the LNA as the bias2 voltage in the first stage Fig 3 denoted as, is varied from-1 V to +1 V. As it can be seen from the figure, when -1 V,

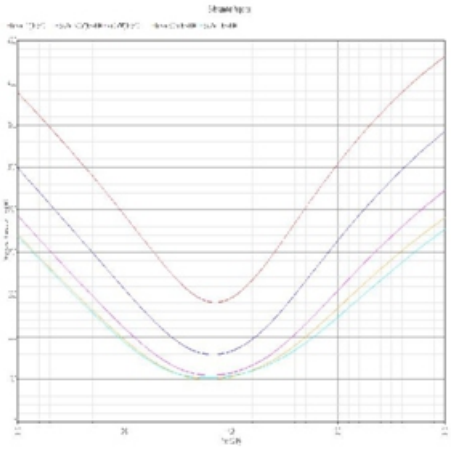

Figure 11) Variation of NF at 4 GHz with bias2 changes from -1 to 1V in first stage.

The noise figure is around 5.1 dB at 4 GHz while with +1 V, the noise figure is about 3.8 dB, i.e., an improvement of 1.3 dB. These measurements confirm that the overall noise figure can be 10db from Fig11. Noise figure measurement results of the prototype channel tapering body-biased LNA for four different values. Noise figure of a particular amplifier is defined as the signal to noise ratio. It is advisable to be as high as possible.

B. power consumed:

The following are general steps common to all the types of power measurements.

i.In the Analog Design Environment (ADE), set up the simulation stimulus file location, and other simulation parameters that must be assigned. This includes setting up simulation for an extracted cell if necessary.

ii.In the ADE, select outputs – save all as shown in figure 4.17. A save options window will appear.

iii.In the save options window, for "select signals to output(save)", "select device currents (currents)" and "select power signals to output(pwr)", click on the appropriate check boxes i.e "All", depending on what power signals are of interest. Click OK to apply the changes.

iv."All" will save all available power waveforms. This option uses the most memory and may slow simulation, however for small circuits, it is not noticeable.

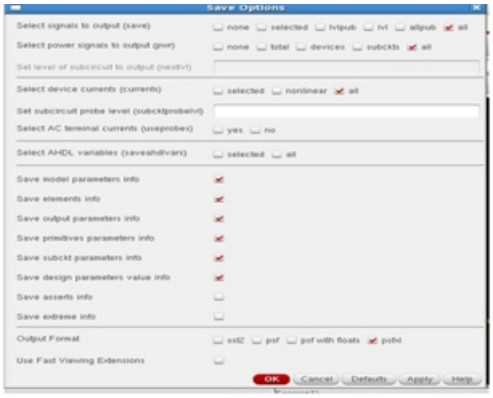

Figure 12) save options window, configured to save all pwr waveforms

v.Run the simulation. If we selected an output to be plotted, the waveform window will appear. If we don't want to plot any outputs, we can open the waveforms window from ADE by selecting Tools – waveform.

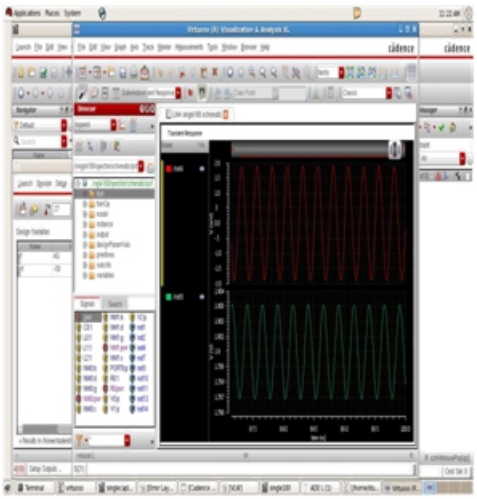

Figure 13) visualization & analysis XL window

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Figure 14) waveform database window

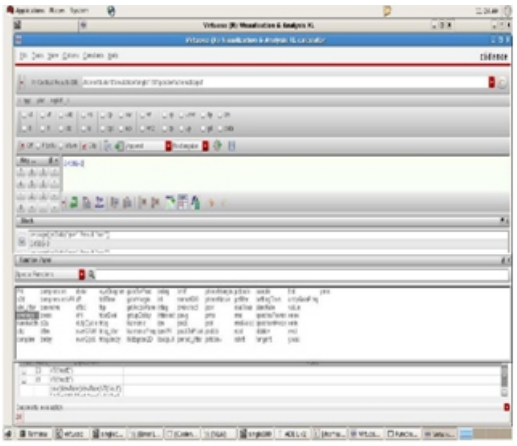

Figure 16) power window.

vi.In the waveform window, select Browser – Results – open results. At the very left side of the Results Bowser, click on the name of the cell view from which we are simulating. Note that multiple cell views may appear depending on past simulations we have conducted on the cell.

vii.Click psf. We are doing transient analysis so click on the tran – pwr in the visualization & analysis XL window .

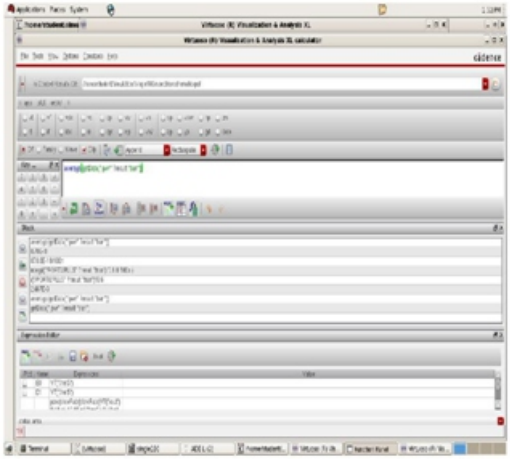

Figure 15) power calculation window

viii.After clicking on the pwrlable. Right click on the pwr select calculator and open it. Then a power calculation window will open.

ix.Select the average power in the given options and click calculate then the power consumed by the given circuit that is the low noise amplifier will be given as shown in the power window that is approximately 2.458 mW of power.

V.CONCLUSION :

A LOW-noise amplifier (LNA) is of body biased three stage amplifier is simulated in cadence tool in 0.18um CMOS technology which is typically the first active block in the receive path of the communication transceivers. Since the signal received by the antenna will be a weak signal, for further signal processing, it has to be amplified. To maintain the signal integrity, the amount of noise that is introduced by the amplifier should be as low as possible. Thus, two main characteristics of any LNA are its gain and its noise performance. Other important design parameters are noise figure, frequency of operation, gain and in some systems linearity. Here the noise figure, gain have been improved. The input voltage has been amplified stage by stage. Three stage low nose amplifier has been simulated in cadence design system stage by stage and the design parameters like noise figure, gain and power consumed have been calculated using cadence.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

REFERENCES:

1)HoomanRashtianand ShahriarMirabbasi, "applications of body biasing in multistage CMOS low noise amplifiers"IEEE transactions on circuits and systemsregular papers, vol. 61, no. 6, page 1638–1647 June2014.

2)SamikshaPatre, NileshBodane and Vinay Keswani "Design of 0.13um CMOS Two Stage Low Noise Amplifier" International Journal of ComputerApplications page 0975 – 8887 Volume 100 – No.15,
August 2014.

3)Akira Hokazono, Member, IEEE, SriramBalasubramanian, "MOSFET Design for Forward Body Biasing Scheme"IEEE electron deviceletters, vol. 27, no. 5, May 2006.

4)MabroukiAya, Taris Thierry, Deval Yann, Begueret Jean-Baptiste. "A variable gain 2.4-GHz CMOS Low Noise Amplifier employing body biasing"IEEETransactionspage168–171July, 2009

5)Ayamabrouki, Thierry taris, Yann deval, and Jean-baptistebegueret, IMS Laboratory "CMOS Low-Noise AmplifierLinearizationthroughBodyBiasing"IEEEInternational Symposium on Radio-Frequency Integration Technology page150 - 153 December,2009.

6)FatemehGhadimipoor, Hossein GharaeeGarakani"A Noise-Canceling CMOS Low-Noise Amplifier forWiMAX"International Conference on ElectronicDevices, Systems and Applications (ICEDSA) May,2011.

7)Salendra, Govindarajulu(IJCSE) "High Performance VLSI Design Using Body Biasing in Domino Logic Circuits"International Journal on Computer Scienceand Engineering Vol. 02, No. 1741-1745 may 2010.

8)Shashikant Sharma, Anjan Kumar, Manisha Pattanaik, and Balwinder Raj "Forward Body Biased Multimode Multi-Threshold CMOSTechnique for Ground Bounce Noise Reduction in Static CMOS Adders"International Journal of Information andElectronics Engineering, Vol. 3, No. 6, 567-52 ISSN:2010-3719 November 2013.

9)S. S. Gore, G. M. Phade"Design Challenges and Performance Parameters of Low Noise Amplifier"International Journal of Innovations inEngineering and Technology (IJIET) ISSN: 2319–1058 Vol. 3 Issue 1 October 2013.

10)H.Rashtian, C. Majek,S. Mirabbasi, T.Taris, Y.Deval, and J.Begueret, "On the use of body biasing to control gain, linearity, and noise figure of a mm-wave CMOS LNA " IEEE Int. New Circuits and syst. Conf.(NEWCAS),page 333–336Jun.2010.

11)Trung-Kien Nguyen, Chung-Hwan Kim, Gook-JuIhm, Moon-Su Yang, and Sang-Gug Lee "CMOS Low-Noise Amplifier Design Optimization Techniques"IEEE transactions on microwave theoryand techniques, Vol. 52, no. 5, May 2004.

12)Abhishek kumar, Lovely Professional University, Phagwara, Punjab, India "Efect of Body Biasing Over CMOS Inverter" ISSN: 2230-7109 IJECT Vol. 4, IssuE 1, March 2013.

Author's Profile:

B. Jyothsna received the B.Tech degree in electrical and electronics engineering from G.Narayanamma Institute Of Technology And Science For Women, India, in 2012.she is currently working towards the M.Tech degree in electronics & communication engineering, with specialization in DSCE from the Sreenidhi Institute Of Science And Technology, India.

N.S.Murthy Sarma belongs to K. Pedapudi, East Godavary district of Andhra Pradesh state, India. He received his Model Diploma for Technicians (MDT), offered with collaboration of United Sates of Soviet Russia (USSR), with specialization in production of radio apparatus (RA) from Government Polytechnic of Masabtank, Hyderabad, his B.Tech from Jawaharlal Nehru Technological University (JNTU) College of Engineering, Hyderabad in 1990, his M.E with specialization in Microwaves and Radar Engineering (MRE) from Osmania University in 1996 and his Ph.D. in E.C.E from O.U, Hyderabad in 2002. As a Part of his diploma curriculum, He was at nuclear instruments division of instruments group in Electronics corporation of India limited (ECIL), Hyderabad as technician apprentice in 1984. From 1991 to 1996 he was a lecturer to U.G courses in electronics, physics in faculty of science and various subjects of electronics and communications engineering for diploma holders (FDH) program of JNTU Engineering College at Hyderabad, and from 1996 to 2001 he was with R&T Unit for navigational electronics (NERTU). During his association with NERTU, he executed projects sponsored by RCI, VSSC, DLRL and DST.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

His research interests include electromagnetic modeling, atmospheric studies, optical fiber communication, low power VLSI, signal processing. Several international and national publications are under his credit. He continued his teaching from 2001 and currently at Sreenidhi Institute of Science and Technology as a professor of ECE. He teaching interests for undergraduate courses includes Electromagnetic theory, antennas and propagation and microwave engineering, post graduate courses in communication systems and microwave radar engineering. Dr. N.S.Murthy sarma is life member of Institute of Science and Technology education (ISTE) since 2002 and fellow of institute of electronics and telecommunication engineers (IETE) since 2003, fellow of Institution of Engineers IE(I) and Member of Institute of Electrical and Electronics Engineers (IEEE) since 2010. He usually reviewers papers for international journals viz. international journal of computer science and Engineering systems and international journal of International Journal of Emerging Technologies and Applications in Engineering Technology and Sciences , besides a regular conference reviewer of conferences(since 2010) of IEEE with immediate recent assignment of ADVCIT15 and ISHAMS15 . He is one of the recognized Ph.D. Supervisors of engineering faculty, Around Eight research scholars are working with him under Ph.D. programme of JNTUH/JNTUK in the area of Communications, Low power VLSI, GPS/GLONASS, since 2008. Two of his scholars were awarded Ph.D. in 2012 and 2015 respectively.