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A Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-Standard Digital Up Counter

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Abstract:

This brief proposes a two-step optimization technique for designing a reconfigurable VLSI architecture of an interpolation filter for multi standard digital up converter (DUC) to reduce the power and area consumption. The proposed technique initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multi standard DUC for three different standards. In the next step, a 2-bit binary common sub expression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multi standard DUC. Most of the area occupied in the design of FIR filter is the multiplier. The low power and area architecture f pulse shaping FIR filter for digital up converter was designed. In the existing system, the two bit binary common sub-expression based binary common sub-expression elimination algorithm and shift and add method was used to generate the partial products. In this paper, carry save adder is used instead of shift and add method and also the simple arithmetic adders of multiplexer unit is replaced by carry save adder. The number of additions and multiplications are reduced using this technique. The designed pulse shaping FIR filter is synthesized and simulated using Xilinx ISE 14.3.

Index Terms:

Digital up converter (DUC), finite-impulse response (FIR) interpolation filter, reconfigurable hardware architecture, software defined radio (SDR) system.

1.INTRODUCTION:

Requirement of various high data transfer rates and high channel capacities by different operating modes of the present day cell phones motivated the telecommunication industry to spawn the concept of software defined radio (SDR). According to [1] and [2], SDR refers to a single device that is capable of supporting all the present as well as emerging standards available under the wireless communication category. In an SDR system, multiple standards can be realized in a single chip [3] by providing a programmable channel select filter at the baseband level. Different standards have different channel bandwidths, sampling rates, carrier-to-noise ratios, blocking, and interference profiles. This makes the development of a reconfigurable sample rate converter chip to be a major challenge faced by the telecommunication industry of today. Several researchers have contributed toward designing a low-power, low-area, and low-complexity reconfigurable channel filter for data rate conversion in SDR system. Lin et al. [4] have proposed a combination of symmetrical retimed direct form architecture, balanced modular architecture, separated signed processing architecture, and modified canonical signed digit (CSD) technique-based finite-impulse response (FIR) filter to improve the power consumption. However, the reduction in power has been achieved by compromising with the speed of operation

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that makes this design unsuitable for the SDR system. A multiplier-less FIR interpolator with smaller area usage has been proposed in [5]. Efficient use of lookup tables (LUTs) in this design helps to reduce the power and area while compared with the conventional FIR filter implementation. In case of higher order filter implementation; this architecture fails to achieve low power because of an increase in the ROM size. Meher et al. [6] presented an area-delay-power efficient FIR filter by systolic decomposition of distributed arithmetic (DA)-based inner-product computation. The implementation results listed in this brief show that reduction in memory size leads to increase in the latency and area. Based on modified DA technique, high-speed and medium-speed FIR filter architectures have been proposed in [7]. The high-speed FIR filter architecture where the LUTs are working in parallel draws a very high current and involves huge area consumption.Chen and Chieueh [8] proposed one novel digit serial reconfigurable FIR filter where CSD-based technique serves as a better solution to design the digital filter rather than multiply and accumulate-based approach. In common sub-expression elimination (CSE) technique, multiplication operations between the constant coefficients and inputs are performed by shift and add operations.

The number of addition operations used to perform the multiplication operation defines the logic depth (LD) or the critical path of the circuit. Gustafsson [9] described lower bound issues related to the problems in constant multiplication (CM). CSE algorithm is a useful solution in achieving less hardware footprint for implementing higher order digital filters, as mentioned in [10] and [11]. A low complexity architecture based on binary CSE (BCSE) algorithm has been proposed in [12] and [13]. This algorithm consumes less hardware and power than those of CSD-CSE method using a common constant/programmable shift-and-add block. However, constant shift multiplication-based FIR filter design proposed in [13] involves use of redundant adder in the multiplier block. This additional hardware usage consumes more area and power, and makes the design unsuitable for SDR system where low power and low area consumptions are the key concerns. From a study of the abovementioned literature, it is evident that the need for developing a low complexity multiplier in the context of reconfigurable interpolation filter is yet to be addressed by which more area and power can be reduced toward designing a multistandard digital up converter (DUC) for SDR system. To overcome the disadvantages of the existing reconfigurable architectures for FIR filter mentioned above, a new reconfigurable architecture has been proposed in this brief for initial reduction of multiplications per input sample (MPIS) and additions per input sample (APIS) and subsequent reduction of hardware and power by designing an efficient constant multiplier using 2-bit binary common subexpression (BCS).Software Defined Radio (SDR) technology is significantly used in wireless communication and it refers to the class of reconfigurable radios in which the physical layer behavior can be flexible through reconfiguration. In the SDR system, FIR filters are mostly used in Digital Up Converter and Digital Down Converter. Digital Up Converter (DUC) is widely used in communication systems for converting the signal sample rate. It is needed when the signal is transmitted from baseband signal to Intermediate band. The input signal which is given to the DUC is filtered and transformed into higher sampling rate and then the signal is modulated with carrier signal. The various sections of Digital Up Converter (DUC) have been optimized individually and then compound in concert. The digital signal processing application using variable sampling rates can improve the flexibility of a software defined radio. It reduces the need for expensive anti-aliasing analog filters and enables processing of different types of signals with different sampling rates. It allows partitioning of the high-speed processing into parallel multiple lower speed processing tasks which can lead to a significant saving in computational power and cost.

Finite Impulse Response (FIR) filters play a vital role in many signal processing applications in communication systems. Many task such as spectral shaping, matched filtering, interference cancellation, channel equalization, etc. can be performed with the use of FIR filters. A single device that supports all the standards under wireless communication is referred to as Software Defined Radio (SDR) [1]. Finite impulse response (FIR) filters are employed as channel filters in SDR receivers. The basic idea behind the SDR is to replace most of the analog signal processing in the transceiver side with digital signal processing in order to provide the advantage of flexibility through reconfiguration. This helps different air- interfaces to be implemented on a single hardware platform to support multi standard wireless communication. The reconfigurability of the receiver to work with different wireless communication standard is another key requirement in a SDR [2]. In order to reduce the complexity of the design we use the interpolation FIR filter [3]. Several designs have been proposed to design a low power consumption and low area and low complexity design reconfigurable FIR filter for SDR system.

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A modified canonical signed digit (CSD) [4] is proposed to design to improve power consumption but this have been obtained by the reduction of operating speed and this technique is unsuitable for SDR system. Low power and low area FIR filter has been achieved by using the efficient Look Up Table (LUT) but however this design is not applicable for higher order filter because it increases the size of ROM. A Distributed Arithmetic (DA) [5] has been proposed to design an area-delay-power efficient filter. Logic depth is defined as number of addition operation required to perform multiplication, it is also known as critical path. An algorithm based on binary common subexpression [6] elimination as been proposed this proposed design consumes less power and area but this involves the addition adder block which makes the design unfit for SDR system.The digital industry is dynamically growing and the development of digitally based products is rising. Various industries such as audio, video, and cellular industry depend heavily on digital technology. A great part of this deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology and its applications to keep businesses and industries connected. The world of digital technology is certainly one that will play vital role for many years to come. Digital Signal Processors (DSPs) are specialized devices designed to implement digital signal processing algorithms on stream of digitized signals. DSPs are widely used in wireless systems to perform various filtering, encoding, decoding and transform functions.

The highly competitive nature of the wireless communications market and constantly evolving communication standards have resulted in short design cycles and product lifetimes. This environment has led to the emergence of a new class of configurable DSPs, which can leverage hardware flexibility, programmability, and reusability, to provide highly customizable DSP solutions [1].DSPs can broadly be divided into two classes: ASIC and Programmable DSP. ASICs implement complex algorithms in hardware and are used in applications that demand high computational performance. Programmable DSPs on the other hand are used to implement low to medium-complexity algorithms in software, and are mainly used in applications that require good performance at low system costs. For this reason, programmable DSPs are widely used in wireless handsets to perform various baseband processing functions such as filtering, equalization, and echo cancellation [2].

As communication standard evolve and time-to-market pressures yield shorter design cycles, programmable DSPs become more appealing than ASICs due to the ease with which their functions can be modified. However when hardware acceleration is the only approach for satisfying the computational demands of an applications, ASICs maintain their advantage. For high end digital signal processing where the highest possible performance is needed at low power consumption, ASICs are still the processors of choice.However, ASICs require very long design and development times and are very expensive to design and manufacture. Moreover, ASICs are inherently rigid and are not very well suited to applications that are constantly evolving. For these reasons, Programmable Logic Device like Field Programmable Gate Arrays (FPGAs) has emerged as an alternative to ASICs in wireless communication systems.FPGAs are mainly used for the flexibility they provide. Like programmable DSPs, FPGAs are programmed and configured in software. This makes it very easy to upgrade or add functionality to an FPGA, even if it is already deployed in the field. Like ASICs, FPGAs achieve high levels of performance by implementing complex algorithms in hardware. FPGAs are particularly well suite for accelerating algorithms that exhibit a high degree of data flow parallelism. The FPGAs suffer from the drawbacks of inefficient resource utilization, high cost and power consumption [3].

Existing Method:

Requirement of various high data transfer rates and high channel capacities by different operating modes of the present day cell phones motivated the telecommunication industry to spawn the concept of software defined radio (SDR). SDR refers to a single device that is capable of supporting all the present as well as emerging standards available under the wireless communication category. In an SDR system, multiple standards can be realized in a single chip by providing a programmable channel select filter at the baseband level. Different standards have different channel bandwidths, sampling rates, carrier-to-noise ratios, blocking, and interference profiles. This makes the development of a reconfigurable sample rate converter chip to be a major challenge faced by the telecommunication industry of today. a combination of symmetrical retimed direct form architecture, balanced modular architecture, separated signed processing architecture, and modified canonical signed digit (CSD) technique-based finite-impulse response (FIR) filter to improve the power consumption.

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However, the reduction in power has been achieved by compromising with the speed of operation that makes this design unsuitable for the SDR system. A multiplier-less FIR interpolator with smaller area usage has been proposed in [5]. Efficient use of lookup tables (LUTs) in this design helps to reduce the power and area while compared with the conventional FIR filter implementation. In case of higher order filter implementation, this architecture fails to achieve low power because of an increase in the ROM size.

Proposed Method:

To overcome the disadvantages of the existing reconfigurable architectures for FIR filter mentioned above, a new reconfigurable architecture has been proposed in this brief for initial reduction of multiplications per input sample (MPIS) and additions per input sample (APIS) and subsequent reduction of hardware and power by designing an efficient constant multiplier using 2-bit binary The organization of this brief is as follows. The problem regarding the realization of a reconfigurable FIR interpolation filter in hardware and the proposed method for its solution have been explained and describe the architectural details of the proposed reconfigurable FIR filter architecture for multi standard DUC. Implementation results and discussion common sub expression (BCS).

2.ISSUES IN DESIGNING THE CONFIGURABLE ROOT-RAISEDCOSINE FIR FILTER AND ITS PROPOSED METHOD FOR SOLUTION:

2.1 Issues in Designing the Reconfigurable RRC:

FIR Filter Multistandard DUC As a design example of multistandard DUC, we have considered three standards, namely universal mobile telecommunication system.

TABLE 1 MATLAB ANALYSIS REPORT:

$\alpha = 0.22$	WCDMA	UMTS			DVB		
Interp. Fact.	4	4	8	16	6	4	3
Sym. Rate (MSPS)	1.25	3.84			27.5	42.25	55
Samp. Freq. (MHz)	5	15.36	30.72	61.44	165	165	165
Taps	25	25	49	97	37	25	19

wideband code division multiple access, and digital video broadcasting.

These three standards have adopted root-raised-cosine (RRC) filter as the pulse shaping filter for its ability to decrease the bit error rate by disallowing timing jitter at the sampling instant. The specifications of these standards presented in Table I are used to calculate the required filter lengths and the interpolation factors. The MATLAB analysis report for each filter. Table I. Efficient hardware implementation of a reconfigurable RRC FIR interpolation filter with the specification mentioned in Table I throw up the following challenges.

1) For a filter of N tap with interpolation factor of R, _N/R_ equivalent multipliers (to implement the convolution operation between the inputs and the filter coefficients), and structural adders (to perform the final addition operation for generating the output) are required. Implementation of three different filter lengths of L, M, and N with three different interpolation factor P, Q, R would require _L/P_+ _M/Q_ +_N/R_ number of equivalent multipliers and structural adders. Now, if the filter parameters (rolloff factors for RRC filter) are different, the total number of multipliers and structural adders will linearly increase with the number of parameters considered for designing the filter. For a constant propagation delay, the problem of area and power consumptions increases as the number of multipliers and structural adders increases for implementing the variable length higher order filter in a single architecture.

2) Amongst several techniques proposed earlier, the BCSE method is the recently proposed popular method for implementing an efficient constant multiplier. In BCSE algorithm, a coefficient of m-bit word length can form 2m − (m + 1) BCS amongst themselves. Proper choice of the length of the BCS is an important factor to avoid the inefficient utilization of hardware.

3) In BCSE technique, LD is the critical path that mainly depends on the number of addition operations in a chain. Propagation delay of the filter is measured by the computation time of (LD + 1) addition operations. Proper use of BCS to decrease the LD that maximizes the operating frequency of the filter is a challenge.

4) CMs are performed through shift and add operations. For example, if X is the number of adders required for a single CM operation, implementation of L-, M-, and N-tap filters wil; require {[L/2+M/2+N/2] X} number of adders.

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By reducing the number of adders by Y say, for a single CM, one can save {[L/2+ M/2 + N/2] Y} number of adders to implement the desired reconfigurable FIR interpolation filter task of FIR Methods.

2.2 Proposed Method for Solution the technique proposed in this brief to solve the problem addressed above consists of the following steps.

1) In the first coding pass (FCP) block, the coefficient sets of the two RRC filters of the same length differing only by the filter parameters are multiplexed through one 2:1 multiplexer, where one control parameter (FLT_SEL) selects the desired filter depending on the roll-off factor. This multiplexing technique helps in decreasing the requirement of the multiplier by 50%as the total number of coefficients is 111 instead of the Initial requirement of 222.

2) In the second coding pass (SCP), the coefficients obtained from the FCP block are passed through another set of multiplexers, where one control parameter (INTP_ SEL) selects the desired filter depending on the interpolation factor.This technique reduces the total number of filter coefficients that will be processed further from the earlier requirement of 111–49 after the FCP.Combination of FCP and SCP steps reduces the requirement of MPIS from 42 to 7 and APIS from 36 to 6, which facilitates 83.3% improvement for this design. According to the proposed method, considering more filters of different specifications will cause more reduction in the APIS and MPIS.

3) Instead of 3-bit BCSE presented, we have proposed2-bit BCS-based BCSE technique, where the LD can be defined as

$$LD_{2BCS} = \lceil \log_2 2 \rceil + \log_2 \left\lceil \frac{16}{2} \right\rceil = 4 \qquad (1)$$

where the term log2 2 is due to the 2- bit BCS and the term log2_16/2_ is due to the fact that the world-length for the coefficients has been considered to be 16 bits. Hence, for the 2-bit BCSbased FIR filter, its propagation delay can be defined as

$$T_{2BCS} = 4 \times t_{add} + t_{4:1mux} + t_{acc} \qquad (2)$$

where tadd is the delay of each adder used in the constant multiplier, t4:1mux is the delay for the 4:1 multiplexer, and tacc is the delay for the final adder in the delay chain of FIR filter.

From (1) and (2), it can be clearly seen that use of 2-bit BCS leads to a good amount of saving in the propagation delay compared with the 3-bit BCS-based constant multiplier design [13]. They made all structure to that some function that they mean to produce the made some level and produced.

4) In any FIR filter, the multiplication operation between the inputs and the coefficients, for which the word length of the coefficient is 16 bits can be written as

$$y1 = x1 + 2^{-1}x1 + 2^{-2}x1 + 2^{-3}x1 + \cdots + 2^{-14}x1 + 2^{-15}x1. \qquad (3)$$

Considering 2-bit BCS in the proposed architecture i.e., x2 = x1 + 2−1x1 (3) can be rewritten as

$$y1 = x2 + 2^{-2}x2 + 2^{-4}x2 + \cdots + 2^{-10}x2 + 2^{-12}x2 + 2^{-14}x2. \qquad (4)$$

In the proposed architecture, the shift add unit has been grouped in eight pre-shifted values of 2N + 1 bit, where N = 8, 7, 6, 5, 4, 3, 2, 1 to implement (4). This will help in reducing the multiplexer and the adder width. As this shifting is done prior to the addition operation, the maximum error (due to truncation) has been pre-calculated and added in the final addition operation of the constant multiplier block. This technique helps in reducing the hardware, as explained in the previous section.

3.PROPOSED RECONFIGURABLE ARCHITECTURE:

The proposed block diagram for the reconfigurable architecture of FIR interpolation filter based on the method proposed above is shown in Fig. 1. In this architecture, two parameters INTP_SEL and FLT_SEL are used to select different interpolation factors and roll-off

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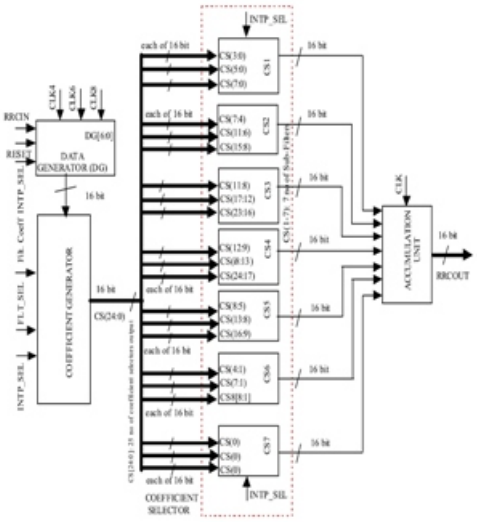

Fig. 1. Proposed architecture of the reconfigurable RRC filter.

factors, respectively. The master clock (CLK) that is used to sample the output (RRCOUT), operates at a higher rate than the other three clock sources CLK divided by four (CLK4), by six (CLK6) and by eight (CLK8), respectively, which have been used for sampling the serial input data (RRCIN) for different interpolation factors.The proposed reconfigurable RRC filter architecture consists of the major modules, viz data generator (DG), a coefficient generator (CG), a coefficient selector (CS), and an accumulation unit block (FA).

DG Block:

DG block (Fig. 1) is used to sample the input data (RRCIN) depending on the selected value of the interpolation factor selection parameter (INTP_SEL). From the design point of view, it has been observed that 25-, 37-, and 49-tap filters with interpolation factors of four, six, and eight constitute a branch filter of seven taps; _25/4_ = _37/6_ = _49/8_ = 7. This indicates that to generate the full filter response, seven subfilters are required for multiplication of the filter coefficients with the input sequence.

B. CG Block:

The CG block performs the multiplication between the inputs and the filter coefficients. The two-phase optimization technique is proposed, which helps in reducing the hardware usage by a considerable amount to facilitate reconfigurable FIR filter implementation with low computation time and low complexity. The data flow diagram of the CG block for programmable coefficient sets is shown in Fig. 2.

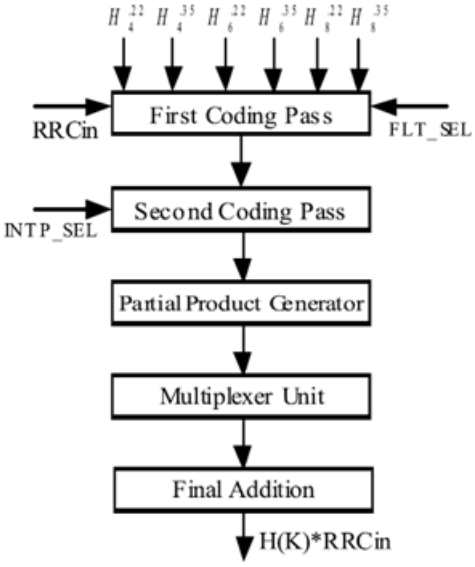

Fig. 2. Data flow diagram of proposed CG block.

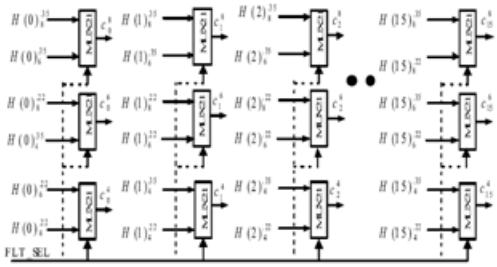

Fig. 3. Architecture for implementation of FCP block.

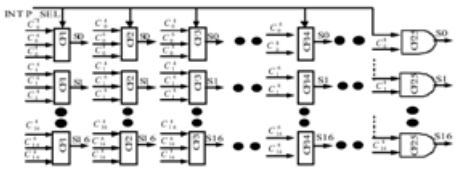

Fig. 4. Architecture for implementation of SCP block.

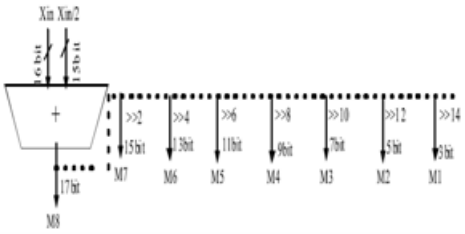

Fig. 5. Architecture for implementation of PPG block.

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The steps mentioned in the previous section have been adopted to enable low area consumption and low complexity.
Functionality of each block shown in Fig. 2 is described as follows.

1) FCP:
In one FCP block, two sets of 25-, 27-, and 49-tap filter coefficients differing only by roll-off-factor are the inputs. Inside the FCP block, three coding pass (CP) blocks are running in parallel for three different interpolation factors. Occurrence of matching between all bits is explored vertically between two coefficients (written as C) of same length filter. Coding has been done according to the procedure mentioned in Section II. The architecture of the FCP block is shown in Fig. 3.

2) SCP:
The outputs from FCP block are three sets of coded coefficients that are 13, 19, and 25 in number and pass through another CP block to get the final coefficient set. In the SCP, the common terms present vertically in between these three coded coefficient sets (written as S) have been found out and coded accordingly. The architecture of the SCP block is shown in Fig. 4.

3) Partial Product Generator (PPG) Unit:
Shift-and-add method is used to generate the partial product during the multiplication operation between the input data (Xin) and the filter coefficients. In BCSE technique, realizations of the common subexpression using shift-and-add method eliminates the common term present in a coefficient. In the proposed architecture, 2-bit BCSs ranging from 00 to 11 have been considered. Within four of these BCSs, an adder is required only for the pattern 11. This facilitates reduction in hardware and improvement in speed while performing the multiplication operation. The shift-andadd block used in this brief is shown in Fig. 5.

4) Multiplexer Unit:
Depending on the coded coefficients, the multiplexer unit will select the appropriate data generated from the PPG unit. The BCS of length 2 bits would require eight 4:1 multiplexer units to produce the partial product that will be added to perform the multiplication operation considering the coefficient word length of 16 bits each. The detailed architecture of the multiplexer unit used in the CG block is shown in Fig. 6.

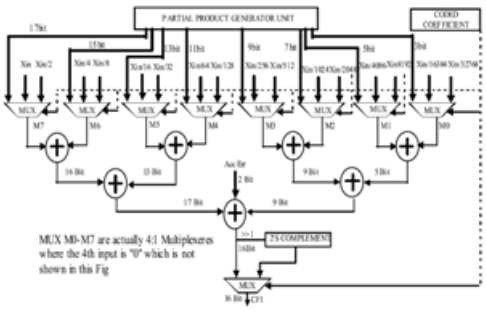

Fig. 6. Block diagram of multiplexer and final addition unit.

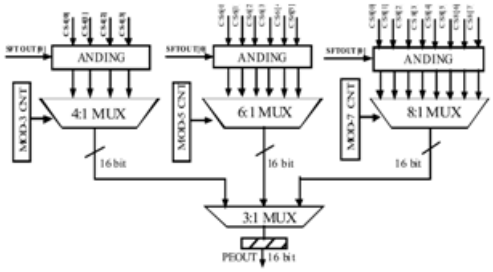

Fig. 7. Hardware architecture of CS block.

5) Addition Unit:
Addition unit performs the task of summing all the outputs of the PPG block followed by eight multiplexer units. The architecture for the final addition is shown in Fig. 6. Different word length adders are required for different binary weights. The outputs from the eight multiplexers viz M7–M0 are added together. The output of the final adder passes through a two's complementer circuit. The final output from this addition unit depends on the sign magnitude bit of the
coded coefficient set.

C. Coefficient Selector:
In the proposed reconfigurable FIR filter, the CS block is used to steer proper data to the final accumulation block depending on the corresponding interpolation factor parameter. It takes the input from the CG block. Hardware architecture of CS block is shown in Fig. 7.

D. Final Data Accumulation Unit (FA):
The proposed reconfigurable FIR filter is based on transposed direct form architecture. The final accumulation block has a chain of six adders and six registers as there are seven sub-filters.

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4.SOFTWARE DEFINED RADIOS

What is Software Defined Radio?

With the exponential growth in the ways and means by which people need to communicate -data communications, voice communications, video communications, broadcast messaging, command and control communications, emergency response communications, etc. – modifying radio devices easily and cost-effectively has become business critical. Software defined radio (SDR) technology brings the flexibility, cost efficiency and power to drive communications forward, with wide-reaching benefits realized by service providers and product developers through to end users.

Software Defined Radio - Defined:

A number of definitions can be found to describe Software Defined Radio, also known as Software Radio or SDR. The SDR Forum, working in collaboration with the Institute of Electrical and Electronic Engineers (IEEE) P1900.1 group, has worked to establish a definition of SDR that provides consistency and a clear overview of the technology and its associated benefits.

Simply put Software Defined Radio is defined as1:

"Radio in which some or all of the physical layer functions are software defined"A radio is any kind of device that wirelessly transmits or receives signals in the radio frequency (RF) part of the electromagnetic spectrum to facilitate the transfer of information. In today's world, radios exist in a multitude of items such as cell phones, computers, car door openers, vehicles, and televisions.Software defined radios are beginning to find also commercial potential. When the software defined radio becomes main stream, the full potential of adaptability may create possibilities for new kind of services. From the users' point of view, seamless operation across networks, without caring about the underlying technology, would be a very desirable feature. The Second Generation (2G) and Third Generation (3G) systems differ mainly in the channel access technique. The 2G or GSM is basically a TDMA oriented system and 3G is strongly based on CDMA. According to an increasing demand for simultaneous global roaming and allin- one wireless phones, the interest in the development of the so-called multi-standard radio transceivers was fostered.

One leading solution is the dynamic reconfiguration of the different modules in the system to suit the specifications of as many standards as possible so, the system should be capable of dynamically reconfiguring itself to the environment as needed [4].In this scenario the availability of reconfigurable platforms both for the base stations and mobile terminals will be of great concern. This will enable the possibility to reconfigure the receiver while the user is moving, leading to ubiquitous access to services. Software defined radio (SDR) is a rapidly evolving technology that is receiving enormous recognition and generating widespread interest in the telecommunication industry. Software Defined Radio involves software implementation of user terminal functions to enable the terminal to dynamically adapt to the radio environment in which it is located. SDR also enables wireless operators to introduce new services independent of the wireless standard used. It also enables subscribers to benefit from new or customized services and truly global connectivity. The development of system on-chip (SoC) design has led to integration of analog RF, analog baseband and digital signal processors on the same chip. This has resulted in low power devices with multi-purpose functionality [5].The second generation of DVB specs, DVB-S2, was developed for satisfying the today's needs for reliable and effective broadband satellite communication services even under 'hostile' conditions. This is achieved by exploiting the new advances in the fields of coding and modulation.

Software defined radio proves to be an enabling technology for future multimode and reconfigurable satellite receivers [6]. To make the transition from one standard to another as smoother as possible, the common and effective domain for the implementation of new system architectures is the Software Defined Radio paradigm. SDR platforms rely heavily on reconfigurable logic to realize complex architectures and evolving standards. Although cost is a major motivating factor in pursuing this technology, the flexibility of accommodating multiple standards under a single hardware "umbrella" is of particular importance to emergency responders (ER) who are often forced to function in environments where wireless coverage is limited or altogether non-existent. In such an environment, ER personnel must have access to radios which can operate not only as common wireless communication devices, but also as push-to-talk P25- compatible radios [7].A successful implementation of SDR depends on the feasibility of implementing various blocks within the communication chain for multiple standards.

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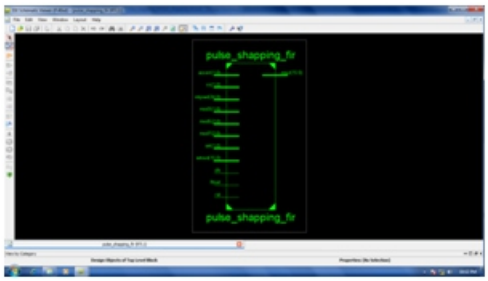
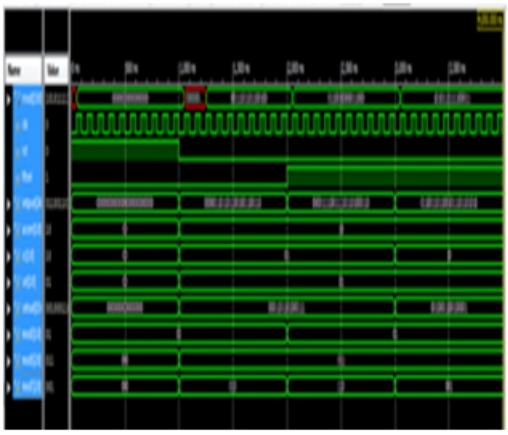
Wireless is a continuously changing environment, wherein the innovation rate is very high. It requires as much flexibility as possible by exploiting software solutions. In fact, observing the past years, software platforms have proved superior scalability capabilities with respect to completely hardware solutions.However, the rates involved in mobile wireless communications and the bandwidth requirements cannot be faced yet only resorting to software. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms.Such a solution allows inexpensive, efficient interoperability between the available standards and frequency ands [8]. The hardware reconfiguration feature of a software defined radio (SDR) architecture can support multiple modes of a digital beam former (DBF) striving for compactness and efficient processing power, which are important issues for microsatellite synthetic aperture radar (SAR) systems [9].

RESULTS & DICUSSIONS:





CONCLUSION:

In this paper, reconfigurable pulse shaping FIR filter was designed for multi-standard digital up converter for Software Defined Radio system. The complexity of area is caused by the multipliers.

The modification to the architecture is included by which carry save adder was used to reduce the power and area consumption. So that the speed of the operation gets increased and also area of the architecture gets minimized. While using this technique, the additions and multiplications were reduced for generating the partial products.

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