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An Efficient Carry Select Adder with Optimized Area and Delay by Using AOI Logic

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Abstract:

In most of the data processing processors to perform arithmetic functions Carry Select Adder (CSLA) is used as this is one of the fastest adders. In order to increase the overall efficiency of the processor we can reduce the area and power consumption of the CSLA of processors. Based on this premise we can modify the regular SQRT CSLA architecture as 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

Index Terms: Adder, arithmetic unit, Carry select Adder, AOI Logic& low-power design.

I. INTRODUCTION:

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin = 1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the –bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III. This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparisons with the proposed de-sign as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively. Finally, the work is concluded in Section VI.

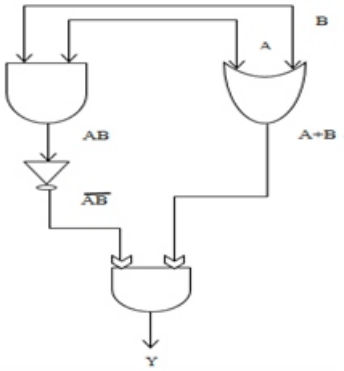

Figure 1: Area evaluation of Exclusive ORgate

II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS:

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate.

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The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Tab l

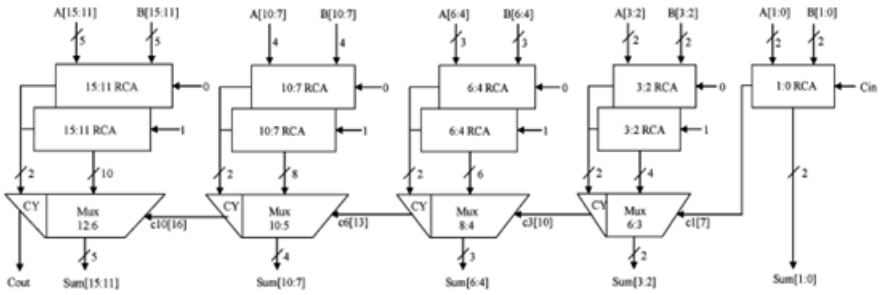

Figure 2: Regular 16-b QRT CSLA

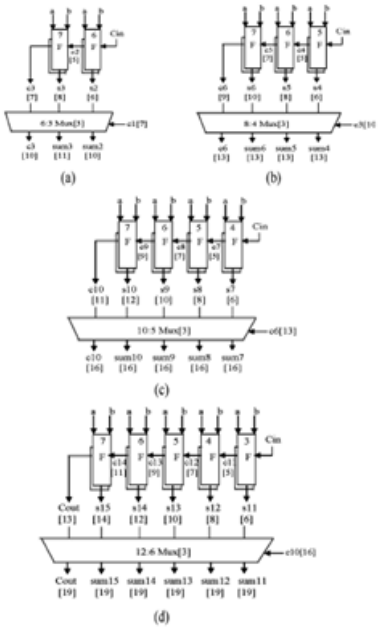

Figure 3: Delay and area evaluation of regular SQRT CSLA (a) group 2 (b) group 3 (c) group 4 and (d) group 5. F is full adder.

III. EXCLUSIVE OR OF MODIFIED AREA EFFICIENT CSLA :

The main idea of MA-CSLA is to use 4 gate XOR which reduces the total gate count. From the Figure 2 it is clear that there is the possibility of reduction of gates by using the XOR gates which has been proposed in our design. In the Modified CSLA the total number of XOR gates is 210.In Modified Area Efficient CSLA (MA-CSLA) the total number of XOR gates is 168.In the Modified Area Efficient CSLA (MA-CSLA) the following expression would

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

Table 1: Delay and Area count of the basic blocks of CSLA.

be used for an XOR operation. Y=(a+b)(~ab)

IV. OPTIMIZED BEC:

The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC[2].When the optimized XOR gate is used in Modified CSLA ,it is verified that there is large reduction in number of gates. The MUX is used to select either the BEC output or the inputs given directly to a BEC circuit[2].In this design, the major function of MUX is to derive the adder speed.

V.DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA:

The structure of the 16-b regular SQRT CSLA is shown in Fig2. It has five groups of different size RCA. The delay and area evaluation of each group are shown in table 2, in which the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

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1) The group2 [see Fig.3(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input C1[time(t) = 7] of 6:3 mux is earlier than S3[t = 8] and later than S2 [t=2]. Thus, Sum3[t= 11] is summation of S3 and mux[t=3] and Sum2[t = 10] is summation of C1and Mux.

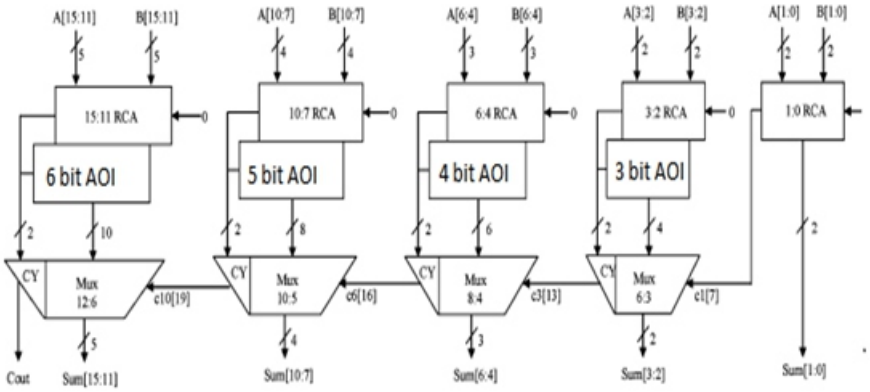
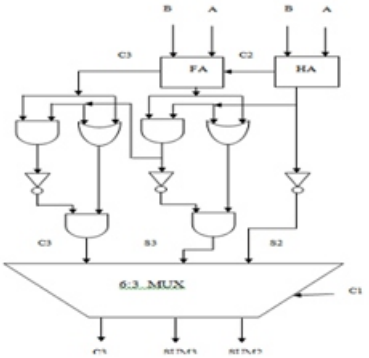
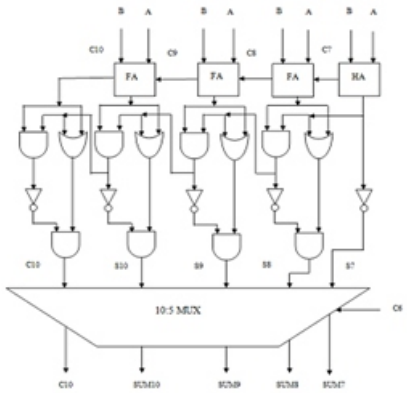


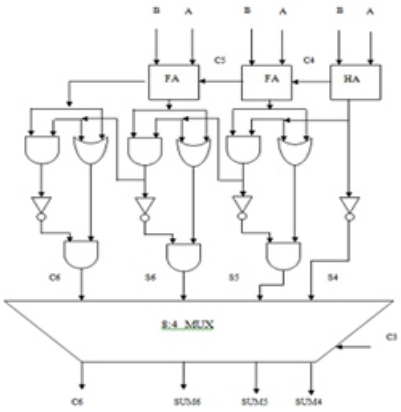
Figure 4: Modified Area efficient carry select adder (MA-CSLA)



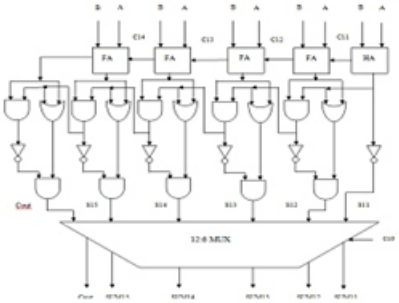
(a)



(c)



(b)



(d)

Figure 5: Delay and area evaluation of modified SQRT CSLA (a) group 2 (b) group 3 (c) group 4 (d) group 5. H is half adder.

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2) Except for group2, the arrival time of mux selection input is al-ways greater than the arrival time of data outputs from the RCA's.Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\{c6, \text{sum}[6:4]\} = c3[t = 10] + \text{mux}$$
$$\{c10, \text{sum}[10:7]\} = c6[t = 13] + \text{mux}$$
$$\{\text{cout}, \text{sum}[15:11]\} = c10[t = 16] + \text{mux}.$$

3) The one set of 2-b RCA in group2 has 2 FA for Cin = 1and the other set has 1 FA and 1 HA for Cin = 0. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57\,(\text{FA} + \text{HA} + \text{Mux})$$
$$\text{FA} = 39(3 * 13)$$
$$\text{HA} = 6(1 * 6)$$
$$\text{Mux} = 12(3 * 4).$$

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

Table II: Delay and Area count of regular SQRT CSLA Groups

4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table II.

VI.DELAY AND AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA:

The structure of the proposed 16-b SQRT CSLA using AOI for RCA with Cin=1to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 5. The steps leading to the evaluation are given here

1) The group2 [see Fig. 3(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin = 0. Instead of another 2-b RCA with Cin = 1 a 3-b AOI is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input C1 [time(t) = 7] of 6:3 mux is earlier than the S3 [t=9] and C3 [t=10] and later than the S2 [t=4].

Thus, the sum3 and final C3 (output from mux) are depending on S3 and mux and partial C3 (input to mux) and mux, respectively. The sum2 depends on C1 and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the AOI. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

Group	Delay	Area
Group2	11	40
Group3	16	57
Group4	23	74
Group5	30	98

Table III: Delay and Area count of modified SQRT CSLA

3) The area count of group2 is determined as follows
Gate Count=40 (FA+HA+Mux+AOI)
FA=13(1*13)
HA=6(1*6)
AND=4
OR=2
NOT=3
Mux=12(3*4)

4) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table III. And similarly group3, group4 and group 5 are evaluated.Comparing Tables II and III, it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, withonly 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

VII.FPGA IMPLEMENTATION RESULTS:

The design proposed in MA-CSLA is successfully tested using (Xilinx) Spartan 3E series target and verilog HDL. The MA-CSLA architecture is simulated using Isim simulator. The result analysis of Modified CSLA (M- CSLA) and Modified Area efficient CSLA(MA-CSLA) is compared below.

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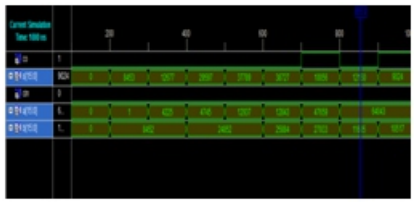

Fig 6: Simulation Result For Regular SQR CSLA

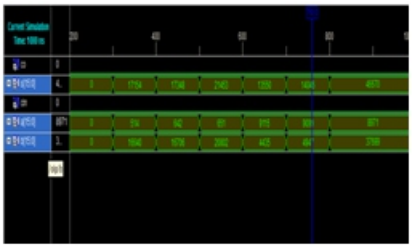

Fig 7: Simulation Result For AOI logic Based SQR CSLA

VIII. CONCLUSIONS:

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power[8]. The compared results show that the modified SQRT CSLA [9] has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere trade off of delay for power and area. The modified CSLA architecture is there-fore, low area, low power, simple and efficient for VLSI hardware implementation. These are most widely used in DSP applications [10]. It would be interesting to test the design of the modified 128-b SQRT CSLA

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