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A PI and Fuzzy Controlled Two-Phase Interleaved PFC Boost Converter

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Abstract
Interleaving control schemes are widely used in converter applications. Merits of such control methods are in reducing input/output current or voltage ripples and volume, and increasing the processed power capacity of converters. For converters with constant frequency operation, it is easy to achieve interleaving control. However, it is difficult to realize interleaving features with variable frequency operation, such as boost-type power factor correctors (PFCs) operated in critical conduction mode (CM) condition. This new interleaving technique makes each phase work at ideally CRM. Natural current sharing and precise 180 ^{0} phase shift are achieved. The scheme can be easily integrated into a PFC control chip. Full-order averaged model of CRM boost is derived to analyze the stability of the converter. In this project, a two-phase PFC boost converter operating with PI and Fuzzy controller at the CRM is described which employs a variation-tolerant phase shifter (VTPS) is proposed and results are presented by using Matlab/simulink software.

Keywords— Critical Conduction Mode (CRM), DC Motor Drive, Interleaved Boost Converter Control, Power Factor Correction (PFC), Variation-Tolerant Phase Shifter (VTPS).

INTRODUCTION

Ac–dc power supplies with transformer isolation are typically implemented with some sort of input power factor correction (PFC) to comply with harmonic standards such as IEC 1000-3-2. There are three techniques to satisfy these standards. One of them is adding passive filter elements to the traditional passive diode rectifier/LC filter input combination; the resulting converter is very bulky and heavy due to the size of the low-frequency inductors and capacitors. Another method is using an ac–dc boost converter in the front-end rectifying stage to perform active PFC for most applications [1]-[3]. The ac–dc boost converter shapes the input line current as an almost sinusoidal shape with a harmonic content compliant with agency standards. Using active PFC, however, increases the cost and complexity of the overall two-stage converter because an additional switching converter must be implemented [4]. This has led to the emergence of single-stage power factor-corrected (SSPFC) converters.

Power factor corrected circuits can be classified as either passive or active PFC among which active PFC is preferred due to its small form factor and higher PF [5]. The operation modes of an active PFC converter can be classified as the continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM) depending on the current flowing through the inductor [6]-[9]. For a heavy load, the CCM is usually employed because it can handle more current than the DCM and CRM. At the CCM, however, the hard switching of the freewheeling diode may result in decreased power conversion efficiency. On the contrary, the freewheeling diode is switched softly at the DCM and CRM and thus higher power efficiency can be expected.

To better understand Power Factor (PF), it is important to know that power has two components:

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•Real Power

•Reactive Power

Real Power is the power that is actually consumed and registered on the electric meter at the consumers' location. It performs the actual work, such as creating heat, light and motion. Real Power is expressed in kW and is registered as kWh on an electric meter. Reactive Power is required to maintain and sustain the Electromagnetic Field (EMF) associated with the industrial inductive loads [10]. Reactive Power is measured in kVAR. The total required power capacity including the real and the reactive components is known as Apparent Power, expressed in kilovolt ampere (kVA).Power Factor is a parameter that gives the amount of real power used by any system in terms of the total apparent power. Power Factor becomes an important measurable quantity because it often results in significant economic savings. When this ratio deviates from one, the input contains phase displacement and harmonic distortion or both and either one degrades the Power Factor. Thus, the power considered as Reactive power in the system is due to two reasons:

• Phase shift of current with respect to voltage, resulting in displacement

• Harmonic content present in current, resulting in distortion

These two factors define Displacement Factor and Distortion Factor, respectively; most power conversion applications use the PFC stage as the first stage in an AC-to-DC converter to improve the displacement and distortion factors so that minimum Apparent Power can be obtained from the supply. To reduce the losses in a power line and a power generator, minimum apparent power is absorbed from the supply, resulting in the improvement of power quality and overall efficiency of the system. The basic function of the PFC stage is to make the input current drawn from the system sinusoidal and in phase with the input voltage [11].

TWO-PHASEINTERLEAVEDCRM PFC BOOST CONVERTERWITH AVTPS

A. Architecture

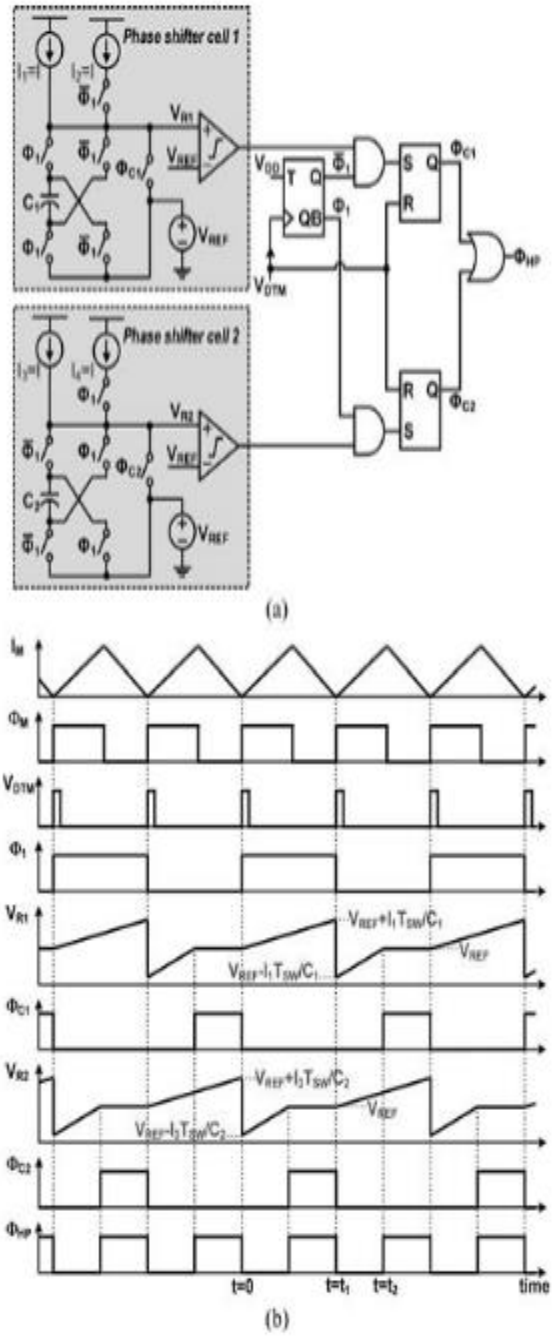

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Fig. 1 shows the block diagram of the two-phase interleaved PFC boost converter with the proposed VTPS operating at the CRM.

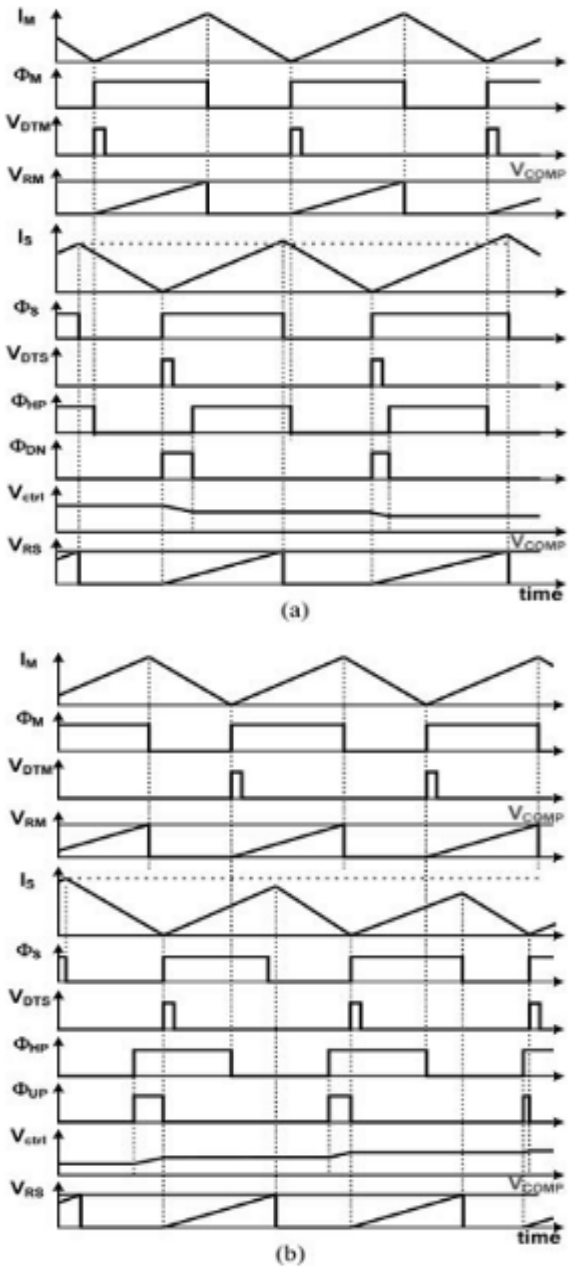

Fig . 2. Timing diagram of the two-phase interleaved CRM PFC boost converter when the slave converter turns ON (a) earlier and (b) later than desired (180^0 phase shifted from the master converter) CRM.

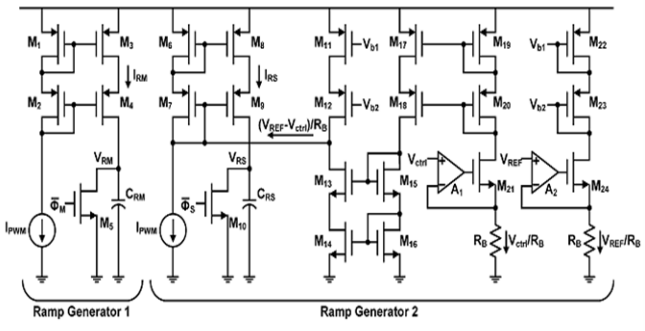

Fig 3.Ramp generator

The upper converter consisting of LM, DM, and SM is the master and the lower one consisting of LS, DS, and SS is the slave [12]-[14]. The output voltage level is compared with the reference level generated by the band gap reference (BGR) to generate the error voltage VCOMP. For the master converter, the fixed slope ramp signal VRM is compared with the error voltage VCOMP and the switching signal ΦM becomes LOW when VRM is larger than VCOMP, decreasing the inductor current IM. The voltage level of the secondary winding of the transformers is utilized to detect the zero current of the primary winding. The zero current detectors (ZCD) generate the pulse VDTM, setting ΦM to HIGH when the voltage level of the secondary winding is lower than the reference level.

The operation of the slave converter is similar to that of the master except that the slope of the ramp signal V_{RS} is variable to get the accurate 180^0 phase difference between the master and slave converters. The slope of VRS is adjusted by the phase shifting loop consisting of the phase-frequency detector (PFD), charge pump (CP), loop filter, and ramp generator, so the rising edge of the ZCD output V_{DTS} of the slave converter is locked to that of ΦHP which is 180^0 phase shifted from V_{DTM} by the phase shifter. Because the switch SS of the slave converter is turned ON by the rising edge of V_{DTS}, the turn-ON instant of the slave converter is 180^0 phase shifted from that of the master converter [15].

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Fig. 1 shows the timing diagram of the two-phase CRM PFC boost converter employing the previously explained phase control scheme. If the slave converter is turned ON earlier (later) than desired, meaning V_{DTS} is faster (slower) than ΦHP, the loop filter output Vctrl controlling the slope of VRS is decreased (increased). Then, the turn-OFF instant of the slave converter becomes slower (faster), which in turn makes the turn-ON instant of the slave converter slower (faster). Because the phase shifting loop locks the rising edge of V_{DTS} to that of ΦHP, the accuracy of the phase shifter is very critical to achieve the desired 180^0 phase shift between the master and slave converters. The VTPS described below ensures the accurate 180^0 phase shift.

B. Variation-Tolerant Phase Shifter

Fig. 2(a) shows the proposed V_{TPS} with its timing shown in Fig. 2(b). When the inductor current of the master converter is zero, the ZCD of the master converter generates a short pulse of the frequency of VDTM is 500 kHz

$$V_{R1}=V_{VREF}-\frac{I_1.T_{SW,n-1}}{C_1}+\frac{(I_1+I_2).t_2}{C_1}=V_{REF} \quad (1)$$

And t_2 can be rearranged as

$$t_2=\frac{I_1}{I_1+I_2}.T_{SW,n-1}=\frac{1}{2}T_{SW,n-1}. \quad (2)$$

Since the switching frequency for PFC control changes slowly due to the low bandwidth of the PFC control loop, the previous switching periodTsw, n−1is almost equal to the present switching period Tsw , n and, therefore, t_2 is

$$t_2=\frac{1}{2}T_{SW,n}. \quad (3)$$

At t=t_2, Φ_{C1} becomes HIGH to set Φ_{HP}, meaning Φ_{HP} is delayed by 180^0 from V_{DTM}. As explained previously, the phase shifter cell 1 generates Φ_{HP} delayed by 180^0 from V_{DTM} whenΦ_1=LOW. WhenΦ_1=HIGH,Φ_{C2} becomes HIGH by the phase shifter cell 2 to generate Φ_{HP} delayed by 180^0 from V_{DTM}. While the conventional phase shifter requires UP and DOWN current sources whose matching is critical but cannot be very good, the proposed one requires only UP current sources, which can be easily matched [16]. A Monte Carlo simulation has been performed to see the achievable accuracy of the phase shift under environmental variations and the results are shown in Fig. 3. The x-axis is the phase difference between the input signal V_{DTM} and the output signal Φ_{HP}; they-axis represents the number of events. In order to compare the phase shifting accuracy with the conventional ones, the conventional phase shifters with UP and DOWN current sources [17] and with a sample-and-hold circuit [18] are also simulated. As can be seen in the figure, the proposed VTPS shows much better phase shifting accuracy than the others against the environmental variations.

Fig. 4 clearly illustrates the importance of the accurate phase shift between the two converters, where the simulated ripple of the input current at the peak of the input line ac voltage is shown as a function of the phase difference of the two converters for the input line voltage of 90 V_{RMS} and the output current of 700 mA [19]-[21].

C. Ramp Generator

For the proper operation of the interleaved PFC boost converter, the slope of the ramp signal V_{RS} of the slave converter should be adjusted by the loop filter output Vctrl. On the contrary, the ramp signal V_{RM} of the master converter has a fixed slope. The ramp generators shown in Fig. 3 provide the required V_{RM} And V_{RS} accordingly. The currents of the transistorsM21 and M24are given as Vctrl/R_B and V_{REF}/R_B, respectively, and are copied to the transistorsM14andM11, respectively. Then, the charging current I_{RS} of the ramp generator 2 is IPWM−(VREF–Vctrl)/R_B. Therefore, the ramp slope of the slave converter increases when the loop filter output Vctrl becomes larger. Because the charging current I_{RM} of the ramp generator 1 is constant, the ramping slope of the master converter is fixed

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D. Stability of the Phase Shifting Loop with the VTPS

In the CRM PFC boost converter, the switching period t_{sw} is the sum of the on-time ton and off-time off of the switch and is given as

$$t_{SW} = t_{on} + t_{off} = t_{on} + \left(\frac{v_{in}}{v_o - v_{in}}\right) t_{on} = \left(\frac{v_o}{v_o - v_{in}}\right) t_{on} \quad (4)$$

Where v_{in} and v_{out} are input and output voltages, respectively .The variables in (4) can be represented as the sum of the dc value and small-signal variation component as

$$t_{SW} = T_{SW} + \hat{t}_{SW}$$
$$t_{on} = T_{on} + \hat{t}_{on}$$
$$v_o = V_O + \hat{v}_o$$
$$v_{in} = V_{in} + \hat{v}_{in} \quad (5)$$

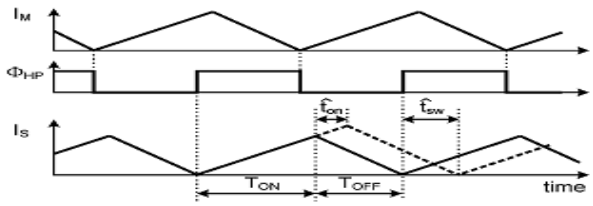

Fig. 4. Perturbation of the switching period when the small on-time perturbation^ ton is induced at the slave converter.

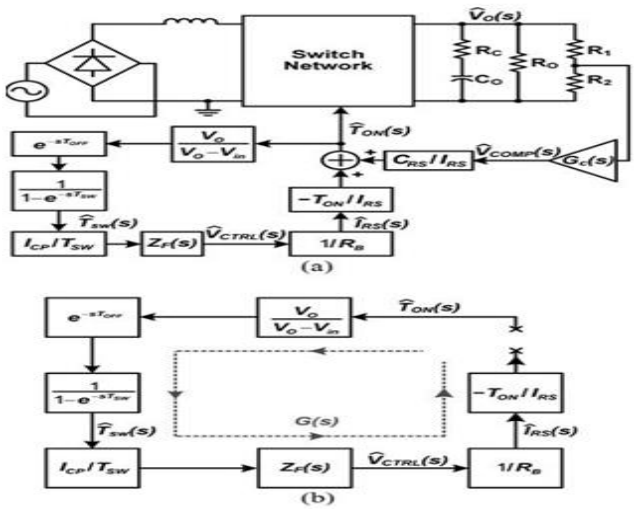

Fig. 6. (a) Small signal model of the slave converter with the VTPS and (b) its open-loop model.

Then,(4)can be rearranged as

$$T_{SW} + \hat{t}_{SW} = \left(\frac{V_o + \hat{v}_o}{V_o + \hat{v}_o - V_{in} - \hat{v}_{in}}\right)(T_{ON} + \hat{t}_{on}) \quad (6)$$

Assuming $\hat{v}_{in}$ and $\hat{v}_o$ are zero, the aforementioned equation becomes

$$\boldsymbol{T_{SW} + \hat{t}_{SW}} = \left(\frac{v_o}{v_o - v_{in}}\right)(\boldsymbol{T_{ON}} + \hat{\boldsymbol{t}}_{\boldsymbol{on}}) \left(\frac{v_o}{v_o - v_{in}}\right)\boldsymbol{T_{on}} + \left(\frac{v_o}{v_o - v_{in}}\right)\hat{\boldsymbol{t}}_{\boldsymbol{on}} \quad (7)$$

Removing dc values in (7), we obtain the following relationship:

$$\hat{\boldsymbol{t}}_{\boldsymbol{SW}} = \left(\frac{v_o}{v_o - v_{in}}\right)\hat{\boldsymbol{t}}_{\boldsymbol{on}} \quad \textbf{(8)}$$

$$\hat{\boldsymbol{t}}_{\boldsymbol{SW}}(\boldsymbol{t}) = \left(\frac{V_o}{V_o - V_{in}}\right)\hat{\boldsymbol{t}}_{\boldsymbol{on}}(\mathbf{t}).\boldsymbol{\delta}(\boldsymbol{t} - \boldsymbol{T_{OFF}}) \quad (9)$$

If there is a variation in the on-time^ ton of the slave converter with the VTPS, the switching period^ tsw would change after some finite delay T_{OFF} as shown in Fig. 6. This can be expresses as [21Therefore,^ tsw of thenth cycle is the sum of the ^ tsw of the (n–1)th cycle and the variation due to the change in the on-time ^ ton, which can be represented as

$$\hat{\boldsymbol{t}}_{\boldsymbol{SW,n}}(\boldsymbol{t}) = \hat{\boldsymbol{t}}_{\boldsymbol{SW,n-1}}(\boldsymbol{t}) + \hat{\boldsymbol{t}}_{\boldsymbol{on,n}}(\boldsymbol{t}).\left(\frac{V_o}{V_o - V_{in}}\right).\boldsymbol{\delta}(\boldsymbol{t} - \boldsymbol{T_{OFF}}) \quad (10)$$

Taking the Laplace transformation of (10), we obtain therefore, the transfer function is

$$\hat{\boldsymbol{T}}_{\boldsymbol{SW,n}}(\boldsymbol{s}) - \hat{\boldsymbol{T}}_{\boldsymbol{SW,n}}(\boldsymbol{s}).\boldsymbol{e}^{-\boldsymbol{sT_{sw}}} = \hat{\boldsymbol{T}}_{\boldsymbol{on,n}}(\boldsymbol{s}).\left(\frac{V_o}{V_o - V_{in}}\right).\boldsymbol{e}^{-\boldsymbol{sT_{OFF}}} \quad (11)$$

Therefore, the transfer function $\frac{\hat{T}_{SW}(s)}{\hat{T}_{ON}(s)}$ is

$$\frac{\hat{\boldsymbol{T}}_{\boldsymbol{SW}}(\boldsymbol{s})}{\hat{\boldsymbol{T}}_{\boldsymbol{ON}}(\boldsymbol{s})} = \frac{\hat{\boldsymbol{T}}_{\boldsymbol{SW,n}}(\boldsymbol{s})}{\hat{\boldsymbol{T}}_{\boldsymbol{on,n}}(\boldsymbol{s})} = \frac{1}{1 - \boldsymbol{e}^{-\boldsymbol{sT_{SW}}}}.\left(\frac{V_o}{V_o - V_{in}}\right).\boldsymbol{e}^{-\boldsymbol{sT_{OFF}}} \quad (12)$$

When the switching period changes, the PFD and CP generate the pumping current for^ tsw and the loop filter output is given as

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$$\hat{V}_{CTRL}(s) = I_{CP}.\frac{\hat{T}_{SW}(s)}{T_{SW}}.Z_F(s) \quad (13)$$

$$\hat{\imath}_{rs} = \frac{\hat{v}_{ctrl}}{R_B} \quad (14)$$

and by the Laplace transformation

$$\hat{I}_{RS}(S) = \frac{\hat{V}_{ctrl}(s)}{R_B} \quad (15)$$

The variation of the charging current IRS of the ramp generator changes the on-time as

$$T_{ON} + \hat{t}_{on} = \frac{V_{COMP}.C_{RS}}{I_{RS}+\hat{\imath}_{rs}} \quad (16)$$

which can be rearranged as

$$T_{ON}I_{RS} + T_{ON}\hat{\imath}_{rs} + I_{RS}\hat{t}_{on} + \hat{t}_{on}\hat{\imath}_{rs} = V_{COMP}C_{RS} \quad (17)$$

The last term of the left part of (17) can be neglected, and because $T_{ON} = \frac{V_{COMP}C_{RS}}{I_{RS}}$

$$T_{ON}\hat{\imath}_{rs} + I_{RS}\hat{t}_{on}=0 \quad (18)$$

Therefore, the transfer function^ TON(s)/^IRS(s) can be obtained as

$$T_{ON}\hat{\imath}_{rs} + I_{RS}\hat{t}_{on}=0 \quad (19)$$

From the aforementioned observations, the small signal model of the phase shifting loop with the VTPS can be obtained as shown in Fig. 9(a) Because the crossover frequency of the voltage regulation loop of the PFC converter is very low.

SIMULATION RESULTS

Here simulation is carried out in several cases, in that

1). Improvement of Power Factor using AC/DC Single Stage Conversion Operated under Phase Shifted Technique.

2). Improvement of Power Factor using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique

3). Improvement of Power Factor using AC/DC Single Stage Conversion with PI and Fuzzy controllers

Case 1: Improvement of Power Factor using AC/DC Single Stage Conversion Operated under Phase Shifted Technique

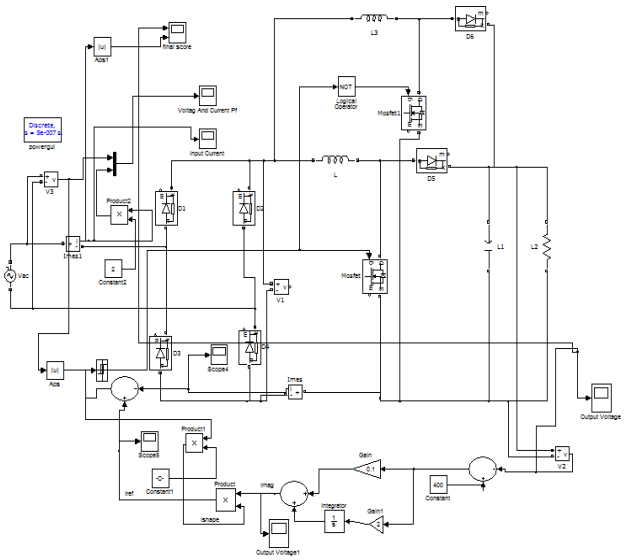

Fig.7 Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique

Fig.7 shows the Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique using Matlab/Simulink software package.

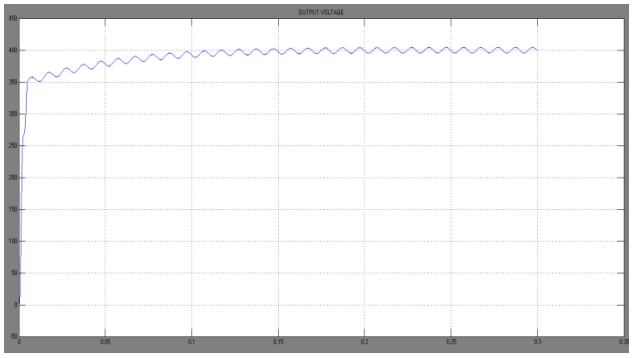

Fig.8 Output Voltage

Fig.8 shows the Output Voltage of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique.

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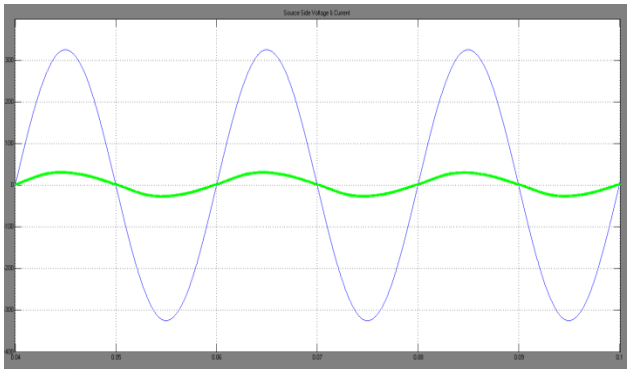

Fig.9 Source Side Voltage & Current

Fig.9 shows the Source Side Voltage & Current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique, which represents the both voltage & current would be placed in in-phase condition, get unity power factor.

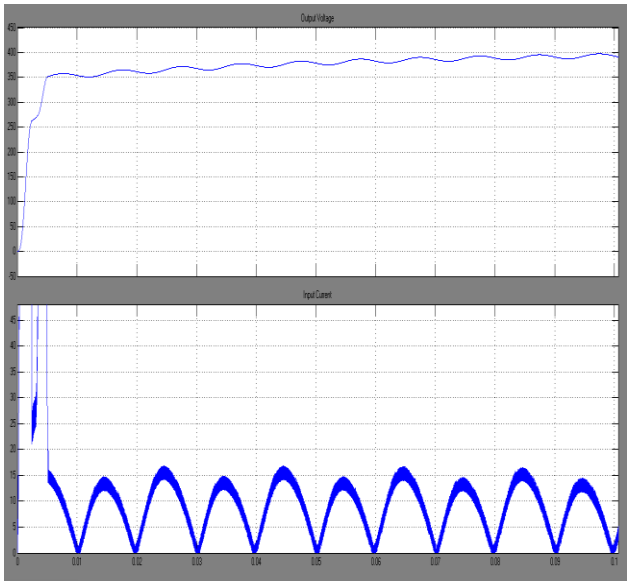

Fig.10 Output Voltage & Input Current

Fig.10 shows the Output Voltage & Input Current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique.

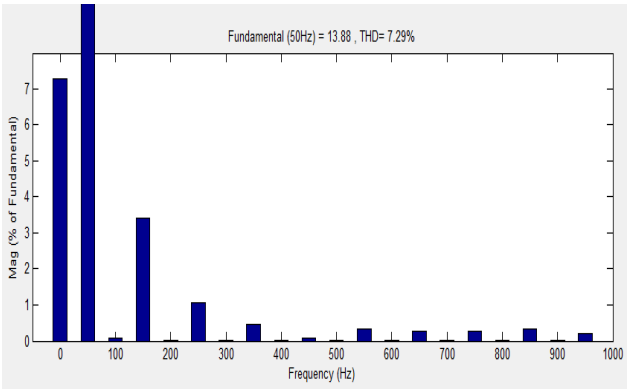

Fig. 11 FFT analysis of source current

Fig. 11 shows the FFT analysis of source current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Phase Shifted Technique, get 7.29%.

Case 2: Improvement of Power Factor using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique

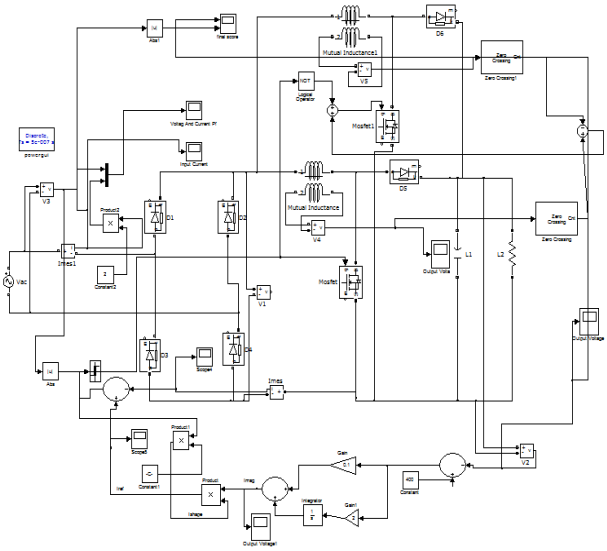

Fig.12 Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique

Fig.12 shows the Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique using Matlab/Simulink software package.

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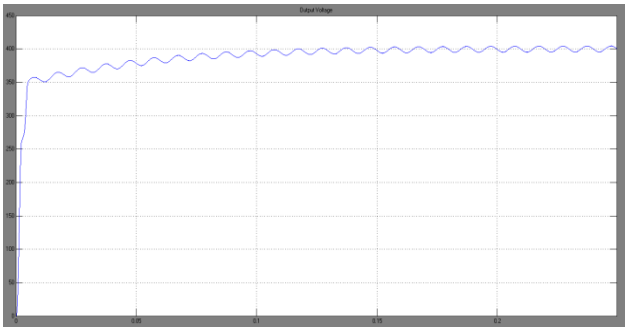

Fig.13 Output Voltage

Fig.13 shows the Output Voltage of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique.

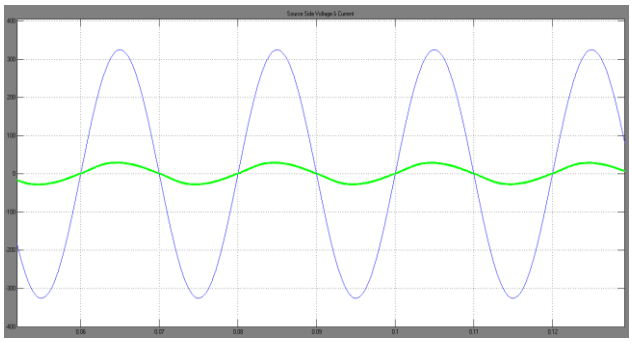

Fig.14 Source Side Voltage & Current

Fig.14 shows the Source Side Voltage & Current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique, which represents the both voltage & current would be placed in in-phase condition, get unity power factor.

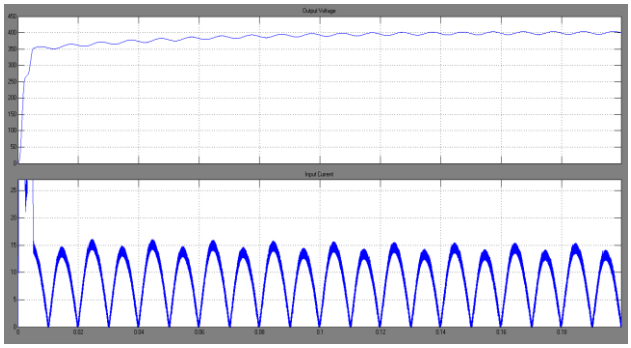

Fig.15 Output Voltage & Input Current

Fig.15 shows the Output Voltage & Input Current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique.

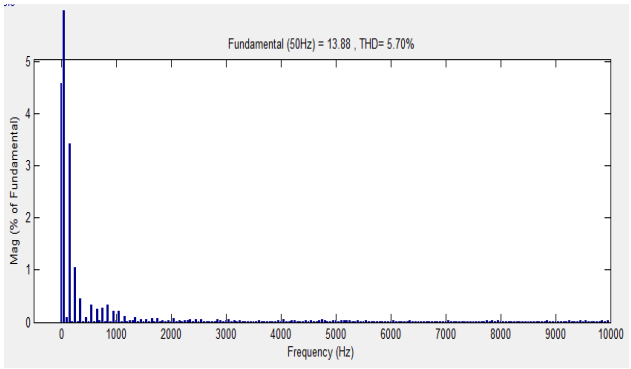

Fig. 16 FFT analysis of source current

Fig. 16 shows the FFT analysis of source current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique, get 5.70%.

Case 3: Improvement of Power Factor using AC/DC Single Stage Conversion with fuzzy controller.

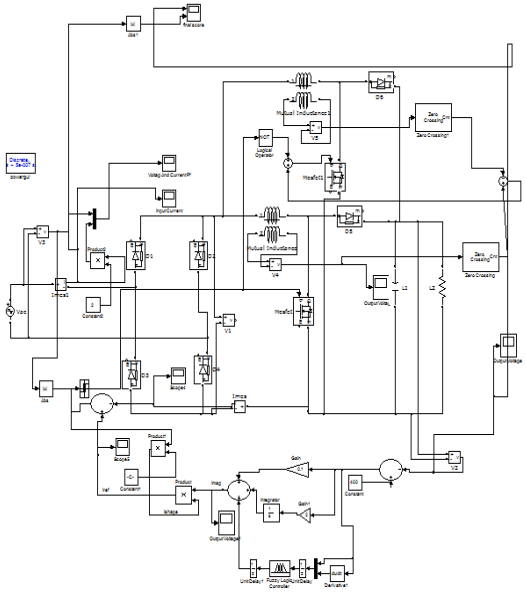

Fig.17 Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion using fuzzy Operated under Variable Phase Shifted Technique

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Fig.17 shows the Matlab/Simulink Model of Proposed Power Factor Correction using AC/DC Single Stage Conversion using fuzzy Operated under Variable Phase Shifted Technique using Matlab/Simulink software package.

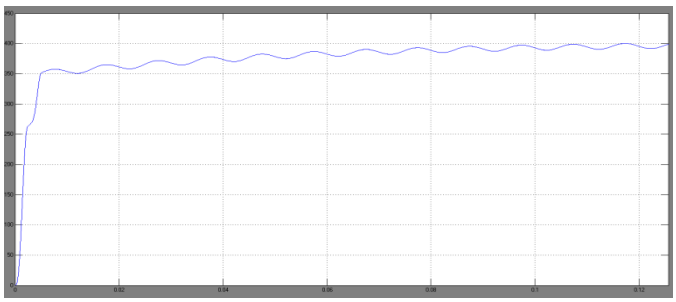

Fig.18 Output voltage

Fig.18 shows the output voltage of Proposed Power Factor Correction using AC/DC Single Stage Conversion using fuzzy controller Operated under Variable Phase Shifted Technique.

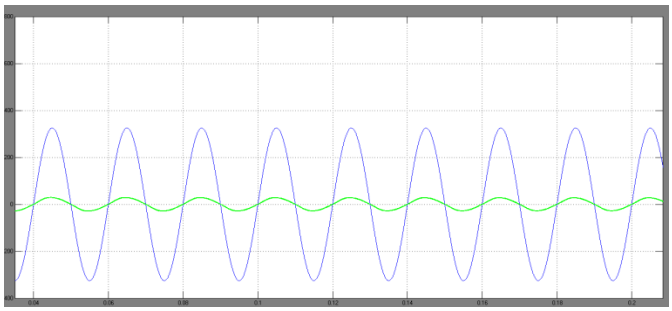

Fig.19 Source Side Voltage & Current

Fig.19 shows the Source Side Voltage & Current of Proposed Power Factor Correction using AC/DC Single Stage Conversion Operated under Variable Phase Shifted Technique with fuzzy controller, which represents the both voltage & current would be placed in in-phase condition, get unity power factor.

CONCLUSION

Here proposed new converter topology to control of fuzzy with improved power quality features by using different control actions, attain lower THD values. This paper discusses several fundamental issues related to the topological derivation, analysis, and control of TL dc–dc converters. Furthermore, it has been demonstrated that the proposed feed forward control scheme works well in maintaining an equal voltage among the dividing capacitors used in the converters. For a two-phase interleaved PFC converter, a variation tolerant 180^0 phase shifter has been developed and applied to a 320-W CRM PFC boost converter implemented in a simulation process. The input current ripple can be greatly reduced with the proposed phase shifter compared with the conventional phase shifting techniques. The proposed DC-DC converter is simulated under PI controller and Fuzzy logic controller. The Input harmonic distortion content for both controllers is presented in the above results and it is shown that for PI controller it gave 7.29% while the THD for Fuzzy logic controller is 5.70%.Although the proposed phase shifter has been applied to a PFC boost converter with DC machine drive to check the performance characteristics of the drive , it can be used in any type of two-phase interleaved switching power converter.

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