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A High Performance Clock Gated Flipflops Design Using Auto Gating Technique

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ABSTRACT:

Power Dissipation plays a major impact in development of the Low Power Devices. In order to increase performances of a system new processor with high operating frequency are designed which may increases the dynamic power dissipation of a circuit. Since Flip-Flops are the major building blocks of the Digital design which may depends on the Clock signal. So these Flip-Flops consume more power than any other circuit. In order to reduce the dynamic losses of the flip-flop here we introduce a data driven clock gating technique and later we proposed Look ahead Clock Gating technique with Auto Gated Flip-Flo. These designes are carried out using 22nm technology using Tanner EDA Software.

KEYWORDS: Clock Gating, AGFF, LACG, Tanner Tools.

1.INTRODUCTION:

Energy dissipation is a very critical parameter that has to be taken into account during the design of VLSI circuits. With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery-operated portable devices a major concern. High power consumption reduces the battery service life. The goal of low-power design for battery-powered devices is thus to extend the battery service life while meeting performance requirements. Reducing power dissipation is a design goal even for non-portable devices since excessive power dissipation results in increased packaging and cooling costs as well as potential reliability problems.

To address these issues directly, it is essential to understand the different types and the CMOS technology is that it is currently the most dominant digital IC implementation technology. Power dissipation in CMOS digital circuits is categorized into two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance.

The voltage drop effects, caused by the excessive instantaneous current owing through the resistive power network, affect the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit.

Also noise margins are reduced, increasing the chance of chip failure due to crosstalk. CMOS digital circuits occur in two forms: dynamic and static. Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance associated with the gate's transistors has to be charged, thereby consuming power. Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another).

Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices For dynamic loss reduction we are using Clock Gating technique and for static loss reduction we are suing RTPG technique explained below.

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CLOCK GATING AND POWER GATING:

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. [1] Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of muxes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree. Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

INTEGRATED CLOCK AND POWER GATING:

Clock Gating and Power Gating are two most commonly used design methods to save dynamic and leakage power respectively. How about integrating the two solutions such that they complement each other? In this post, I will talk about a simple way to do so.

CLOCK GATING:

Clock signals are omnipresent in synchronous circuits. The clock signal is used in a majority of the circuit blocks, and since it switches every cycle, it has an activity factor of 1. Consequently, the clock network ends up consuming a huge fraction of the on-chip dynamic power. Clock gating has been heavily used in reducing the power consumption of the clock network by limiting its activity factor. Fundamentally, clock gating reduces the dynamic power dissipation by disconnecting the clock from an unused circuit block.

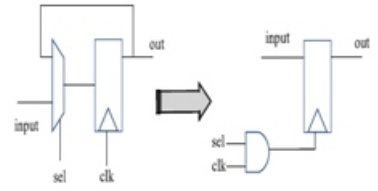

Fig 1. Clock Gating

Fig. 2.1 In its simplest form, clock gating can be implemented by finding out the signal that determines whether the latch will have a new data at the end of the cycle. If not, the clock is disabled using the signalTraditionally, the system clock is connected to the clock pin on every flip-flop in the design. This results in three major components of power consumption:

1. Power consumed by combinatorial logic whose values are changing on each clock edge;
2. Power consumed by flip-flops – this has a non-zero value even if the inputs to the flip-flops are steady, and the internal state of the flip-flops is constant;
3. Power consumed by the clock buffer tree in the design. Clock gating has the potential of reducing both the power consumed by flip-flops and the power consumed by the clock distribution network.

Clock gating works by identifying groups of flip-flops sharing a common enable signal (which indicates that a new value should be clocked into the flip-flops). This enable signal is ANDed with the clock to generate the gated clock, which is fed to the clock ports of all of the flip-flops that had the common enable signal. For high-performance design with short-clock cycle time, the clock skew could be significant and needs to be taken into careful consideration. An important consideration in the implementation of clock gating for ASIC designers is the granularity of clock gating. Clock gating in its simplest form is shown in Fig. 2.1. At this level, it is relatively easy to identify the enable logic. In a pipelined design, the effect of clock gating can be multiplied. If the inputs to one pipeline stage remain the same, then all the later pipeline stages can also be frozen.

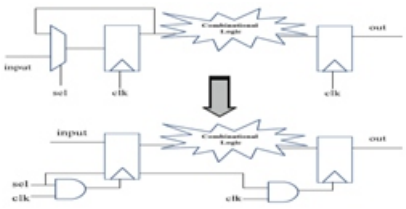

Fig 2. In pipelined designs, the effectiveness of clock gating can be multiplied.

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If the inputs to a pipeline stage remain the same, then the clock to the later stages can also be frozenFigure 2 shows the same clock gating logic being used for gating multiple pipeline stages. This is a multi-cycle optimization with multiple implementation tradeoffs, and can save significant power, typically reducing switching activity by 15–25%. Apart from pipeline latches, clock gating is also used for reducing power consumption in dynamic logic. Dynamic CMOS logic is sometimes preferred over static CMOS for building high speed circuitry such as execution units and address decoders. Unlike static logic, dynamic logic uses a clock to implement the combinational circuits. Dynamic logic works in two phases, pre charge and evaluate. During pre charge (when the clock signal is low) the load capacitance is charged. During evaluate phase (clock is high) depending on the inputs to the pull-down logic, the capacitance is discharged.

DATA DRIVEN CLOCK GATING TECHNIQUE:

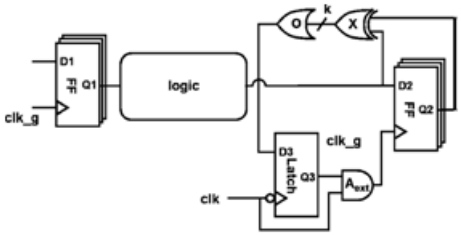

Fig 3. Clock implementation of data-driven clock gating.

In Data Driven Clock gating technique gated clock signal was disabled whenever their was switching activity was done in the Input. The structure consists of xor gate which compares the input and output for every flip-flop and all the outputs are tied to the or gate in order to generate a enable signal which will drive latch with and gate clock gating circuit. Whenever the input was changed to any flip-flop then xor gate generates an enable signal and it passed on generates a clock enable signal to the grouping.

Data-driven gating is shown in above fig,A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The outputs of XOR gates are ORed to generate a joint gating signal for FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is used by commercial tools and is called Integrated Clock Gate (ICG) It is beneficial to group FFs whose switching activities are highly correlated.

Data-driven gating suffers from a very short time-window where the gating circuitry can properly work. This is illustrated in Fig The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF. Such constraints may exclude 5%-10% of the FFs rom being gated due to their presence on timing critical pathsIn order to over these we show Auto Gated Flip-Flop

AUTO GATED FLIP-FLOP:

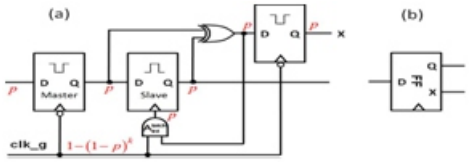

Fig 4. An auto-gated flip-flop.

The FF's master latch becomes clear on the falling edge of the clock, wherever its output should stabilize no later than a setup time before the arrival of the clock's rising edge, when the master latch becomes opaque and also the XOR circuit indicates whether or not the slave latch ought to amendment its state. If it does not, its clock pulse is stopped and otherwise it's passed. In [12] a significant power reduction was rumored for register-based small circuits, like counters, wherever the input of every FF dependson the output of its precursor within the register. AGFF can also be used for general logic, however with 2 major drawbacks.Firstly, solely the slave latches ar gated, exploit 1/2 the clock load not gated. Secondly, serious temporal arrangement constraints ar imposed on those FFs residing on important ways, that avoid their gating In auto gated Flip-Flop clock enable signal was generated one clock cycle ahead .

LACG LOGIC:

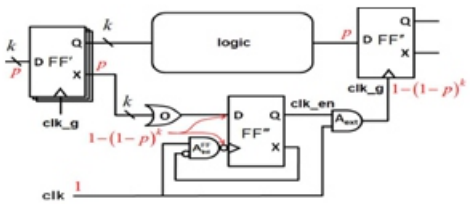

Fig 5. LACG of general logic

LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints.

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LACG is based on using the XOR output in Fig. 4 to generate clock enabling signals of other FFs in the system, whose data depend on that FF. There is a problem though. The XOR output is valid only during a narrow window of around the clock rising edge, where and are the FF's setup time and clock to output contamination delay, respectively. After a delay the XOR output is corrupted and turns eventually to zero. To be valid during the entire positive half cycle it must be latched as shown in Fig. 5(a). Fig. 5(b) is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input . Such gating has been proposed in [16] and it involves another XOR and OR gates, useful for high clock switching probability.

SIMULATION AND RESULTS:

These Circuits are designed and simulated using Tanner Tools 13.0

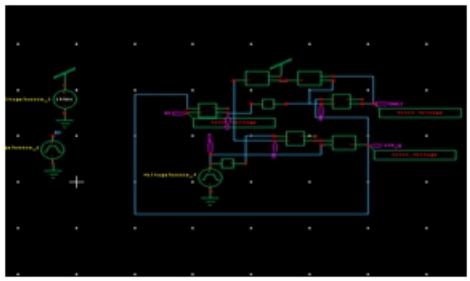

Fig 6. Data Driven Clock Gating S-Edit Design

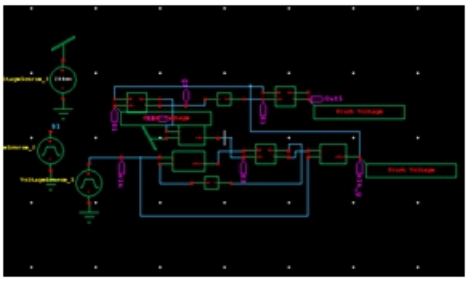

Fig 7. Look ahead Clock Gating S-Edit Design

NON CLOCK GATING SCHEMATIC DESIGN:

The NON-CG Schematic Design Shown in fig 8.1 is designed using S-EDIT of TANNER tool.

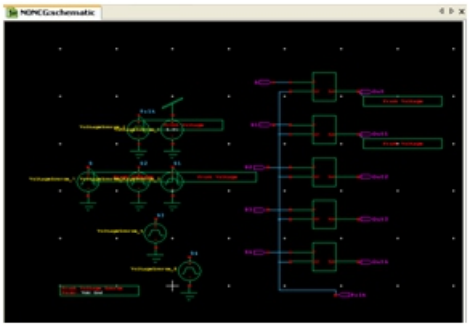

Fig 8. Design of Non Clock Gating

CLOCK GATING SCHEMATIC DESIGN:

The CLOCK GATING schematic design shown in fig 8.3 is designed using S-EDIT of TANNER tool.

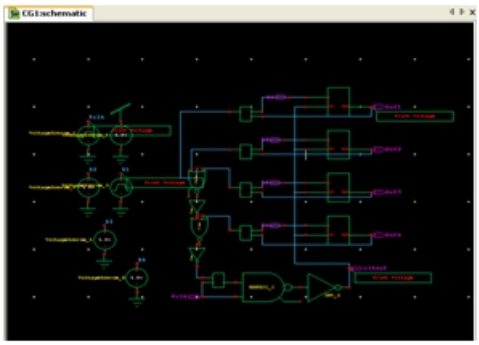

Fig 9. Design of clock gating

CLOCK GATING WITHOUT RTPG SCHEMATIC DESIGN:

The CLOCK GATING WITHOUT RTPG schematic design shown in fig 8.5 is designed using S-EDIT of TANNER tool.

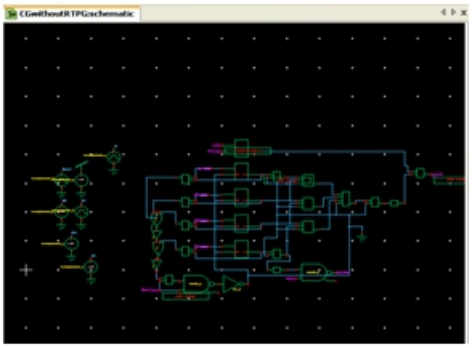

Fig 10. Design of clock gating without RTPG

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CLOCK GATING WITH RTPG SCHEMATIC DESIGN:

The CLOCK GATING WITH RTPG Schematoc design shown in fig 8.7 is designed using S-EDIT of TANNER tool.

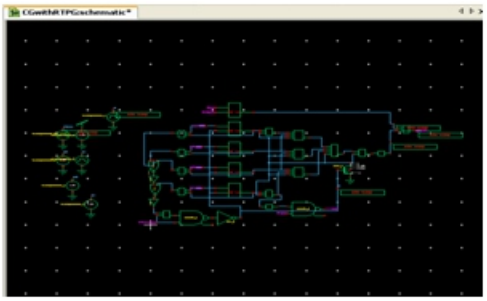

Fig 11. Design of clock gating with RTPG

The simulation of NON CLOCK GATING is done using LT-SPICE of TANNER tool and the output is shown in fig 8.2.

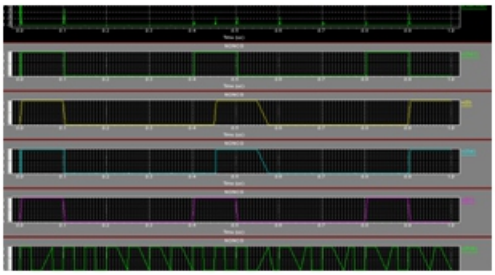

Fig 12. output of non clock gating

The simulation of CLOCK GATING is done using LT-SPICE of TANNER tool and the output is shown in fig 8.3.

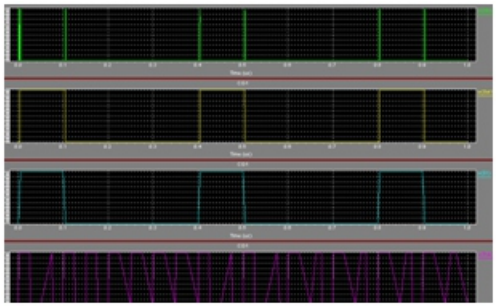

Fig 13. output of cock gating.

The simulation of CLOCK GATING WITHOUT RTPG is done using LT-SPICE of TANNER tool and the output is shown in fig 8.5

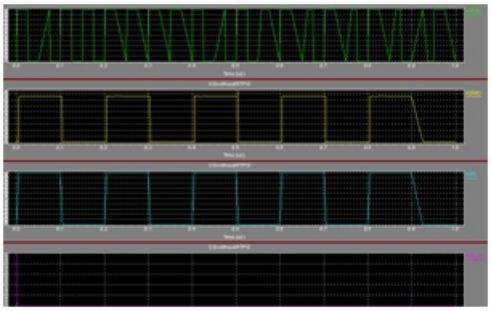

Fig 14. Output of clock gating without RTPG

The simulation of CLOCK GATING WITH RTPG is done using LT-SPICE of TANNER tool and the output is shown in fig8.8.

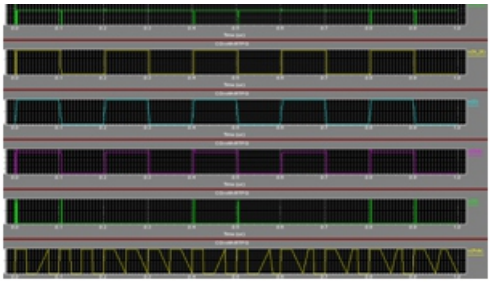

Fig 15. output of clock gating with RTPG

COMPARISION TABLES:

Circuit	**Power Dissipation**
DDCG	2.312750e-007 watts
LACG	1.653563e-008 watts
Circuit	**Time Delay**
DDCG	9.6391e-009
LACG	8.6123e-009

CONCLUSION:

In this Paper, we implemented the Clockgating technique integration in order to reduce the dynamic power in Flip-Flops and later we extend to Auto Gated Flip-Flop which will reduce the more power consumption with one clock head of gating.

FUTURE SCOPE: For Integration of clock gating reduces the dynamic power dissipation later we can extend this power gating in order to reduce the . static power dissipation.

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