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Design and Implementation of Fault Coverage Circuits for Testing All VLSI Elements

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Abstract:

A new fault coverage test pattern generator using a linear feedback shift register (LFSR) called FC-LFSR can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

Keywords:

LFSR, Optimization, Low Power, Test Pattern Generation, BIST.

INTRODUCTION:

1.1 Objective:

The VLSI circuit manufacturer cannot guarantee the defect free integrated circuits(IC's).This makes us to evolve a fast accurate means of testing such circuits. In a small-scale environment, it may not be feasible to invest large sums of money into complex IC testers. In labs till now we are having Digital testers which will test IC's based on some non functional parameters like temperature, any short circuits in the IC etc. & are used for testing only Combinational circuits. In this paper, the validation is based on functionality of IC. The digital pattern generator and logic analyzer are used to test the combinational, sequential circuits. This paper describes a versatile but inexpensive, testing system for standard digital IC's (7400-series transistor-transistor logic (TTL)[1] based on the use of a FPGA.

This tester can be economically implemented for small or medium-scale users of such IC's & provides a quick but thorough checkout of most small & medium-scale functions with minimal operator action. Dedicated special-purpose hardware is minimal, allowing this tester to be implemented on virtually FPGA. Each IC is tested by applying test patterns to input pins of the chip & the resulting chip outputs are then examined for errors resulting from the stuck-at conditions or other functional errors [3]. For Dedicated ATE, all input & output patterns expected outputs, For Generalized ATE, the DUT output can be stored in the Logic analyzer & user need to check the functionality based on the input & output results. This ATE can be used to test the combinational and sequential circuits. The test set for each IC is an exhaustive set of all possible input combinations; this ATE is used for SSI & MSI functions.

1.2. Introduction to Automated Test Equipment:

The automated test equipment is useful for functional testing, debug of new designs and failure analysis of existing designs. The automated test equipment can be used early in the design cycle to substitute for system components that are not yet available. For example, a automated test equipment might be programmed to send interrupts and data to a newly developed bus circuit when the processor that would normally provide the signals doesn't yet exist. automated test equipment consists of

1. Frequency synthesizer 2. Switch matrix 3. Control blocks

Automatic or Automated Test Equipment (ATE) is any apparatus that performs tests on a device, known as the Device Under Test (DUT) or Unit Under Test (UUT), using automation to quickly perform measurements and evaluate the test results.

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ATE systems are designed to reduce the amount of test time needed to verify that a particular operation. One ATE tests several (usually identical) devices at the same time. DUT has greater than 1 circuit. ATE handles multiple devices simultaneously.

2. BASIC BIST ARCHITECTURE:

The various components of BIST hardware are the test pattern generator (TPG), the test controller, circuit under test (CUT), input isolation circuitry and the output response analyzer (ORA). This is shown in the figure 2.1 below.

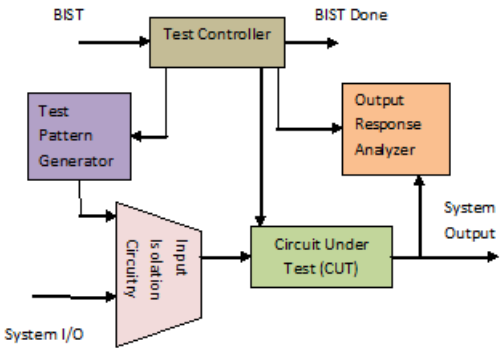

Fig 2.1 Basic BIST architecture.

2.1 Test Pattern Generator (TPG):

Responsible for generating the test vectors according to the desired technique (i.e. depending upon the desired fault coverage and the specific faults to be tested for) for the CUT. Linear feedback shift register (LFSR) and pseudo random pattern generator (PRPG) are the most widely used TPGs.

2.2 Test Controller:

Responsible for controlling the other components to perform the self test. The test controller places the CUT in test mode and allows the TPG to drive the circuit's inputs directly. During the test sequence, the controller interacts with the ORA to ensure that the proper signals are being compared.

The test controller asserts its single output signal to indicate that testing has completed, and that the ORA has determined whether the circuit is faulty or fault-free.

2.3 Output Response Analyzer (ORA):

Responsible for validating the output responses i.e. the response of the system to the applied test vectors needs to be analyzed. Also, a decision is made about the system being faulty or fault-free. LFSR and multiple input signature register (MISR) are the

3. DESIGN OF ATE:

The digital pattern generator is useful for functional testing, debug of new designs and failure analysis of existing designs. The digital pattern generator can be used early in the design cycle to substitute for system components that are not yet available. For example, a digital pattern generator might be programmed to send interrupts and data to a newly developed bus circuit when the processor that would normally provide the signals doesn't yet exist. Digital Pattern Generator (DPG) consists of

1. Frequency synthesizer 2. Switch matrix 3. Control blocks.

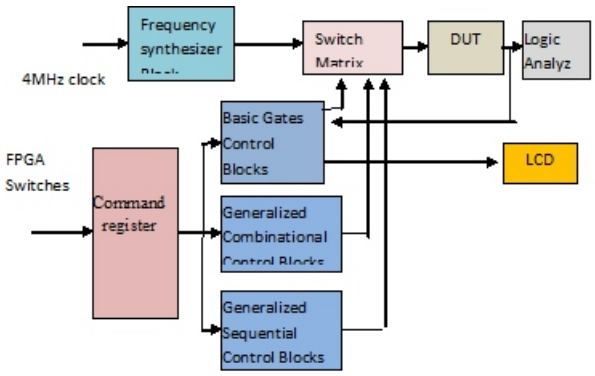

Fig.3.1. Block diagram of Automatic Test Equipment for Digital Integrated Circuits

3.1 Frequency synthesizer:

Frequency synthesizer will produce different frequency signals by the excitation of a 4MHz clock signal. The clock signal has been generated from a crystal oscillator which generates six different frequencies ranging from 1 Hz to 1 MHz Frequency Synthesizer is nothing but designing different counters so that required clock frequency can be obtained. Sparten2 FPGA consists of 4 MHz crystal oscillator. As shown in the figure 3.2, six different frequencies are generated first by using mod 4 counter 1 MHz clock. .

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Use 1Mhz as a clock and give it to mod 10 counter to generate 100Khz in the same way three more mod 10 counters are used to obtain 10Khz,1Khz and 100hz.finally to generate 1hz mod 100 counter is used by giving 100hz as a clock.

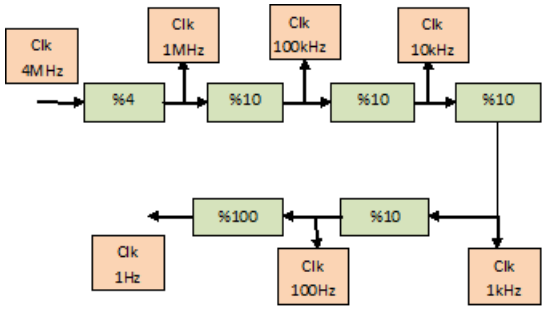

Fig.3.2.Generation of different frequency signals

3.2 Switch Matrix:

A switch matrix is used in test systems, in both design verification and manufacturing test, to route high frequency signals between the device under test (DUT) and measurement equipment. Since the signal routing and signal conditioning needs for a test system differ from design to design. The internal switch configuration of switch matrix as explained in figure 3.3, consists of eight 8:1 multiplexers. Each multiplexer has six inputs from frequency synthesis block and other two are Vcc and ground. The select line signals for each multiplexer was generated from control block based on DUT. If the DUT is any basic gate then select lines will be generated by basic gates control block. If the DUT is combinational integrated circuit then select lines will be generated by generalized combinational control block. The select lines will be generated by generalized sequential control block if the DUT is sequential integrated circuit.

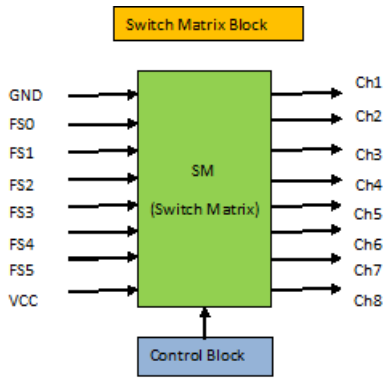

Fig.3.3.Switch Matrix Block

3.3 DUT:

3.3.1 XOR gate:

The XOR gate is a digital logic gate that implements an exclusive or; that is, a true output (1/HIGH) results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) and both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is “one or the other but not both”.

The Algebraic Expressions

$A \cdot \overline{B} + \overline{A} \cdot B$ and

$(A + B) \cdot (\overline{A} + \overline{B})$ both represent

the XOR gate with inputs A and B.

3.3.2. Array Multiplier:

The implementation of multipliers is considered first. Xilinx FPGAs such as Spartan-II as well as Virtex devices and Altera FPGAs such as APEX and Cyclone II devices have fast carry logic and dedicated AND gate for each of the Look Up Tables (LUTs) in the Slices/Logic Elements (LEs). Since multiplying an N bit number by 2 requires only AND gates and adders, fast Nx2 multipliers can be implemented using this dedicated hardware [10 & 11]. To implement a Nx4 multiplier, output of two Nx2 multipliers has to be added [12]. To implement an NxM multiplier, the output of ⌈log2M⌉ , Nx2 multipliers have to be added, 2 at a time in parallel in ⌈log2M⌉ stages appropriately.

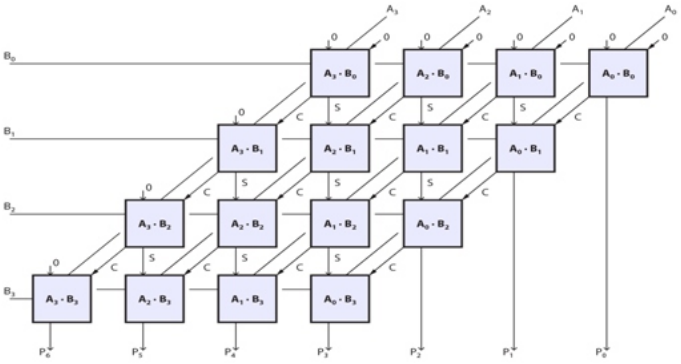

Fig.3.5.Multiplication of two numbers

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3.4 Control Block:

This module consists of three control blocks namely basic gates control block, generalized combinational control block, generalized sequential control block. The control blocks will generates the twenty four bit pattern which is used as select input signals to all the eight multiplexers, three bits to each multiplexer. The command register will receives the input signals from FPGA switches and enables the control block accordingly. Each control block generates the different select line signals based on DUT.

3.4.1 XOR gate control block:

The input conditions of xor gate are generated by using this control gate module. The test conditions values consists of 4 outputs

3.4.2 Combination control block:

The input conditions of multiplier are generated by using this control gate module. The test conditions values starts from 0000 to 1111 with the total conditions of 225 outputs .

3.4.3 Memory Control Block:

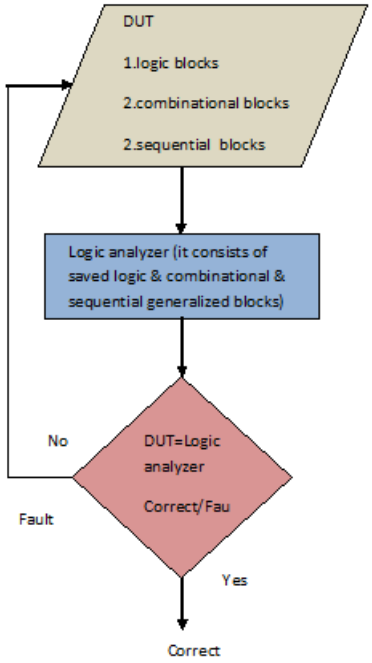
In this memory control block, write and read signals are activated. Address and Data values are generated depends upon the write and read conditions.

3.5 Logic Analyzer:

A logic analyzer is an electronic instrument which displays signals of a digital circuit and used to check and analyze the test outputs. A logic analyzer may convert the captured data into timing diagrams, protocol decodes, state machine traces, assembly language, or correlate assembly with source-level software.

Flow Chart:

By using the command register and switch matrix the logic blocks, combinational blocks , sequential block are given as input to the DUT and then to the logic analyzer . Logic analyzer consists of the saved logic, combinational and sequential blocks where the DUT three blocks are tested for the fault by comparing with the logic analyzer. If the given blocks are fault free the output is given as correct if there is any fault the output is again given to the DUT .



4. RESULTS & DISCUSSION:

The power consumed by the chip under test is a measure of the switching activity of the logic inside the chip which depends largely on the randomness of the applied input stimulus. The existing technologies reduced correlation between the successive vectors of the applied stimulus into the CUT can result in much higher power consumption by the device. The increased power may be responsible for cost, reliability, performance verification, autonomy and technology related problems.

Synthesis Report:

Minimum period: 4.007ns (Maximum Frequency: 249.563MHz)

Minimum input arrival time before clock: 8.424ns

Maximum output required time after clock: 17.999ns

Maximum combinational path delay: 20.608ns.

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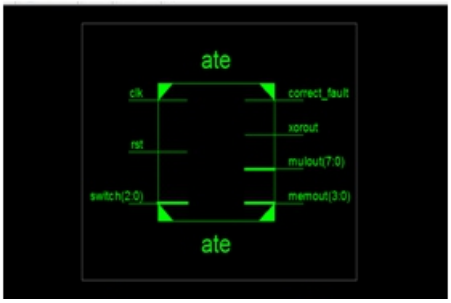
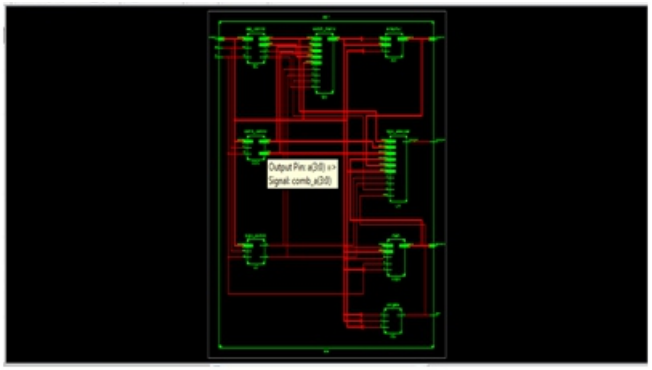
RTL Schematic:





7.4 Simulation:

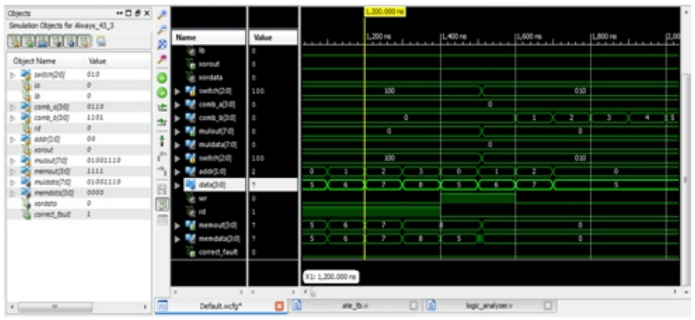
7.4.1 Logic Control:

Correct Output

Fault output\

7.4.4 Overall output:

Fault free output of logic control ,Array multiplier and memory.



CONCLUSION:

The paper proposed an optimization procedure for Test Pattern Generation (TPG) technique with reducing power dissipation during testing along with fault coverage. The transition is reduced by increasing the correlation between the successive bits, reduces the power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. The circuit is tested during the presence of fault and withoutfault for fault coverage .so, compared toe to existing the proposed method got less delay so that it we can say the proposed method is efficient in fault coverages.

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