

Low Power, Compensation Technique for Sub-Micron CMOS Amplifiers Using Minimally Invasive Process

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Abstract

Process variation is an difficulty in designing reliable CMOS mixed signal systems with high yield. To minimize the variation in voltage gain due to variations in process, supply voltage, and temperature for common trans conductance-based amplifiers, we present a new compensation method based on statistical feedback of process information. We further apply our scheme to two well known amplifier topologies in the sub-micron CMOS process as design examples—an inductively degenerated low-noise amplifier (LNA) and a common source amplifier (CSA). The proposed method improves the variation in S_{21} of an inductively degenerated cascode LNA from 8.75% to 1.27%, which is a reduction in variation of 85%. The presented scheme is also robust over variations in supply voltage, temperature, and process conditions. The compensation method presented can be utilized to stabilize the gain of a wide variety of amplifiers.

Index Terms—CMOS analog integrated circuits, process compensation, process variation, self-biasing.

I INTRODUCTION:

Low noise amplifiers (LNA) are the first active block in the receiver chain in RF communication systems. They are characterized by their high gain to suppress the influence of noise, their low noise figure, their 50 Ω match to both the input and output, and their linearity [1]. Advances made in CMOS have made it possible to easily integrate radio frequency communication systems on chip. However, with continuous scaling of

transistor sizes to improve the performance of digital systems, RF systems have, in most cases, suffered due to increased device variability in the manufacturing process. As technologies keep scaling, accurately modeling transistor performance becomes increasingly difficult [2]. Statistical uncertainty arising from sub-wavelength lithography, diffusion process, and uneven oxide thickness translate to variations in electrical parameters such as gate length, sheet resistance, threshold voltage, and gate capacitance. Non uniform deposition and diffusion of impurities translate to variations in threshold voltage [3] [4]. Work presented in [5] shows how imperative it is to keep the power gain (S_{21}) of the LNA stable to maintain both sensitivity effects and intermediation specifications. In this paper we determine that the variation in threshold voltage of the input transistor is the main contributor to gain variations of standard amplifier configurations where trans conductance determines gain. With this in mind, we design and develop a compensation scheme that measures the changes in threshold voltage and generates a bias signal for amplifiers in order to minimize deviations in their voltage gain. Our scheme can be adapted to a variety of such amplifier topologies and we experimentally demonstrate the validity of our method on two well-known amplifier topologies—an inductively degenerated cascode LNA and a common source amplifier, both used as standard gain cells in many mixed-signal system applications. Both topologies have been designed in the TSMC 65 nm CMOS process.

This work presents a compensation scheme to reduce the variations in S_{21} of an LNA by 85%. We first identify the electrical parameters which are susceptible to variability in the manufacturing process and how they translate to variations in S_{21} . We then propose a novel bias scheme to improve yield of LNAs and conclude with simulation results.

In Section II we introduce the related work on sub-micron amplifier compensation. Design methodology in section III. Design of bias circuit in section IV. simulation results are shown in section V. This paper concluded in section VI.

II RELATEDWORK:

Traditional approaches to detecting and correcting for variations in the gain of amplifiers have relied on using either built-in-self-test (BIST) devices, which either map the peak output signal to a corresponding DC value or introducing additional circuitry which adapts to variations in process. A survey of the state of the art of other LNA compensation schemes in literature shows good examples of these approaches. Han *et al.* [4] devised a calibration scheme which demonstrates significant reduction in variation of LNA gain but the presence of a DSP and tuning control circuitry makes it very costly in power and area. Jayaraman *et al.* [12] also used peak detectors to maximize S_{21} gain but off-chip calibration makes it impractical for on chip, low-power solutions. Sen *et al.* [13] used a sensing transistor at the output to control the current in the LNA. However, the large transistor used in the design makes the scheme unsuitable for low supply voltage processes. Sivonen *et al.* [14] identified that the variation in gain of an LNA is a function of its load impedance and, by replacing the load resistor with a parallel combination of different resistance ratios, they demonstrated simulated voltage gain stability over process corners. However, variation of passive elements is reported to be much smaller than that of active elements [15], therefore the major contributor is the variation of the transconductance of the G_m in (1)

with respect to the circuit parameters subject to variations in process, supply, and temperature

Therefore

$$\begin{aligned} \frac{\partial G_m}{\partial g_m} &= \frac{1}{w_0 C_{gs} (R_s + w_T L_s)} = \frac{G_m}{g_m} \\ \frac{\partial G_m}{\partial C_{gs}} &= \frac{-g_m}{w_0 C_{gs}^2 (R_s + w_T L_s)} = \frac{-G_m}{C_{gs}} \\ \frac{\partial G_m}{\partial w_0} &= \frac{-g_m}{w_0^2 C_{gs} (R_s + w_T L_s)} = \frac{-G_m}{w_0} \end{aligned}$$

Total variations in transconductance

Since inductors can be implemented as off-chip components we can assume that they have insignificant variation in this case. Therefore

$$\frac{\Delta w_0}{w_0} = \frac{-1}{2} \frac{\Delta C_{gs}}{C_{gs}}$$

And since

$$\begin{aligned} w_T &= \frac{g_m}{C_{gs}} \\ \frac{\partial G_m}{\partial w_T} &= \frac{-G_m (L_s w_T)}{(R_s + w_T L_s)} \left(\frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \right) \end{aligned}$$

In

$$\begin{aligned} &\Delta G_m \\ &= G_m \left(\frac{\Delta g_m}{g_m} \frac{\Delta C_{gs}}{C_{gs}} \frac{\Delta w_0}{w_0} \frac{L_s w_T}{(R_s + w_T L_s)} \left(\frac{\Delta g_m}{g_m} \frac{\Delta C_{gs}}{C_{gs}} \right) \right) \end{aligned}$$

Around the input match condition, $R_s = \omega T L_s$ for optimal power match.

Therefore

$$\begin{aligned} \frac{\Delta G_m}{G_m} &= \left[\frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{2 C_{gs}} - \frac{1}{2} \left(\frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \right) \right] \\ \frac{\Delta G_m}{G_m} &= \frac{1}{2} \frac{\Delta g_m}{g_m} \end{aligned}$$

This equation indicates that, in order to achieve zero variation for G_m and, hence, S_{21} , the variations in output transconductance of the input transistor of the LNA must be eliminated.

III. DESIGN METHODOLOGY

Similar to the methodology described in [8] for current generators, we develop an input transistor for the LNA whose output transconductance g_{mtotal} is the sum of the transconductances of two transistors M1 and M2 which are in parallel.

$$g_{m1} = 2k_1(v_{gs1} - v_{th1}), g_{m2} = 2k_2(v_{gs2} - v_{th2})$$

To eliminate the variation in S21 of an LNA, the variation in the output transconductance of its input transistor should be zero. In our case, $\Delta g_{mtotal} = 0$. Let us assume that V_{gs1} is set and does not vary and the nominal value of V_{gs2} is set at V_{gs1} . Transistors M1 and M2 are sized the same ($k_1 = k_2$) and placed close to each other in layout so that local match would ensure that V_{th1} approximately equals V_{th2} .

With these assumptions:

$$\Delta g_{m1} = -2k(\Delta V_{th}) + 2\Delta k(V_{gs2} - V_{th})$$

$$\Delta g_{m2} = 2k(\Delta V_{gs2} - \Delta V_{th}) + 2\Delta k(V_{gs2} - V_{th})$$

The variation in transconductance of the modified LNA is

$$\Delta g_{mtotal} = \Delta g_{m1} + \Delta g_{m2}$$

$$\Delta g_{mtotal} = 2\Delta g_{m1} + 2k\Delta V_{gs2}$$

With no variations in transconductance of the input transistor, Δg_{mtotal} equals zero, and that gives

$$\Delta V_{gs2} = 2\Delta V_{th} + \frac{2\Delta k(V_{gs1} - V_{th})}{k}$$

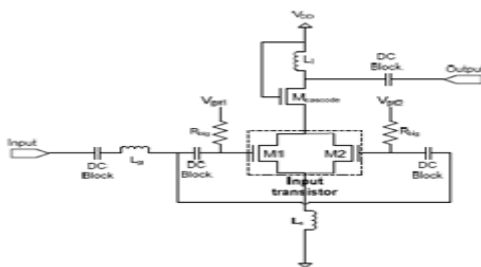


Fig Modified LNA used as a part of the compensation scheme

For a cascode LNA, the input transistor would be large to achieve substantial gain; therefore k for both M1 and M2 will be large. Also, for low power operation of the LNA, the input transistor would be biased at moderate inversion to limit the current. These two assumptions allow us to conclude that the first term dominates over the second in (9) and the condition of zero variation can be approximated by

$$V_{gs2} = 2V_{th}$$

Gives us information about the condition for $\Delta g_{mtotal} = 0$ and it also gives us a clue to its implementation. By designing a bias circuit for transistor M2 which is able to provide the following:

$$V_{gs2} = V_{gs1} + 2V_{th}$$

We will be able to design an LNA which has an S21 robust to process, supply, and temperature variations.

IV. DESIGN OF BIAS CIRCUIT

This section describes the design and implementation of a bias circuit for transistor M2 which satisfies (11). The output of this block must provide a DC bias which has an average value of V_{gs1} . It must also exhibit positive correlation with the threshold voltage by changing with twice the change in threshold voltage according to (11). by changing with twice the change in threshold voltage according to (11). variations in supply voltage. The bias circuit is designed as a four stage cascode as shown in Fig. 3. All transistors are kept in saturation and each stage is carefully sized to ensure that the condition in (11) is met for V_{out} of the bias circuit.

In the circuit, $k_i = C_{ox}(W_i/L_i)$ for transistor M1. α is a scaling factor used to bias the NMOS transistor and is generated by using a resistive divider between VDD and ground. Using wide and well matched resistors ensures that the variation on α is low. A_i are relative scaling ratios for transistors in stage i . By placing the transistors close together in layout, local match is

assumed and threshold variations of all transistors will be correlated. The first stage is self biased with two diode connected NMOS transistors. Subsequent stages take input only signals from the previous stage as input. The motivation for this is that the bias circuit should be self sufficient in tracking changes in threshold voltage, independent of the operation of the LNA. Analysis for each stage is provided in the remainder of this section.

A. First Stage:

The output signals for each stage are determined by doing a KCL analysis at each output node. Applying KCL analysis at node Vo1 and taking partial derivatives with respect to process, the following is evaluated:

$$\Delta V_{01} = \frac{\Delta V_{DD}}{A_1 + 1} + \Delta V_{th}$$

For large value of A1, total variation of V01 is given as

$$\Delta V_{01} = \Delta V_{th}$$

B. Second Stage:

Applying KCL at node Vo2 and taking partial derivatives gives us the following expression

$$\Delta V_{02} = \Delta V_{DD} - \Delta V_{th}$$

C. Third Stage:

The third and fourth stages will allow us some flexibility in choosing γ to satisfy $V_{out} = \gamma \Delta V_{th} + V_{gs1}$ and approximate the behavior in (11). The factor γ encompasses effects such as channel length modulation and short channel effects which are not taken into account in the idealized square law current equations. By applying KCL at node Vb3 and taking partial derivatives, we are able to obtain an expression which contains both coefficients of ΔV_{DD} and ΔV_{th} .

$$\Delta V_{b3} = \Delta V_{DD} \left(\frac{A_3 - 2}{A_3} \right) + \Delta V_{th} \left(\frac{4 - 2A_3}{A_3} \right)$$

These coefficients are controllable by sizing the third stage and, along with proper sizing of the transistors of the fourth stage, we can optimize the design of the bias

circuit by picking the best value of γ which gives lowest variation min S21, but may not in fact exactly mirror (11).

D. Fourth Stage

The output of the fourth stage, Vout, is used to bias transistor M2 of the LNA. The analysis of this stage is similar to those of previous stages. For V out to be supply independent, the following relation is established between the sizes of the transistors:

$$\sqrt{k_5} = \frac{\sqrt{k_6}}{\alpha} \left(\frac{A_3 - 2}{A_3} \right)$$

We can now use (15) and (16) to set the value for γ . A also assists in establishing the nominal dc voltage at the output. The expression for γ , based on circuit parameters, is shown in (17).

$$\gamma = \alpha \left(\frac{3A_3 - 4}{A_3 - 2} \right) - 1$$

To solve above equation for γ and sizing of the fourth stage, values of α and A3 were iteratively picked in simulations. Results confirmed that, when α was set to 1, choosing A3 to 5 resulted in lowest variations in S21 of the LNA, while providing the desired nominal dc value at Vout.

V. SIMULATION RESULTS

We ran Monte Carlo simulations including effects from wafer level variation and local device mismatch at room temperature in the Cadence Spectre simulator. Realcomponents are used for all circuit elements in the LNA other than the inductors. The LNA designed operates at a center frequency of 4.6GHz. The baseline case, which has both input transistors M1 and M2 connected to a constant external bias, has a mean S21 magnitude of 1.85 with a standard deviation of 0.162 which gives it a variation of 8.75% about its mean value at room temperature. The compensated LNA, which has the dc value of M2 being provided by the bias circuit, has a mean S21 magnitude of 1.89 with a standard deviation of 0.024 giving it a variation of

1.27%. The bias circuit decreases the variation in S21 by 85%. Histograms for S21 of both the uncompensated and compensated LNA are shown in Fig. 4. Histograms of the magnitude of S21 of the LNA (a) without compensation and (b) with compensation. The supply voltage was swept and the gain recorded for both the uncompensated and compensated LNA. As shown in Fig. 5, S21 for the uncompensated LNA changes by 16% from its mean value. S21 for the compensated system changes only by 2.5%. To ensure that the compensation scheme would work under extreme conditions, process corner simulations were carried out over a temperature range of -500C to 1000C, as shown in Table I. For the uncompensated LNA, the worst case is the slow-slow corner at -500C, when the gain deviates from its mean value at room temperature by 55%. For the compensated LNA, under the same conditions, the maximum variation is 10%.

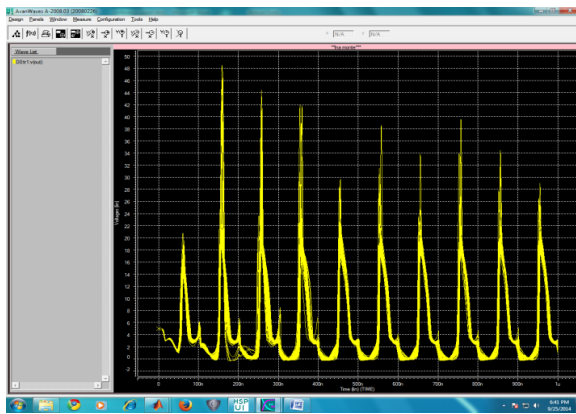
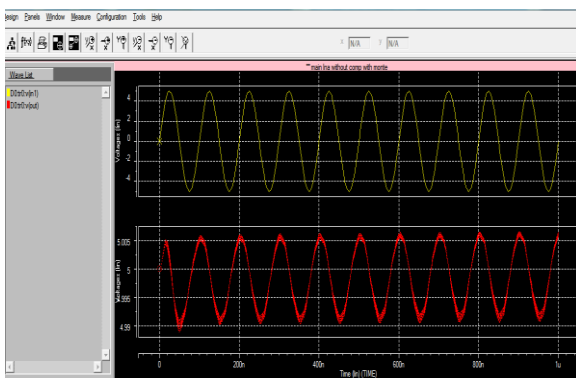


Fig4(a):simulation results for without compensation



Fig(b):simulation results for with compensation

The bias circuit has a power overhead of 1.3mW and requires additional area of 588 μm^2 . The standalone LNA consumes 3.3mW. This additional cost in power and area is not excessive, considering the large reduction in variability of S21.

VI. CONCLUSION

We have demonstrated a compensation scheme for low noise amplifiers in the 65nm process technology. Without any post fabrication trimming, the novel bias circuit scheme reduces variations in S21 due to manufacturing effects by 85%. The compensation scheme is robust under all process corners and a wide range of operating temperature. The technique can also very easily be ported to other RF amplifiers and significantly improve reliability with very little area and power overhead, translating to low cost and higher yield for RF systems.

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