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Multiple Fault Diagnosis of Analog Electronic Circuits

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Abstract:

The fault diagnosis of analog circuits has been a major field of interest in research for the past few decades. The analog fault diagnosis is important because of the growing usage of mixed mode analog/digital IC's. The fault diagnosis of Digital circuits is reasonably well established and the fault diagnosis of Analog circuits is still is a big challenge to researchers all over the world. In this paper, a fault diagnosis system for analog circuit testing based on Simulation Before Test (SBT) approach for multiple faults is proposed. Efficient algorithms to diagnose single and multiple faults are proposed in this paper.

Index Terms:

analog circuits, double faults, fault dictionary, fault signatures, integer coded fault dictionary, and multi frequency test.

I.INTRODUCTION:

With the help of computers, the analog electronic circuit fault diagnosis has gained wide spread attention in the area of atomized testing. Advances in System-on-Chip (SOC) innovation have brought about expanded significance of the simple hardware, along these lines moving it into the standard IC innovation. The increased complexity of the IC's is due to the advances made in deep sub micron technology and the co-existence of analog and digital circuits called mixed signal design. This has made testing an exceptionally difficult undertaking which must be done on little chips having complex usefulness. The fault diagnosis of analog circuits is far more complicated than the digital circuits. The main reasons are poor fault models, non linearity, measurement of voltages and currents at internal nodes which are sometimes not accessible and ambiguity in the measurements. The ambiguity results mainly because of the tolerances in the components. Because of all these reasons analog circuit fault diagnosis is relatively underdeveloped.

A fault can be defined as the change in the value of an element with respect to its nominal value which results in the failure of the whole circuit. The main classification of faults are Catastrophic faults (Hard Faults) and Parametric Deviation faults (soft faults). In hard faults the faulty element is either short or open. Soft faults or deviation faults are those faults where the element value changes or deviates from its nominal value without reaching the extreme bounds i.e. short or open. These deviation faults result mainly because of aging, manufacturing tolerances or parasitic effects. The most popular categorization of fault diagnosis techniques is based on the stage at which the testing process simulation is carried out. They are either Simulation Before Test (SBT) and Simulation After Test (SAT).Simulation Before Test method places emphasis on building Fault Dictionary or directory in which the nominal behaviour of the circuit in DC, time domain or frequency domain is stored. Also the responses of the circuit for various anticipated faults are stored. The anticipated faults are chosen based on experience of the field engineers.

The two important methods in SBT are:

i)Fault dictionary technique and
ii)Probabilistic theoretic approach

In Simulation After Test approach the simulation is carried out at the time of testing. This is done to identify the network parameters. Voltage and current measurements of the circuit are taken and these are then used to arrive at the component values. The faulty elements are then identified by determining those components which fall outside the design tolerance range. These methods are called as topological methods as they assume the knowledge of the circuit topology.

The 3 main methods of SAT are:

(1) Parameter identification technique
(2) Fault Verification Technique
(3) Optimization Technique

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The purpose of fault diagnosis is to determine the cause of failures in a manufactured, faulty chip. Most of the studies on failure analysis have assumed a single defect. But for the present technologies and chip sizes, this assumption may not be true. Multiple defects on a failing chip often reflect the reality. It is also possible that certain single location defects behave as multiple faults. It has been challenging for the researchers to develop practical models and inference algorithms for diagnosing multiple faults. It is more difficult to model and detect multiple faults particularly in presence of tolerance or measurement noise. Generally one faults effect on the circuit could be masked by the effects of other faults in multiple faults cases. So the research is still in progress for developing the multiple fault diagnosis techniques.In this paper the problem of multi frequency method in analog fault diagnosis is studied extensively. Fault dictionary method which belongs to the Simulation before test (SBT) approach is used in this thesis. Method to optimize the size of fault dictionary is presented. Method to optimize the test frequency set is also discussed. To reduce the fault dictionary size, a new approach which is based on the position of the component is developed.

II.FAULT DICTIONARY METHOD OF ANALOG FAULT DIAGNOSIS:

In recent years, application of different approaches to fault dictionary by taking different types of measurements has gained popularity. The widely used measurements are node voltage, magnitude and phase of node voltages, voltage/current measurements [1]. This chapter presents effective ways to construct fault dictionary for the analog circuits with catastrophic double faults. The fault dictionary is constructed with measurements read by using multi frequency method and also by single frequency method. The methods presented in this chapter are Integer coded fault dictionary for the analog circuits with double faults and the Second method is based on position of the component placed in the analog circuit.In analog circuit fault diagnosis using SBT approach, the measurements of the circuit are used in the construction of fault dictionary [12]. The fault dictionary is a table of readings of the test circuit under different fault conditions and one nominal condition i.e., fault free condition. The measurements of the circuit are made by introducing double faults into the circuit under test. To ensure that maximum numbers of faults are diagnosed, the measurements are made at different nodes and at different frequencies.

Due to the intrinsic properties of the analog circuits, sometimes the measurements made are either same or lie in a very close range. This makes the measurements practically difficult to distinguish. This ambiguity in the measurements results in the ambiguity sets.Usually the circuit under test may have many number of ambiguity sets and so in-order to distinguish them, integer codes were first proposed by Lin and Elcheirf. In this method, the measurements which lie in the same range are grouped and ambiguity sets are formed by giving the integer numbers to the groups. The fault dictionary can then be replaced by the integer coded fault dictionary. The integer codes provide the benefit of easy processing on the fault dictionary.

Integer code is based on the measurement readings and therefore the measurements of the CUT are to be first read. Steps to effectively construct integer coded fault dictionary are:

Step 1: Consider the analog circuit which has to be diagnosed and make the measurement of the circuit for initial (nominal) values of the components.

Step 2: Introduce hard faults into two components (double faults) of the CUT at a time and then the measurements of the circuit are read. This results in the faulty responses of the circuit.

Step 3: Repeat Step 1 and Step 2 for different frequencies at each node of the circuit under test to include maximum number of faults for diagnosis.

Step 4: Tabulate the nominal (fault-free) and the faulty responses of the circuit under test which were read at different frequencies.

Step 5: Determine the range as ± based on the measurements read. Now all those values which lie on the same range are given same integer number and ambiguity sets are thus formed.

Step 6: Using these integer codes, the fault dictionary table is replaced by the integer coded table which can also be called as ambiguity table.

This integer coded table can be effectively used to reduce the size of test frequency set in the multi frequency approach of analog fault diagnosis.

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To maximize the effectiveness of fault diagnosis the same procedure can be applied at different node measurements of the analog circuit under test. The test frequencies for the above process are selecting as follows: The transfer function of the CUT is calculated as a rational function of s. The coefficients of the function are expressed in terms of the circuit elements. Compute the corner frequencies of the CUT with its components having nominal values. Now choose the test frequencies such that there must be one frequency below the least corner frequency and one above the highest corner frequency and at least one value in between the corner frequencies.Illustration of Integer Coded Fault Dictionary Table: Consider a passive filter circuit shown in the figure

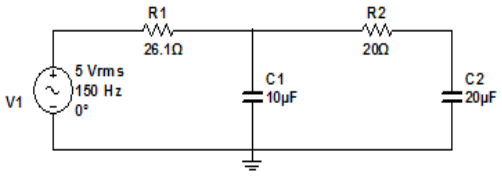

Fig. 1: Passive Filter

The transfer function H(S) of the circuit is given in the equation.

$$H(S) = \frac{R2}{(1+sR2C2)(R1+R2+sC1R1R2)-R1} \quad \ldots\ldots(1)$$

The nominal component values of the circuit are R1=26.1Ω, R2=20Ω, C1=10µF, C2=20µF. The corner frequencies of the CUT are 2500 Hz and 192.31 Hz. The test frequencies can therefore be FT= {150Hz, 192Hz, 500Hz, 1500Hz, 2000Hz 2500Hz, 3000Hz}. The illustration is done by considering only hard faults.

List Of Faults Considered		
S.No	Fault Type	Fault Name
1	Nominal	f_0
2	R1,R2 open	f_1
3	R1 open R2 short	f_2
4	R1 short R2 open	f_3
5	R1, R2 short	f_4
6	R1 C1 open	f_5
7	R1 open C1 short	f_6
8	R1 short C1 open	f_7
9	R1,C1 short	f_8
10	R1,C2 open	f_9
11	R1 open C2 short	f_{10}
12	R1 short C2 open	f_{11}
13	R1,C2 short	f_{12}
14	R2,C1 open	f_{13}
15	R2 open C1 short	f_{14}
16	R2 short C1 open	f_{15}
17	R2,C1 short	f_{16}
18	R2,C2 open	f_{17}
19	R2 open C2 short	f_{18}
20	R2 short C2 open	f_{19}
21	R2,C2 short	f_{20}
22	C1,C2 open	f_{21}
23	C1 open C2 short	f_{22}
24	C1 short C2 open	f_{23}
25	C1,C2 short	f_{24}

The fault dictionary table is constructed as follows by considering open circuit faults at 100MΩ, short circuit faults at 100Ω:

Fault Dictionary With Measurements Read By Multi-Frequency Approach												
Frequencies	Faults (mV)											
	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}
F1=150Hz	3.8	3.8	3.9	4.1	4.1	3.8	2.5	4.1	2.8	3.8	3.4	4.1
F2=192Hz	3.5	3.5	3.5	3.8	3.8	3.5	2.3	3.8	2.7	3.5	3.2	3.8
F3=500Hz	2.7	2.7	2.7	2.9	2.8	2.7	2.2	2.9	2.3	2.7	2.7	2.9
F4=1000Hz	3.1	3.2	3.0	3.2	3.0	3.2	2.8	3.2	2.8	3.2	3.2	3.2
F5=1500Hz	3.7	3.7	3.5	3.7	3.4	3.7	3.4	3.7	3.4	3.7	3.7	3.7
F6=2000Hz	4.1	4.1	3.9	4.0	3.8	4.1	3.9	4.0	3.8	4.1	4.1	4.0
F7=2500Hz	4.3	4.3	4.2	4.3	4.1	4.3	4.2	4.3	4.1	4.3	4.3	4.3
F8=3000Hz	4.5	4.5	4.4	4.4	4.3	4.5	4.4	4.4	4.3	4.5	4.5	4.4

Fault Dictionary With Measurements Read By Multi-Frequency Approach (Continuation$_{o_1}$)													
Frequencies	Faults (mV)												
	f_{12}	f_{13}	f_{14}	f_{15}	f_{16}	f_{17}	f_{18}	f_{19}	f_{20}	f_{21}	f_{22}	f_{23}	f_{24}
F1=150Hz	3.8	3.8	2.5	3.9	2.5	3.8	3.4	3.9	3.3	3.8	3.4	2.5	2.2
F2=192Hz	3.6	3.5	2.3	3.5	2.4	3.4	3.2	3.5	3.2	3.5	3.2	2.3	2.2
F3=500Hz	3.0	2.7	2.2	2.7	2.3	2.7	2.8	2.7	2.7	2.7	2.7	2.2	2.2
F4=1000Hz	3.3	3.2	2.8	3.0	2.8	3.2	3.2	3.0	3.0	3.2	3.2	2.9	2.9
F5=1500Hz	3.7	3.7	3.4	3.5	3.3	3.7	3.7	3.5	3.5	3.7	3.7	3.4	3.5
F6=2000Hz	4.0	4.1	3.9	3.9	3.8	4.1	4.1	3.9	3.9	4.1	4.1	3.9	3.9
F7=2500Hz	4.3	4.3	4.2	4.2	4.0	4.3	4.3	4.2	4.2	4.3	4.3	4.2	4.2
F8=3000Hz	4.4	4.5	4.4	4.4	4.3	4.5	4.5	4.4	4.4	4.5	45	4.4	4.4

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Now the above fault dictionary table is replaced by the following integer coded fault dictionary table:

Integer Coded Fault Dictionary with ±0.1 range

Frequencies	Faults											
	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}
F1=150Hz	6	6	5	6	5	6	4	6	4	6	2	6
F2=192Hz	7	7	6	7	6	7	5	7	5	7	3	7
F3=500Hz	4	4	3	5	4	4	2	5	3	4	2	5
F4=1000Hz	2	2	1	3	3	2	1	3	3	2	1	3
F5=1500Hz	2	2	2	3	3	2	1	3	3	2	2	3
F6=2000Hz	1	1	1	2	2	1	1	2	2	1	1	2
F7=2500Hz	1	1	1	2	2	1	1	2	2	1	1	2
F8=3000Hz	1	1	1	2	2	1	1	2	2	1	1	2

Integer Coded Fault Dictionary with ±0.1 range (Continuation..)

Frequencies	Faults												
	f_{12}	f_{13}	f_{14}	f_{15}	f_{16}	f_{17}	f_{18}	f_{19}	f_{20}	f_{21}	f_{22}	f_{23}	f_{24}
F1=150Hz	2	6	4	5	3	6	2	5	2	6	2	4	1
F2=192Hz	2	7	5	6	4	7	3	6	2	7	3	5	1
F3=500Hz	3	4	2	3	1	4	2	3	1	4	2	2	2
F4=1000Hz	3	2	1	1	1	2	1	1	1	2	1	1	1
F5=1500Hz	3	4	1	2	1	2	2	2	1	2	1	1	1
F6=2000Hz	2	2	1	1	1	1	1	1	1	1	1	1	1
F7=2500Hz	2	2	1	1	1	1	1	1	1	1	1	1	1
F8=3000Hz	2	2	1	1	1	1	1	1	1	1	1	1	1

Therefore the above integer coded fault dictionary method can be used to reduce the test frequency set in multi-frequency method of analog fault diagnosis. The advantage of this integer coded fault dictionary is that the data of the table can be easily processed for further diagnosis. The other method of reduction of size of fault dictionary is based on the positions in the circuit. This method has been developed to reduce the size of fault dictionary. The hard faults are first introduced into the CUT based on simulation before test approach [9]. The measurements of the CUT are tabulated in the fault dictionary. These measurements are then arranged according to the position of the faulty components. A check must be made on the faulty responses. All those fault signatures which have the same value with respect to same position can be eliminated from the fault dictionary. This method helps in easily reducing the size of fault dictionary of circuits which contain large number of components.Illustrations: Example Circuit 1: Consider the circuit as shown in figure with the nominal component values R1=26.1Ω, R2=20Ω, C1=10μF, C2=20μF.

The fault free response is first measured and then the hard faults are introduced into the circuit. The responses of the CUT for the introduced faults are tabulated.

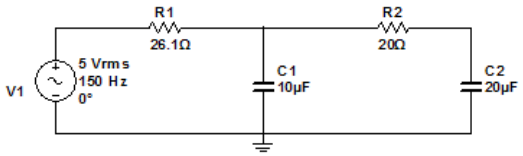

Fig. 2: Example circuit 1

List Of Faults Considered

S.No	Fault Type	Fault Name
1	Nominal	f_0
2	R1,R2 open	f_1
3	R1 open R2 short	f_2
4	R1 short R2 open	f_3
5	R1, R2 short	f_4
6	R1 C1 open	f_5
7	R1 open C1 short	f_6
8	R1 short C1 open	f_7
9	R1,C1 short	f_8
10	R1,C2 open	f_9
11	R1 open C2 short	f_{10}
12	R1 short C2 open	f_{11}
13	R1,C2 short	f_{12}
14	R2,C1 open	f_{13}
15	R2 open C1 short	f_{14}
16	R2 short C1 open	f_{15}
17	R2,C1 short	f_{16}
18	R2,C2 open	f_{17}
19	R2 open C2 short	f_{18}
20	R2 short C2 open	f_{19}
21	R2,C2 short	f_{20}
22	C1,C2 open	f_{21}
23	C1 open C2 short	f_{22}
24	C1 short C2 open	f_{23}
25	C1,C2 short	f_{24}

The fault dictionary table is constructed as follows by considering open circuit and short circuit faults:

Fault Dictionary of Example Circuit 1

Faults	Circuit Measurements
f_0	7.198mV
f_1	4.98 mV
f_2	260.709 μV
f_3	60.96 nV
f_4	54.69 μV
f_5	4.98 mV
f_6	20.971μV
f_7	3.249 V
f_8	1.291 V
f_9	4.98 mV
f_{10}	61.682 μV
f_{11}	41.942 μV
f_{12}	811.2 pV
f_{13}	9.96 mV
f_{14}	41.942 μV
f_{15}	50.251 μV
f_{16}	41.941 μV
f_{17}	0 V
f_{18}	249.557 μV
f_{19}	37.627 μV
f_{20}	5 V

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f_{21}	4.98 mV
f_{22}	60.136 µV
f_{23}	41.942 µV
f_{24}	41.942 µV

The above fault signatures are now grouped based on position of the components. The place of the very first component in the circuit is given position 1 and the next components from left to right are given positions sequentially.

Faults associated with the component placed in position 1		
Fault Name	Fault Type	Fault Signature Value
f_5	R1, C1 open	4.98 mV
f_1	R1, R2 open	4.98 mV
f_9	R1, C2 open	4.98 mV
f_6	R1 open, C1 short	20.971 µV
f_2	R1 open, R2 short	260.709 µV
f_{10}	R1 open, C2 short	61.682 µV
f_7	R1 short, C1 open	3.249 V
f_3	R1 short, R2 open	60.96 nV
f_{11}	R1 short, C2 open	41.942 µV
f_8	R1, C1 short	1.291 V
f_4	R1, R2 short	54.69 µV
f_{12}	R1, C2 short	811.2 pV

Faults associated with the component placed in position 2		
Fault Name	Fault Type	Fault Signature Value
f_{13}	R2, C1 open	9.96 mV
f_{17}	R2, C2 open	0 V
f_{14}	R2 open, C1 short	41.942 µV
f_{18}	R2 open, C2 short	249.557 µV
f_{15}	R2 short, C1 open	50.251 µV
f_{19}	R2 short, C2 open	37.627 µV
f_{16}	R2, C1 short	41.941 µV
f_{20}	R2, C2 short	5 V

Faults associated with the component placed in position 3		
Fault Name	Fault Type	Fault Signature Value
f_{21}	C1, C2 open	4.98 mV
f_{22}	C1 open, C2 short	60.136 µV
f_{23}	C1 short, C2 open	41.942 µV
f_{24}	C1, C2 short	41.942 µV

The above re-arrangement helps in easily identifying the same fault signatures. The fault signatures f1, f5 and f9 can be grouped into one set and thus two signatures can be reduced from fault dictionary.Example Circuit 2: Consider the circuit as shown in figure with the nominal component values R1=26.1Ω, R2=20Ω, R3=15Ω, C1=10µF, C2=20µF, C3=30µF.

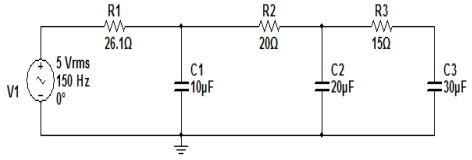

Fig. 3: Example circuit 2

List Of Faults Considered		
S.No	Fault Type	Fault Name
1	Nominal	f_0
2	R1,C1 open	f_1
3	R1 open C1 short	f_2
4	R1 short C1 open	f_3
5	R1, C1 short	f_4
6	R1 C2 open,	f_5
7	R1 open C2 short	f_6
8	R1 short C2 open	f_7
9	R1,C2 short	f_8
10	R1,C3 open	f_9
11	R1 open C3 short	f_{10}
12	R1 short C3 open	f_{11}
13	R1,C3 short	f_{12}
14	R1,R2 open	f_{13}
15	R1 open R2 short	f_{14}
16	R1 short R2 open	f_{15}
17	R1,R2 short	f_{16}
18	R1,R3 open	f_{17}
19	R1 open R3 short	f_{18}
20	R1 short R3 open	f_{19}
21	R1,R3 short	f_{20}
22	R2,C1 open	f_{21}
23	R2 open C1 short	f_{22}
24	R2 short C1 open	f_{23}
25	R2,C1 short	f_{24}
26	R2,C2 open	f_{25}
27	R2 open C2 short	f_{26}
28	R2 short C2 open	f_{27}
29	R2, C2 short	f_{28}
30	R2 C3 open	f_{29}
31	R2 open C3 short	f_{30}
32	R2 short C3 open	f_{31}
33	R2,C3 short	f_{32}
34	R2,R3 open	f_{33}
35	R2 open R3 short	f_{34}
36	R2 short R3 open	f_{35}
37	R2,R3 short	f_{36}
38	R3,C1 open	f_{37}
39	R3 open C1 short	f_{38}
40	R3 short C1 open	f_{39}
41	R3,C1 short	f_{40}
42	R3,C2 open	f_{41}
43	R3 open C2 short	f_{42}
44	R3 short C2 open	f_{43}
45	R3,C2 short	f_{44}
46	R3,C3 open	f_{45}
47	R2 open C3 short	f_{46}
48	R3 short C3 open	f_{47}
49	R3,C3 short	f_{48}
50	C1,C2 open	f_{49}
51	C1 open C2 short	f_{50}
52	C1 short C2 open	f_{51}
53	C1, C2 short	f_{52}
54	C1 C3 open	f_{53}
55	C1 open C3 short	f_{54}
56	C1 short C3 open	f_{55}
57	C1,C3 short	f_{56}
58	C2,C3 open	f_{57}
59	C2 open C3 short	f_{58}
60	C2 short C3 open	f_{59}
61	C2,C3 short	f_{60}

The fault dictionary table is constructed as follows by considering open circuit and short circuit faults:

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Fault Dictionary Of Example Circuit 2	
Faults	Circuit Measurements
f_0	8.289 mV
f_1	4.975 mV
f_2	41.943 µV
f_3	5.397 V
f_4	528.306 mV
f_5	4.974 mV
f_6	31.773 µV
f_7	4.489 V
f_8	7.3 V
f_9	4.975 mV
f_{10}	25.78 µV
f_{11}	3.249 V
f_{12}	398.126 mV
f_{13}	4.975 mV
f_{14}	59.818 µV
f_{15}	101.1 nV
f_{16}	4.03 V
f_{17}	4.975 mV
f_{18}	206.695 µV
f_{19}	3.949 V
f_{20}	2.373 V
f_{21}	9.95 mV
f_{22}	41.943 µV
f_{23}	1.237 V
f_{24}	41.941 µV
f_{25}	8.288 mV
f_{26}	51.561 µV
f_{27}	1.497 V
f_{28}	41.942 µV
f_{29}	8.288 mV
f_{30}	249.558 µV
f_{31}	75.57 µV
f_{32}	520.797 mV
f_{33}	8.288 mV
f_{34}	43.645 µV
f_{35}	1.834 V
f_{36}	32.687 µV
f_{37}	8.293 mV
f_{38}	20.971 µV
f_{39}	296.398 µV
f_{40}	41.941 µV
f_{41}	11.913 mV
f_{42}	85.792 µV
f_{43}	254.188 µV
f_{44}	21.767 µV
f_{45}	0 V
f_{46}	375.818 µV
f_{47}	1.514 mV
f_{48}	71.136 µV
f_{49}	8.956 mV
f_{50}	60.138 µV
f_{51}	41.941 µV
f_{52}	5 V
f_{53}	6.94 mV
f_{54}	78.488 µV
f_{55}	20.971 µV
f_{56}	20.971 µV
f_{57}	4.975 mV
f_{58}	59.037 µV
f_{59}	87.792 µV
f_{60}	182.277 µV

The above fault signatures are now grouped based on position of the components.

Faults associated with the component placed in position 1		
Fault Name	Fault Type	Fault Signature Value
f_{13}	R1, R2 open	4.975 mV
f_1	R1, C1 open	4.975 mV
f_{17}	R1, R3 open	4.975 mV
f_5	R1, C2 open	4.975 mV
f_9	R1, C3 open	4.975 mV
f_{14}	R1 open, R2 short	59.818 µV
f_2	R1 open, C1 short	41.943 µV
f_{18}	R1 open, R3 short	207.695 µV
f_6	R1 open, C2 short	31.773 µV
f_{10}	R1 open, C3 short	25.98 µV
f_{15}	R1 short, R2 open	101.1nV
f_3	R1 short, C1 open	5.397 V
f_{19}	R1 short, R3 open	3.949 V
f_7	R1 short, C2 open	4.489 V
f_{11}	R1 short, C3 open	3.249 V
f_{16}	R1, R2 short	4.03 V
f_4	R1, C1 short	528.30 mV
f_{20}	R1, R3 short	2.373 V
f_8	R1, C2 short	7.3 V
f_{12}	R1, C3 short	398.126 m

Faults associated with the component placed in position 2		
Fault Name	Fault Type	Fault Signature Value
f_{21}	R2, C1 open	9.95 mV
f_{25}	R2, C2 open	8.288 mV
f_{33}	R2, R3 open	8.288 mV
f_{29}	R2, C3 open	8.288 mV
f_{22}	R2 open, C1 short	41.943 µV
f_{26}	R2 open, C2 short	51.561 µV
f_{34}	R2 open, R3 short	43.645 µV
f_{30}	R2 open, C3 short	249.558 µV
f_{23}	R2 short, C1 open	1.237 V
f_{27}	R2 short, C2 open	1.497 V
f_{35}	R2 short, R3 open	1.834 V
f_{31}	R2 short, C3 open	75.57 µV
f_{24}	R2, C1 short	41.941 µV
f_{28}	R2, C2 short	41.942 µV
f_{36}	R2, R3 short	32.687 µV
f_{32}	R2, C3 short	520.797 mV

Faults associated with the component placed in position 3		
Fault Name	Fault Type	Fault Signature Value
f_{37}	R3, C1 open	8.293 mV
f_{41}	R3, C2 open	11.913 mV
f_{45}	R3, C3 open	0 V
f_{38}	R3 open, C1 short	20.971 µV
f_{42}	R3 open, C2 short	85.792 µV
f_{46}	R3 open, C3 short	375.818 µV
f_{39}	R3 short, C1 open	296.398 µV
f_{43}	R3 short, C1 open	254.188 µV
f_{47}	R3 short, C1 open	1.514 mV
f_{40}	R3, C1 short	41.941 µV
f_{44}	R3, C2 short	21.767 µV
f_{48}	R3, C3 short	71.136 µV

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Faults associated with the component placed in position 4		
Fault Name	Fault Type	Fault Signature Value
f_{49}	C1, C2 open	8.956 mV
f_{53}	C1, C3 open	6.94 mV
f_{50}	C1 open, C2 short	60.138 µV
f_{54}	C1 open, C3 short	78.488 µV
f_{51}	C1 short, C2 open	41.941 µV
f_{55}	C1 short, C3 open	20.971 µV
f_{52}	C1, C2 short	5 V
f_{56}	C1, C3 short	20.971 µV

Faults associated with the component placed in position 5		
Fault Name	Fault Type	Fault Signature Value
f_{57}	C2, C3 open	4.975 mV
f_{58}	C2 open, C3 short	59.037 µV
f_{59}	C2 short, C3 open	87.792 µV
f_{60}	C2, C3 short	182.277 µV

The fault signatures f1, f5, f9, f13, f17 can be grouped into one set and thus four signatures can be reduced from fault dictionary. From the above two illustrations it is clear that upto 25% of the fault signatures can be reduced with respect to position 1. It is also observable that if the component placed in position 1 has open circuit fault and if the other component of the circuit is also open circuit fault component then they are resulting in the same fault signature. Further work on this concept may provide a way to reduce the more number of fault signatures.

III.OPTIMIZATION OF TEST FREQUENCY SET:

This section presents application of test frequency set reduction method to analog circuits consisting of double faults. There exist many methods to eliminate the redundant frequencies present in the multi frequency method of analog fault diagnosis [7], [11]. This multi frequency method of analog fault diagnosis is widely used because of its simplicity. This method includes analyzing the behavior of the circuit under test at different frequencies. The criteria for selection of these test frequencies are already mentioned in the previous section. Integer coded fault dictionary method described in the previous section is useful for the reduction of test frequency set.

Step 1: Obtain the test frequency set by following the procedure mentioned in section II.

Step 2: Obtain the responses of the circuit under test for all those frequencies by considering nominal component values as well as the faulty component values of the CUT.

Step 3: Construct a fault dictionary which includes measurements read from CUT at different frequencies.

Step 4: Replace this false dictionary table with integer coded fault dictionary table.

Step 5: From this integer coded fault dictionary table identify the number of singletons and number of ambiguity sets for each frequency.

Step 6: Choose the row which has highest number of ambiguity sets and intersect it with the row having next highest number of ambiguity sets. Eliminate the intersected ambiguity sets. If there is no intersections in the ambiguity sets then go to next step.

Step 7: Construct the sub-ambiguity table with the remaining singletons and ambiguity sets and now eliminate the frequency with highest number of ambiguity sets if there is no repetition found.

Step 8: Finally when there are no repetitions found when intersected stop. Otherwise repeat the above process.

A valid set of test frequencies is thus obtained. A test frequency set is said to be valid if it isolates all desired faults. This reduction helps in carrying out the further diagnosis process within less time.

IV.SIMULATION TOOL:

The measurements of the analog electronic ciruits mentioned in this thesis are obtained by simulating the CUT in Multisim software. It is the most popular electronic design and education software from Electronics Workbench. Multisim is the schematic capture and simulation application of National Instruments Circuit Design Suite, a suite of EDA (Electronics Design Automation) tools that assists in carrying out the major steps in the circuit design flow. Multisim is designed for schematic entry, simulation, and feeding to downstage steps, such as PCB layout. It offers graphical interface for design and analysis needs. Multisim software is available in three editions for educational community namely Education edition, Lab edition and Student edition. Education edition is used for creation of demonstrations, examples, assignments or tests. Lab edition is usually used by students in laboratory environment. Student edition is also used by students but for home study purpose.

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V.CONCLUSION AND SCOPE:

In this thesis Fault Dictionary method of Simulation before Test approach for analog fault diagnosis has been discussed. The following work carried out in this thesis is as follows:

•Using the multi frequency method and also single frequency method, the fault dictionary table for double faults of analog electronic circuit is constructed.

•Methods to reduce the size of fault dictionary is discussed and illustrated.

•Integer coded fault dictionary technique is applied for CUT with double faults.

•Reduction in the test frequency set is discussed.

The methods presented in this thesis to reduce the size of fault dictionary are applied to the CUT with double faults. Further work in this area requires developing more efficient methods which will be applicable to analog circuits with more than two faulty components.

Although these methods give good results to circuits with any number of components, time required to process the data of fault dictionary increases with increase in number of components. Therefore the advancements can be made in this area to reduce the timing parameter.

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