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Simulation of Cascade Switched-Diode Multilevel Converter Fed Induction Motor Drive with Minimum Number of Power Electronic Components

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Abstract
This paper presents two types of multilevel inverters, known as symmetrical and asymmetrical multilevel inverter. Both types are very effective and efficient for improving the quality of the inverter output voltage. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given.This multilevel converter requires only 50% of the number of DC sources required in conventional seven and fifteen-level cascaded Switched-Diode Multilevel converters. In addition, the three-phase output voltages of this converter can be easily balanced because they are synthesized by using the same DC sources. An active harmonic elimination method is applied to eliminate any number of specific higher order harmonics of multilevel converters with unequal dc voltages. The simulation of three phase nine level inverter fed induction motor model is done using Simulink.

Keywords: Induction motor, multilevel converter, Asymmetric, bidirectional switch, cascade, fullbridge converter.

I. INTRODUCTION
Multilevel inverter has become more famous overprevious years in high power electric applicationswithout the usage of a transformer and filters [1]. Multilevelinverters can be categorized into three topologies, they are,diode-clamped, flying-capacitor and cascaded H-bridge cell.The idea of cascaded multilevel inverter is based on linking H-bridgeinverters in series to attain an output of sinusoidalvoltage. The output voltage is the sum of the voltage that isproduced by each cell. As the number of levels gets increases,the synthesized output waveform has several steps whichgenerate a staircase wave that approaches a preferredwaveform [2].

The cascaded multilevelinverters have received special attention due to themodularity and simplicity of control. The cascadedmultilevel inverters are mainly classified into twogroups:1) symmetric, with equal magnitude for the dcvoltage sources; and 2) asymmetric, with differentvalues of the dc voltage sources. By increasing themagnitude of dc voltage sources, the higher numberof output levels will be generated. Therefore, theasymmetric cascaded multilevel inverters increase thenumber of output levels by using powersemiconductor devices that are the same as thesymmetric ones [3], [4], [5]–[9]. Up to now,different topologies with several algorithms todetermine the magnitude of their dc voltage sourceshave been presented in the literatures. In [10], the H-bridgecascaded multilevel inverter with two differentalgorithms as symmetric and asymmetric invertershas been presented. Two other symmetric cascadedmultilevel inverters have been also presented in [11]and [12]. The main advantage of these inverters is thelow number of different voltage amplitudes of theused dc sources. However, the higher number ofrequired insulated gate bipolar transistor

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(IGBTs),power diodes, and driver circuits in generating aspecific output level are their remarkabledisadvantages. In order to increase the number ofoutput levels with a lower number of powersemiconductor devices, different asymmetriccascaded multilevel inverters have been presented.The bidirectional power switches havebeen used in these topologies. Each bidirectionalpower switch includes two IGBTs, two power diodes,and one driver circuit if the common emitterconfiguration is used.

Power electronic inverters are becoming popular forvarious industrial drives applications. In recent years,inverters have even become a necessity for manyimplementations such as motor controlling and powersystems [13], [14]. The concept of utilizing multiple smallvoltage levels to perform power conversion was patented byan MIT researcher over twenty years ago[15]. The multi-levelinverter system is very promising in AC drives, when bothreduced harmonic contents and high power are required[16], [17]. Multilevel inverters have been mainly used inmedium or high power system applications, such as staticreactive power compensation and adjustable-speed drives[18], [19]. A multilevel inverter not only achieves high powerratings, but also enables the use of renewable energy sources.

II. BASIC OF PROPOSED MULTILEVEL CONVERTER TOPOLOGIES

Fig.1.shows the basic topology for proposed switched-diode multilevel converter. In this circuit, when the switch S is turned off, the current flows from the diode *D* and load voltage will be *E*. But, when the switch *S* is turned on, the diode is reverse biased and current flows from the voltage source *E* and load voltage will be (2*E*). By the use of this method, the load voltage is controlled. This method is the basic of proposed multilevel converter. The new presented structures in three different topologies are introduced and consist of: 1) symmetric switched-diode multilevel converter; 2) asymmetric switched diode multilevel converter; and 3) cascade switched-diode multilevel converter.

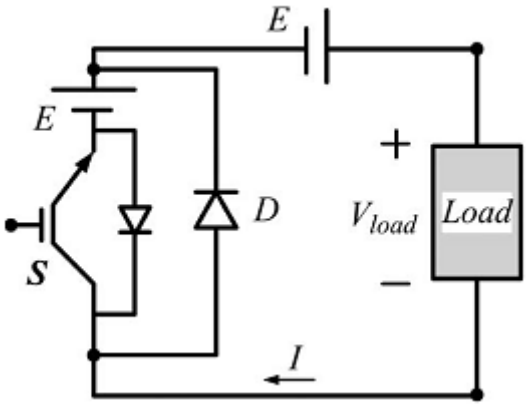

Fig.1.Basic circuit of proposed switched-diode multilevel converter.

III. PROPOSED SYMMETRICAL SWITCHEDDIODE MULTILEVEL CONVERTER

The structure of proposed symmetric switched-diode multi level converter is shown in Fig. 2. In this structure, the values of the dc voltage sources are equal. Therefore, this topology is called symmetric switched diode multilevel converter. Table I gives the values of output voltages (*Eo*) for different states of switches. In this topology, the basic unit generates a staircase voltage waveform (*Eo*) with positive polarity (*E*, 2E, 3E . . .). It is connected to a fullbridge converter, which particularly alternates the input voltage polarity and generates positive or negative staircase waveform (*Eo*) at the output voltage (0, ±*E*, ±2*E*, ±3*E*, ...).

The number of output levels (*Nlevel*), IGBTs (*NIGBT*), and the maximum output voltage (*Eo*,max) in the proposed symmetric converter are obtained as follows, respectively:

$$N_{level} = 2K + 1 \quad (1)$$

$$N_{IGBT} = K + 3 \quad (2)$$

$$E_{o,\max} = KE \quad (3)$$

Where K represents the number of dc voltage sources. Fig.3. compares the number of IGBTs versus the

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number of output levels (*Nlevel*) in the proposed symmetric switched-diode topology and the symmetric conventional cascade topology. This figure shows that the proposed converter requires the least number of IGBTs.

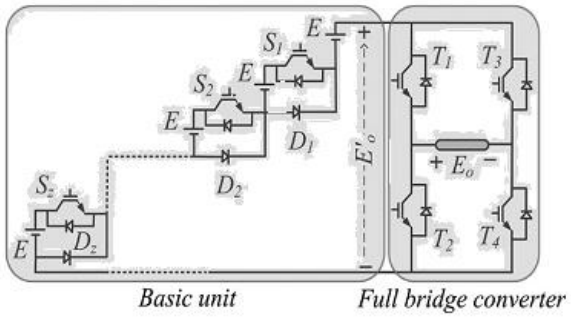

Fig.2. Proposed symmetric switched-diode multilevel converter topology.

IV. PROPOSED ASYMMETRICAL SWITCHED-DIODE MULTILEVEL CONVERTER

Asymmetrical multilevel converter provides an increased number of output voltage levels for the same number of power electronic devices than its symmetric counterpart. For dc voltage sources of conventional cascade H-bridge topology, two main methods have been suggested, which have been called binary and trinary configuration. The trinary configuration can produce a great number of levels in comparison with binary configuration. Fig. 3. shows the proposed topology for asymmetrical switched-diode converter, which consists of one basic unit and a full-bridge converter.

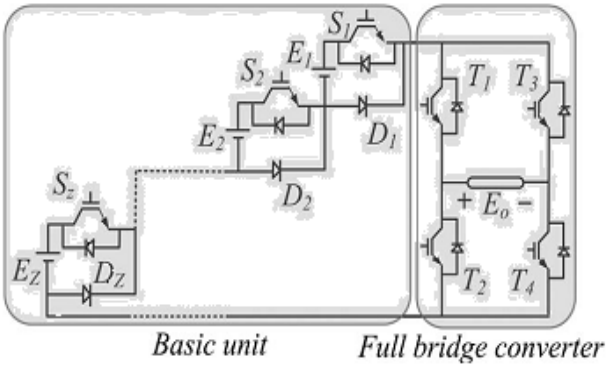

Fig.3. Proposed asymmetrical switched-diode multilevel converter topology.

Table I shows the ON switches look-up table for proposed asymmetric topology. In this topology, the values of dc sources are suggested to be chosen according to the following algorithm:

$$E_1 = E \quad (4)$$

$$E_j = 2^{(j-1)}E \qquad \text{For j} = 2, 3, 4, \ldots, \text{Z}. \quad (5)$$

TABLE I
SWITCH STATES FOR ASYMMETRICAL TOPOLOGY

state	Switches states									Output voltage
	S_1	S_2	....	S_{z-1}	S_z	T_1	T_2	T_3	T_4	
1	0	0	....	0	0	1	0	1	0	0
2	1	0	....	0	0	1	0	0	1	E_1
3	1	0	....	0	0	0	1	1	0	$-E_1$
4	0	1	....	0	0	1	0	0	1	E_2
5	0	1	....	0	0	0	1	1	0	$-E_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2Z	0	0	....	1	1	1	0	0	1	E_z
2Z+1	0	0	....	1	1	0	1	1	0	$-E_z$
2Z+2	1	1	.....	0	0	1	0	0	1	(E_1+E_2)
2Z+3	1	1	....	0	0	0	1	1	0	$-(E_1+E_2)$
⋮	⋮	⋮	....	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2^{(Z+1)}$-2	1	1	....	1	1	1	0	0	1	$(E_1+E_2+...+E_z)$
$2^{(Z+1)}$-1	1	1	....	1	1	0	1	1	0	$-(E_1+E_2+...+E_z)$

For this method, the number of levels and maximum output voltage are given by (6) and (7), respectively

$$N_{level} = 2^{(Z+1)} - 1 \quad (6)$$

$$E_{o,\max} = (2Z-1)E \quad (7)$$

Where Z represents the number of dc sources. In the proposed asymmetric topology, the number of IGBTs is obtained by

$$N_{IGBT} = Z + 4 \quad (8)$$

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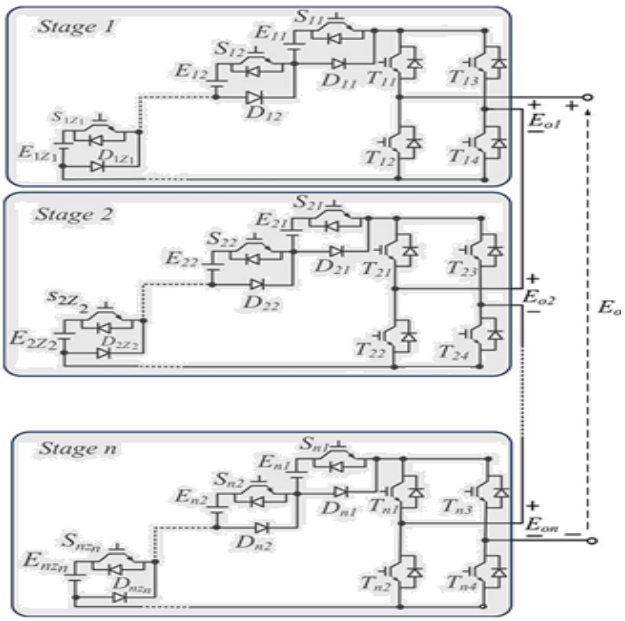

Fig.3.Proposed cascade switched-diode multilevel converter topology.

V. PROPOSED CASCADE SWITCHED-DIODE MULTILEVEL CONVERTER

To provide a large number of levels with less number of components, cascade switched-diode multilevel converters can be used. Fig.3.shows the structure of proposed cascade multilevel converter. The output voltage of the proposed cascade switched diode multilevel converter is given by

$$E_{out} = E_{o_1} + E_{o_2} + \cdots + E_{o_n} \quad (9)$$

For the proposed cascade topology, two methods for determination of values of the dc sources are presented.

A. First Algorithm

In this algorithm, the values of all of the dc voltage sources in each stage are the same. For stage 1,

$$E_{1i} = E_1 \qquad i = 1, 2, 3, \ldots, Z_1 \quad (10)$$

Therefore, the maximum output voltage of this stage ($E_{o1,\max}$) will be

$$E_{o_{1,\max}} = Z_1 \times E_1 \quad (11)$$

For stage 2,

$$E_{2i} = E_2 = E_1 + \left(2 \times E_{o_{1,\max}}\right) = (2Z_1 + 1) \times E_1 \; i = 1, 2, \ldots, Z_2 \quad (12)$$

In this stage, the maximum output voltage ($Eo2$, max) will be

$$E_{o_{2,\max}} = Z_2 \times E_2 \quad (13)$$

For stage 3,

$$E_{3i} = E_3 = E_1 + (2 \times E_{o_{2,\max}}) + (2 \times E_{o_{1,\max}}) = (2Z_1 + 1) \times (2Z_2 + 1) \times E_1 \; i = 1, 2, 3, \ldots, Z_3 \quad (14)$$

For the jth stage,

$$E_{ji} = E_j = (2Z_1 + 1) \times (2Z_2 + 1) \times \cdots \times (2Z_{j-1} + 1) \times E_1 \quad (15)$$

In this method, the number of output voltage levels ($Nlevel,F$) can be determined by the following equation:

$$N_{level,F} = N_{level,stage1} \times N_{level,stage.2} \times \cdots \times N_{level,stage.n} = (2Z_1 + 1) \times (2Z_2 + 1) \times \cdots \times (2Z_n + 1) \quad (16)$$

In this method, the maximum output voltage ($E_{omax,F}$) is

$$E_{o_{\max,F}} = \sum_{i=1}^{n} Z_i \times E_{i1} \quad (17)$$

B. Second Algorithm

In this structure for the jth stage, the dc voltage source magnitudes are given by (18) and (19)

$$E_{j1} = \left(2^{(Z_1+1)} - 1\right) \times \left(2^{(Z_2+1)} - 1\right) \times \cdots \times \left(2^{(Z_{j-1}+1)} - 1\right) \times E \quad (18)$$

$$E_{ji} = 2^{(i-1)} E_{j1} \quad i = 2, 3, \ldots, Z_j \quad (19)$$

In this method, the maximum output voltages of converter ($E_{omax,S}$) and the number of output voltage levels (N_{level},S) can be calculated as follows, respectively:

$$E_{o_{\max,S}} = \sum_{i=1}^{n} [(2^{Z_i+1} - 1)] \times E_{i1} \quad (20)$$

$$N_{level,S} = N_{level,stage.1} \times N_{level,stage.2} \times \cdots \times N_{level,stage.n} = (2^{Z_1+1} - 1) \times (2^{Z_2+1} - 1) \times \cdots \times (2^{Z_n+1} - 1). \quad (21)$$

The number of IGBTs in the proposed cascade topology is

$$N_{IGBT} = (Z_1 + Z_2 + Z_3 + \cdots + Z_n) + 4n \quad (22)$$

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C. Seven-Level Symmetric Switched-Diode Converter

Fig. 4.shows a seven-level symmetric switched-diode converter structure. In this topology, the values of dc sources areequal and for each one of them 35 V has been used. Hence,the maximum output voltage is 105 V. In this topology, threedc sources and six IGBTs has been used. For the same number of levels, the symmetric CHB topology needs three dc sourcesand 12 IGBTs, which the number of IGBTs is higher than thatof recommended symmetric structure.Based on this figure andthe value of THD for current, it is clear that the load currentis almost sinusoidal because the R-L load of the symmetricswitched-diode converter (R-L) behaves as a low-pass filter forthe current.

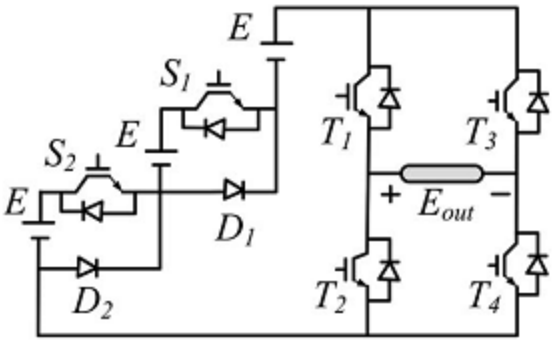

Fig .4. Seven-level symmetric converter.

D. Fifteen-Level Asymmetric Switched-Diode Converter

In this section, the simulation results fora 15-level asymmetric switched-diode converter are explained.Fig.5.shows the structure of proposed 15-level converter.

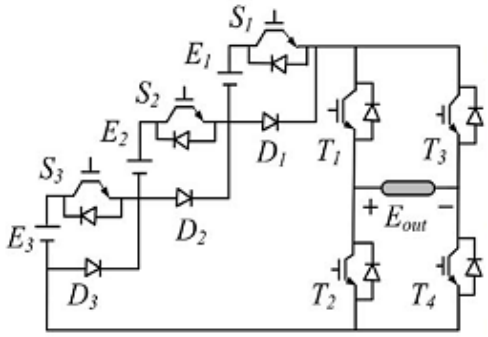

Fig. 5.Fifteen-level asymmetric converter.

VI.INDUCTION MOTOR

Induction Motor (1M) An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

VII.MATLAB/SIMULINK RESULTS

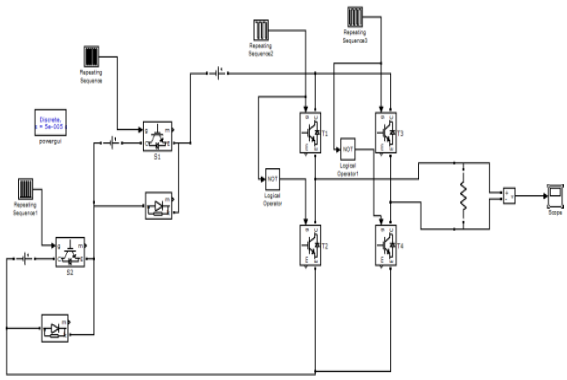

Fig.6. Simulink model of the seven Level inverter with reduced switches.

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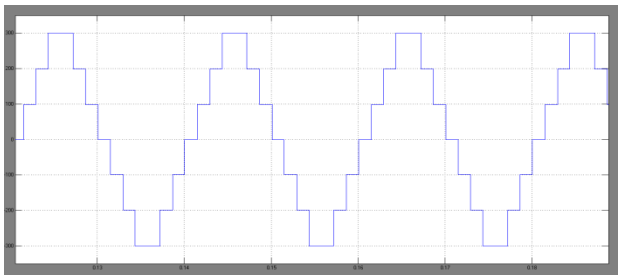

Fig.7. Simulated output voltage of the seven level inverter.

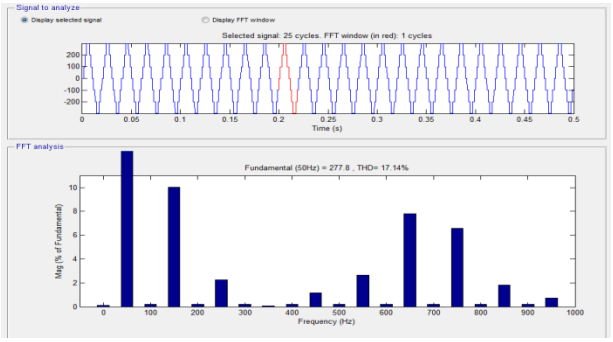

Fig.8. shows Total Harmonic Distortion Seven Level output voltage.

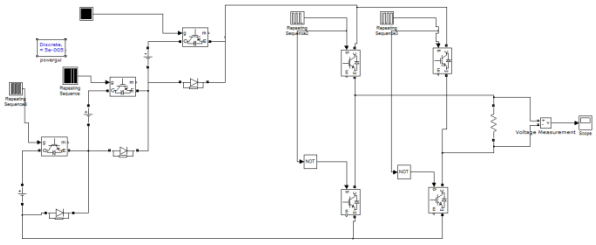

Fig.9. Simulink model of the Fifteen level inverter.

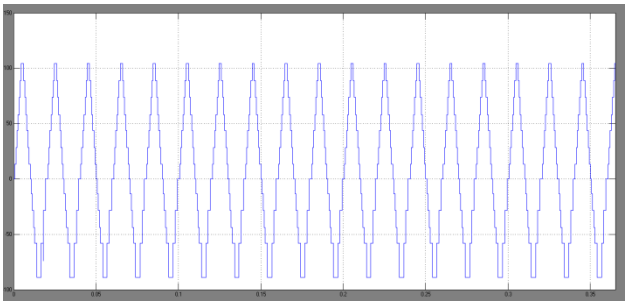

Fig.10. Simulated output wave form of the fifteen level inverter.

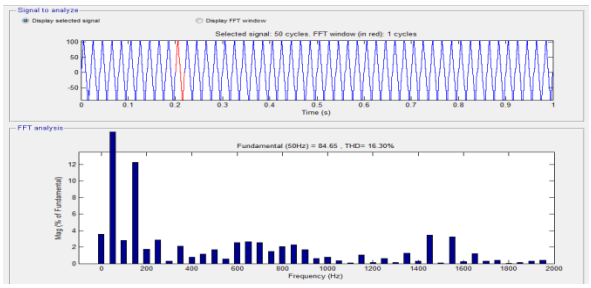

Fig.11. shows Total Harmonic Distortion Fifteen Level output voltage.

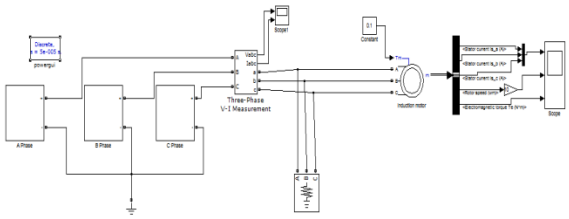

Fig.12. Simulink model of the proposed concept implemented with three phase induction motor.

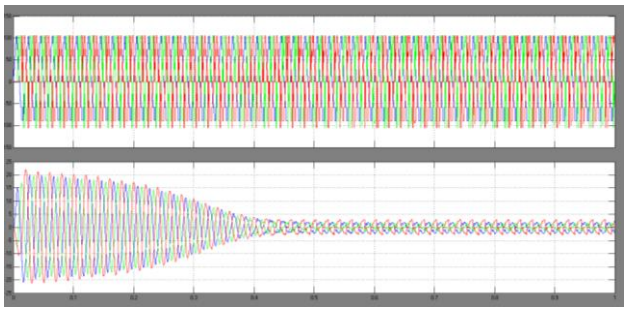

Fig.13. Simulated output voltage of the three phase 15 level inverter.

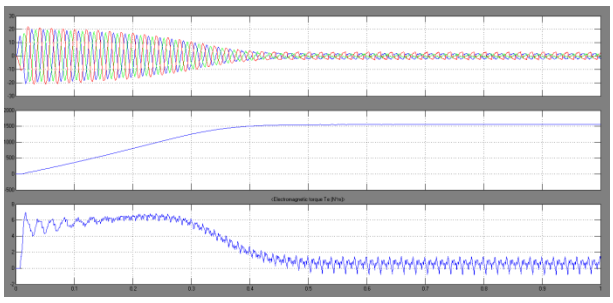

Fig.14. Simulated wave forms of the fifteen level inverter fed induction motor stator currents, speed and torque.

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VIII.CONCLUSION

This paper proposes new topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with reduced number of components for industrial drive applications. The proposed cascade structure extends the design flexibility and the possibilities to optimize the converter for different objectives such as the minimization of the number of IGBTs, gate driver circuits, dc voltage sources, standing voltage on switches, and power diodes. Less number of the switches leads to the reduction of size, simple control strategy, and high efficiency. This high efficient system fed to induction motor drive application and its performance characteristics as current, speed and torque has been simulated and studied by using matlab/simulink software.

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