ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Low Power Single Phase Clock Distribution Using VLSI Technology

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Abstract:

The clock distribution network consumes nearly 70% of the total power consumed by the Ie since this is the only signal which has the highest switching activity. Normally for a multi clock domain network we develop a multiple PLL to cater the need, this project aim for developing a low power single clock multiband network which will supply for the multi clock domain network. This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology.

INTRODUCTION:

Division operation is very important in the computer system. For division algorithm earlier they used Phased Lock loop (PLL), but now a day's we are using hardware module divider. There are so many techniques to implement the divider. In synchronous technique it always need clock signal to trigger the system. If we use this technique we may cause some problems like clock skew, dynamic power consumption etc. But in asynchronous circuits no need of system clock signals so it doesn't have the shortcomings mentioned above.Multiband RF circuits increases in conjunction.RF circuits need high power consumption. they demand high cost The integrated synthesizers for WLAN applications at 5 GHz consume up to 25 mw in CMOS realizations but it consumes large chip area and has a narrow locking range. To overcome this we used the best published frequency synthesizer at 5 GHz but it consumes power around 9.7 mw. In order to overcome this we used dynamic latches, dynamic latches are faster and low power consumption compare to static divider. The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problems. But E-TSPC prescaler will consume 6.25 mW. To overcome this we used a low power wideband 2/3 prescaler and wideband multimodulus 32/33/47/48 prescaler which can consume power up to 158.43 mw.Frequency dividers are also called prescaler which are used in many communication applications like frequency synthesizer, timing-recovery circuits and clock generation circuits. A prescaler is loaded at the feedback path of the synthesizer, takes signal and generates a periodic output signal and frequency. Frequency synthesizer is the one of the critical block because it operates at highest frequency and consumes large power. So there must be power reduction in the first stage of prescaler which will reduce the total power consumption.

1.1.Motivation:

In a wireless communication application is having frequency synthesizer. Prescaler determines the speed of VCO. It contains logic gates and flip-flops. This project aim for developing multi band network by using single phase clock which will supply for the multi clock domain network.

1.2.Literature Survey:

H.R.Rategh et al.,, "A CMOS frequency synthesizer with an injected locked frequency divider for 5-GHz wireless LAN receiver .Frequency divider having high power consumption. Due to the high input frequency, the first stage of the divider cannot be implemented in conventional static CMOS logic. Instead, it is commonly realized in source-coupled logic (SCL), which allows higher operating frequency, but burns more power. A more efficient alternative to the first SCL divider is the injection locking -divider employed in. However, this resonant divider requires a tank whose area is larger than the oscillator's tank, and it suffers from pulling phenomenaL. Lai Kan Leung, "A I-V 9.7-mW CMOS frequency synthesizer for IEEE 802.lIa transceivers, High speed frequency Prescaler is a fundamental module for frequency synthesizers and designing circuits are operates high frequency and its having high consumption..

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A Prescaler consists of flip - flops (FF) and extra logic, it determines the terminal count and Conventional high speed FF based divide by counter designs use current - mode logic (CML) latches and suffer from the disadvantage of large load capacitance.V. K. Manthena etc aIl, "A low power fully programmable J MHz resolution 2.4 GHz CMOS PLL frequency synthesize integrated phased array systems are for the most important part not too different from normal single channel transceivers and the phase shifter is the additional key point. A new phased array architecture that uses digital phase locked loop PLL modulator to realize phase shift is developed and to achieve phase shifting capability and PLL is a natural. If we combine PLL's phase shifting and modulation capabilities then we can realize phased array system using solely PLLs and with recent breakthrough in digital PLL, a digital circuits PLL generates the phase shift but analog circuits will not do this. In the data modulation using phase shift capabilities. With both phase shift and data modulation capabilities and we only need an array of such PLLs to realize a phased array. Compared with conventional phased arrays. It is also more flexible.

Thesis organization:

Chapter 1 gives introduction about project, the motivation, Literature survey and Thesis organization. Chapter 2 Describes about Clock networks Chapter 3 deals about Clock distribution Network. Chapter 4 deals in detail about Optical clock distribution Chapter 5 deals about Proposed method and classification and Chapter6 deals about summarizes the Verilog, Design issues, design reusability, importance of HDLs, design flow of verilog Also gives details about Xilinx ,overview, project navigator, creating project, creating source file and about synthesize & simulation. Chapter 8 deals about experimental results finally, the conclusion and suggestions for further refinement of the proposed solutions are given in Chapter 9.

THE CLOCK NETWORK:

The processing of data must occur. In a clock network, which the data are processed is coordinated by a clock signal. The clock signal, in the form of a periodic square wave that is globally distributed to control all sequential elements achieves synchronization of the circuit operation when all data are allowed to pass through the sequential elements simultaneously. A clock network is required to deliver the clock signal to all sequential elements.

The nature of long interconnects becomes more pronounced because of technology scaling, the control of arrival times of the same clock edge at different sequential elements, the entire chip is scattered, becomes more difficult. If not properly controlled, the clock skew, denned as the deference in the signal delays to sequential elements, can adverselyaect the performance of the systems and even cause erratic operations of the systems (e.g., latching of an incorrect signal within a sequential element).A well designed clock must also account for variations in devices. The complication of the network is the interplay between the clock network and the power/ground network. For example, all sequential elements are triggered almost simultaneously in a zero-skew clock network. Because these elements draw current from the power network or sink current to the ground network almost simultaneously when the clock switches, the zero-skew design often leads to severe power supply noise, resulting in unacceptable degradation in performance and reliability. This, in turn, acts the arrival times of clock signal at different sequential elements.There are many types of clock networks. Those are H-trees some combinations of them. In this project, we will consider burred H-trees driving local grids as representative of present clock distribution, to which we will refer as the conventional approach. Advanced active de-skewing techniques, which further improve the quality of standard clock distribution, are not considered in this simple analysis.Several interconnect solutions have been proposed to mitigate the increasingly difficult clock distribution, 3-D, optical, and RF being the most important ones. The advantage of the 3D-interconnects vertical dimension to decrease the die size, therefore alleviating clock distribution. Optical interconnects have also been proposed for clock distribution since they are immune to crosstalk noise from adjacent electrical interconnects, and because of their speed-of-light propagation. Optical interconnects also have the potential for large bandwidths, which are mostly relevant for signaling. The main difference between the RF approach and conventional approach is that RF uses a narrow-band sinusoidal wave for transmitting the clock signal as opposed to the digital square signal that is employed in conventional clock distribution.. Definitions.

2.1.Clock Skew:

A synchronous digital system typically consists of a series of registers, between which are blocks of combinational logic.

ISSN No: 2348-4845
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The functional requirements of the system are met by these blocks of combinational logic, while the registers provide the global performance and satisfy the local timing requirements. The registers are typically inserted in such a way that the combinational logic is partitioned into several time windows of ideally equal duration.The operation of a single stage in a pipelined synchronous system can be broken down as follows. Each data signal is stored in a register. The arrival of the clock signal latches a new value of the data into the register. At this time the data propagates through the register and into the combinational logic block. The signal passes through this network of logic, arrives at the input of the next register, and, for a properly functioning system, is stored on the next latching clock edge. The design of a clock distribution network is the difference in the arrival times of the clock edge between two registers. This difference is called clock skew, and the goal is to minimize, manage, or eliminate this term altogether.Clock skew is most important between sequentially adjacent registers. A formal definition for clock skew given by Friedman in is repeated below.Given two sequentially-adjacent registers, RI and RJ, and an equipotential clock distribution network, the clock skew between these two registers is defined as TSKEW(I,J) = TCI - TCJ, where TCI and TCJ are the clock delays from the clock source to the registers RI and RJ, respectively. Though the definition states that clock skew is a characteristic of sequentially adjacent registers, it exists, in fact, between any two registers. The presence of clock skew can severely limit the performance of a synchronous system, and even create a race condition that causes incorrect data to be latched in a register.

Power Dissipation:

The focus of most contemporary clock distribution network designs is the power dissipation associated with the clock signal. Increasing die sizes and operating frequencies have resulted in a significant, and sometimes inordinate, percentage of a chip power dedicated to the clock distribution. This cause and effect can be simply represented by the dynamic power equation P = CV2fWhere C is the capacitive load, f is the switching frequency and V is the voltage swing of the signal.The DEC Alpha 21164 microprocessor illustrates the extent to which the clock distribution network power dissipation can become a problem. The 21164 is a 16.5 mm 18.1 mm chip with 3.75 nF of capacitance on the clock net. With an operating frequency of 300 MHz and a power supply of 3.3 V, the clock distribution dissipates 65% of the 50 W consumed by the chip.In microprocessor designs of today the total power dissipation is a major concern. The present trends quickly result in power dissipations that complicate system-level design. For this reason a lot of attention is being focused on reducing the processor's total power dissipation, including that of the clock distribution.Examination of the above equation should reveal one of the best ways for reducing a chip's total power dissipation. Decreasing the power supply voltage reduces the squared term in the power equation. Since this affects all logic gates, including those associated with the clock distribution, it has a significant effect on the power dissipation..The sharp transitions required on the clock net are another cause for increased power dissipation. As the RC product of the clock network increases, the rise and fall times of the clock signal will increase unless there exists a corresponding increase in power. Another common method is to use multiple levels of clock burring. This has the effect of separating the high resistive load of the long clock nets from the high capacitive load of the register elements. More detail on clock distribution methods will be covered in a following chapter.A third method of reducing the power dissipation in the clock network is to shut o the clock signal to unused portions of the chip. This method is used to significant gain on the DEC Strong ARM microprocessor. It is estimated that conditional clocking reduced the power dissipation of the Strong ARM's clock network almost four-fold.

2.2.Jitter :

Increasing clock frequencies reveal a problem that has been previously considered negligible. With designs such as the DEC Alpha 21164 reporting a peak skew of 80 ps. at a clock period of 3.33 ns this rule seems easy to meet. However, future generation processors will see clock periods on the order of 1 ns. While clock skew itself may still be manageable at these frequencies (assuming die sizes remain the same), the quantity called jitter has yet to be considered.Jitter represents the time varying behavior of the clock signal. Noise from various sources because perturbations on the clock network that can cause any receiver of the clock signal to perceive a transition at a different time. The jitter performance of a typical phase-locked loop clock generator is 150 ps. This implies nothing about the jitter introduced along the network in the buffers or registers. Obviously, this quantity will become significant for future generation systems. The noise sources that contribute to jitter most significantly are the

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

following:Noise coupled through the circuit's power and ground connections; Noise coupled through adjacent or intersecting traces; Noise inherent to the circuit's transistors themselves.

THE CLOCK DISTRIBUTION NETWORK:

This section will discuss some design issues and methodologies for each of three general stages in a clock distribution network the clock generator; The global clock distribution; the local clock distribution. Where appropriate, the sections will cover design issues relating to the topics of clock skew, power dissipation, and jitter.

3.1.1.Global Clock Distribution :

The global clock distribution concerns the means by which the clock signal is relayed from the clock generator to the register loads. The routing, and signaling methodologies are major design decisions and have significant impact on overall system performance. The timing requirements involved in the clock distribution network make its design a very difficult one. In fact, system level trade-off s between system speed, physical die area, and power dissipation are significantly affected by the design of the clock distribution network. This section discusses some traditional methods for global clock distribution design and their characteristics in terms of clock skew, power and jitter.

3.1.2.Clock Tree :

By far the most common method for distributing clock signals in VLSI applications is the clock tree method. This tree structure is so called because buffers are placed between the clock source and along the clock paths as they branch out towards the clock loads. Figure 3.2 illustrates the organization of a clock tree distribution network. The distributed buffers amplify the clock signal to remove any degradation of the signal due to interconnect resistance between the clock source and the registers. An extension of this scheme is demonstrated by the DEC Alpha 21064 microprocessor (Figure3.3). In this have stage buffer tree design, one of the intermediate clock tree stages was made into a mesh by strapping metal lines across each of the branches. This minimizes both the delay through the clock distribution and the total skew within it.

Furthermore, the inputs to previous buffer stages were strapped together to smooth any asymmetric arrival times of the clock signal.If the interconnect resistance from the clock source to the registers is negligible, then the clock tree scheme can be reduced to a single buffer driving the entire network. The advantages of this strategy are the removal of the skew introduced by the distributed buffers, and the reduced area obtained by eliminating the distributed buffers. However, the single buffer must be capable of providing enough current to drive the network capacitance of the interconnect and register loads, while maintaining sharp, consistent transitions. In this clock distribution network, a tree of buffers converges on a single buffer which drives the entire clock load of 3.75 nF. This design resulted in an incredibly low maximum clock skew of 80 ps across the 16.5 mm x 18.1 mm die. However, the price for this performance was the dissipation of nearly 65% of the total processor power of 50W in the clock distribution network.

Wireless Clock Distribution:

Clock distribution is a crucial aspect of modern multi-GHz microprocessor design. Conventional distribution schemes are more or less monolithic in that a single clock source is fed through hierarchies of clock buffers to eventually drive almost the entire chip. This raises a number of challenges. First, due to irregular logic, the load of the clock network is non-uniform, and the increasing process and device variations in deep sub-micron semiconductor technologies further ads to the spatial timing uncertainties known as clock skews. Second, the load of the entire chip is substantial, and sending a high quality clock signal to every corner of the chip necessarily requires driving the clock distribution network \hard", usually in full swing of the power supply voltage. Not only does this mean high power expenditure, but it also requires a chain of clock buffers to deliver the ultimate driving capability. These active elements are subject to power supply noise, and add delay uncertainty jitter which also eats into usable clock cycle. Jitter and skew combined represent about 18% of cycle time currently, and that results in indirect energy waste as well. To compensate and make the circuitry faster, the supply voltage is raised, therefore increasing energy consumption. Conversely, any improvement in jitter and skew generates timing slack that can be used to allow the logic circuit to operate more energy efficiently. As commercial microprocessors are rapidly becoming multi-core systems, monolithic clock distribution will be even less applicable.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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In the era of billion-transistor microprocessors, a single chip is really a complex system with communicating components and should be treated as such. In communication systems, synchronizing clocks is also a rudimentary and crucial task. In this section, we will discuss the concept of wireless clock distribution network in a microprocessor. Wireless interconnect should provide an additional means for global communications, freeing up conventional wires for other uses. This new interconnect technology is being developed utilizing a clock distribution system as the driver. Using wireless interconnects in a clock distribution system should reduce the latency in the clock tree which should help reduce clock skew .and should eliminate the frequency dispersion problem that may ultimately limit the maximum clock frequencyA conceptual illustration of a single-chip or intra-chip wireless interconnect system for clock distribution is shown in Figure 3.5 An approximately 20-GHz signal is generated on-chip and applied to an integrated transmitting antenna which is located at one part of the IC. Clock receivers distributed throughout the IC detect the transmitted 20-GHz signal using integrated antennas, and then amplify and synchronously divide it down to a 2.5-GHz local clock frequency. These local clock signals are then buffered and distributed to adjacent circuitry. Figure 3.6 shows an illustration of a multi-chip or inter-chip wireless clock distribution system.

3.2.Clock Receiver :

Figure 3.8 shows a block diagram for an integrated clock receiver. The global clock signal is detected with a receiving antenna, amplified using a low noise amplifier (LNA), and divided down to the local clock frequency. These local clock signals are then buffered and distributed to adjacent circuits. The amplifier is tuned to the clock transmission frequency to reduce interference and noise. Since the microprocessor is extremely noisy at the local clock frequency and its harmonics, transmitting the global clock at a frequency higher than the local clock frequency provides a level of noise immunity for the system. Also, operating at a higher frequency decreases the required antenna size.

Comparison of Power Consumption with Conventional Methods :

Kenneth et al. have discussed the power consumption in a wireless clock distribution network and given a comparison with conventional clock distribution networks.

To compare the power requirements between different types of global clock distribution systems, the system voltage and frequencies are assumed to be equal. Under these assumptions, the power dissipation can be converted to capacitances and these can be used to compare the power dissipation of different global distribution systems, similar to an approach taken in.The total global capacitance can be allocated among three components: CG, CW, and CL. CG are the equivalent capacitance of the highest level network which delivers the clock from its source to spine locations distributed throughout the chip. CG includes the total capacitance of the nal driver stage, herein termed the sector buffer, plus any buffers leading up to the sector buffer. The sector buffers are assumed to be exponentially tapered for minimum delay. CW is the capacitance of the interconnecting wires for delivering the clock from the spine locations to the local distribution system. CL is the load capacitance representing the input capacitance of the local clock generators.Two cases are used in comparing these clock distribution systems for 0.1-um generation microprocessors. Case 1 is for aluminum interconnects and conventional dielectrics; case 2 is for copper interconnects and low-K dielectrics.

3.3.Grid Based System :

The grid-based system, based on DEC 21264, consists of a global tree supplying the clock to different spine/buffer locations, and the capacitance of this network is CG. These buffers drive the clock grid, which has capacitance CW. The local clock generators tap o of the grid. Due to the amount of wiring used to form the grid, CW is large. Consequently, large sector buffers are needed, increasing CG.The wireless system consists of a clock transmitter broadcasting a microwave signal to a grid of distributed receivers. A receiver corresponds to a spine location. Due to their low capacitance, balanced H-trees are used to distribute the signal from the receivers to the local clock generators. Thus, CW for both the H-tree and wireless schemes is equal. In wireless clock distribution systems, long interconnects for delivering the clock from its source to spine locations are not present and the associated component of CG is zero. However, since the wireless system contains components with static power dissipation, an equivalent global capacitance, representing this power dissipation, is needed. This capacitance is then used to make a comparison to the grid and H-tree systems. To obtain this equivalent capacitance, the total power dissipation of the clock transmitter and receivers is divided by the factor (V2f).Table 3.1 shows a breakdown of

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

the global capacitive loading for the three distribution systems for cases 1 and 2, and includes the initial 0.25-um data. All capacitance units are in pF. The nal row gives the power consumed by the global clock distribution systems as a percentage of total microprocessor power. This percentage represents the relative amount of power dissipated in the global system to drive a load of CL. The results show that for both cases, the wireless system is comparable in performance to the H-tree system and better in performance than the grid-based system in terms of power dissipation. The results also show that technology developments such as Cu or low-k will have the greatest positive impact on systems whose total equivalent capacitance is dominated by CW, such as the grid. Finally, the results show that the power dissipated in the clock receivers, given by CG, should be a small fraction (2.3%) of the total power dissipated in the microprocessor. These results show that power dissipation does not impose limitations for wireless clock distribution systems. However, additional work focused on the overall feasibility and implementation of this system is ongoing.

3.4.Potential Benefits :

The wireless clock distribution system would address the interconnect needs of the semiconductor industry in providing high-frequency clock signals with short propagation delays. These needs would be met while providing multiple benefits. First, signal propagation occurs at the speed of light, shortening the global interconnect delay without requiring integrated optical components. Second, the global interconnect wires used in conventional clock distribution systems are eliminated, freeing up these metal layers for other applications. Third, referring to Figure 3.2, the inter-chip clock distribution system can provide global clock signals with a small skew to an area much greater than the projected IC size. This is an additional benefit, possibly allowing synchronization of an entire PC board or a multi-chip module (MCM). Fourth, in the wireless system, dispersive effects are minimized since a monotone global clock signal is transmitted. Fifth, another benefit is a more uniformly distributed power load equalizing temperature gradients across the chip. Sixth, by adjusting the division ratio in the receiver, higher frequency local clock signals can be obtained, while maintaining synchronization with a lower frequency system clock. Seventh, an intangible benefit of wireless interconnect systems is the e ect they could have on microprocessor or system implementations, potentially allowing paradigm shifts such as drastically increased chip size. Finally, compared to other potential breakthrough interconnect techniques, such as optical, superconducting, or organic, a wireless approach based on silicon seems to be a potential solution which is compatible with the technology trends of the semiconductor industry.

3.5.Areas of Research :

The main areas of research for wireless clock distribution are as follows: integrating com-pact power-efficient antenna structures, identifying noise-coupling mechanisms for the wire-less clock distribution system and estimating the signal-to-noise ratio that can be achieved on a working microprocessor, implementing the required 20-GHz circuits in a CMOS process consistent with the ITRS , and characterizing a wireless clock distribution system in terms of skew and power consumption and estimating the overall feasibility of the system.

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