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DS-CDMA Implementation with Iterative Multiple Access Interference Cancellation

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ABSTRACT:

In this paper an implementation of iterative joint detection for multiple access interference using direct-sequence code-division multiple-access (DS-CDMA) is presented. Results for multiple field programmable gate array (FPGA) platforms and multiple technology nodes for synthesized application specific integrated circuits (ASIC) are resented. The joint detection is performed using a generalized version of Interleave-Division Multiple-Access (IDMA) known as partition spreading (PS) CDMA. Decoding is performed using iterative methods from turbo and sum-product decoding. The synthesized ASIC system demonstrates a maximum aggregate throughput of 197 Mb/s for a fully loaded 50-user system, while the implemented FPGA 50-user system has a maximum aggregate throughput of 119 Mb/s.

Index Terms:

Digital circuits, direct-sequence code-division multiple access, field programmable gate arrays, interference cancellation.

I.INTRODUCTION:

The cellular concept originated at Bell Labs in 1947. The first automatic analog cellular system started operation in Japan in 1979 and in the Nordic countries in 1981. The first commercial AMPS wireless cellular system in the United States started in October 1983 in Chicago. Analog cellular service introduced in 1983 and it operates on the 800 MHz frequency band based on FDMA (Frequency Division Multiple Access). It became apparent that higher capacity, more reliable, and lower cost wireless systems were needed to meet booming demand. In CDMA cellular systems (e.g. IS-95 in the United States) that use direct sequence spread (DSS) spectrum techniques, the (digital) information from an individual user is modulated by means of the unique PN code (spreading sequence) assigned to each user. All the PN –code-modulated signals from different users are then transmitted over the entire CDMA frequency channel (e.g., 1.23 MHZ in case of IS-95). Since the signal in the case of CDMA utilize the entire allocated block of spectrum, no guard bands of any kind are necessary within the allocated block.

II.CELLULAR COMMUNICATIONS :

A cellular mobile communications system uses a large number of low-power wireless transmitters to create cells which are the basic geographic service area of a wireless communications system. Each cell consists of a base station (BS) transmitting over a small geographic area usually depicted as an hexagon (the true shape of a cell is not a perfect hexagon due to constraints impose by the terrain).

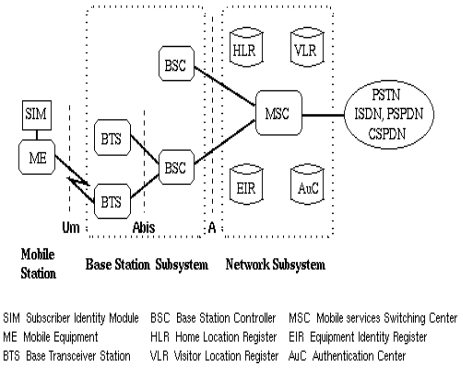

Fig 1: structure of cellular communication systems

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Different spread spectrum techniques can be used in communications systems such as: Direct-Sequence (DS), Frequency-Hopping (FH), Time-Hopping (TH), Multi-Carrier CDMA (MCCDMA) and chirp modulation. As DS-CDMA systems are the main concern in this work, a brief description of this technique is presented here.

A.Direct-Sequence Systems:

A direct sequence (DS) spread spectrum technique is performed by multiplying a radio frequency (RF) carrier and a pseudo-noise (PN) digital signal. First the PN code is modulated onto the data signal, using one of several modulation techniques (e.g. BPSK, QPSK, etc). Then the PN modulated data signal and the RF carrier are multiplied. This process causes that the RF signal to be replaced with a very wide bandwidth signal with the spectral equivalent of a noise signal. In the reception of the signal, the receiver must not only know the code sequence to dispread the signal but also it requires to be synchronised with the code generator in the transmitter.

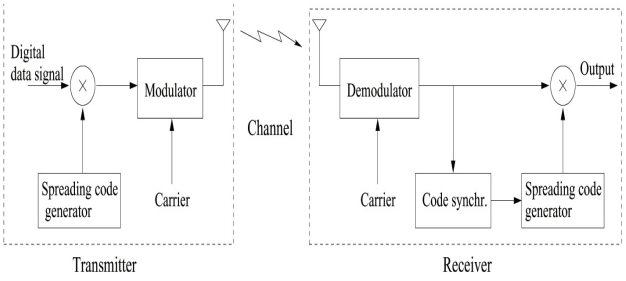

Fig.2 DS/SS system

B.FEC Coded DS-CDMA System:

In a DS-CDMA system all users share the same communication channel overlapping the transmitted signals both in time and frequency. To separate and detect the intended data signal a unique spreading waveform is assigned to each of the users in the system. FEC coded signals are treated in this work not only as a medium of resistance to the degradations introduced by the communication channel (physical medium) but also because it plays and essential role in the iterative multiuser receiver structures.

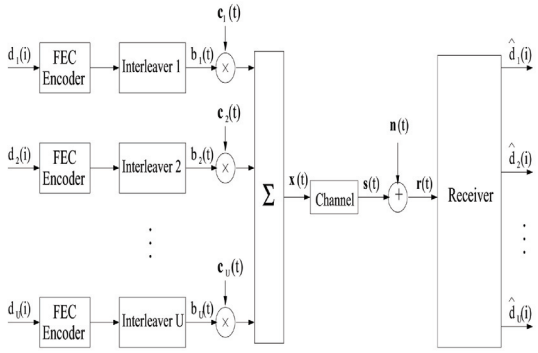

Fig.3 Coded DS-CDMA system model for the downlink (base station to mobile)

In this model each user transmits an input data stream, {du (i)} € {1, 2. . . U} with u € {1, 2. . . U}, and i € {1, 2. . . L}, where each individual data bit is first encoded with a rate R0 and then passed through a modulation function. At the encoder output each user transmits L/ R0 coded bits bu (t) ϵ {-1, 1} where t € {1, 2. . . L/R0} identifies the coded bit interval and u as defined before. To reduce the effect of error bursts at the input of the decoder channel, interleaving (π) is incorporated at the encoder output as is shown in Figure 3. The resulting interleaved coded bits are then spreading by a unique PN code sequence, Cu (t). The nth chip of the spreading code Cu (t) is defined as Cu, n (t) € {-1/√N, 1/√N}, where N is the processing gain of the system and n € {1, 2, ... , N}. A mathematical representation of the transmitted signal at time t is expressed as:

$$\mathbf{x}(t) = \sum_{u=1}^{U} \sqrt{P_u}\mathbf{c}_u(t)b_u(t).$$

where Pu denotes the transmitted power of the uth user. For the downlink, the signals are passed synchronously through the same communication channel since the users' signals are transmitted by the same source (base station). At the receiver side, the received signal, r (t) = s (t) + n (t), results from the convolution of the channel response and the transmitted signal, represented by s(t), plus the additive white Gaussian noise (AWGN), n(t).

Finally, the intended signal is extracted from r (t) by dispreading the signal with the same code used in the transmitter. If orthogonal spreading codes are used, i.e. CTu (t) Ck (t) = 0 for u, k € {1, 2, • • •, U} where u ≠ k, no mutual interference exist between users in the system and then only the impairments from the channel are the noise sources. This type of interference is called multiple access interference.

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III.TRANSMITTER:

As shown in Figure 4, a basic transmitter scheme consists primarily of the FEC encoder and spreading functions for each of the users in the system. One of the reasons of using FEC coding is to increase the robustness of data transmission over the distortions and disturbances of the physical channel. Since the physical channel provokes degradation in the system performance, in terms of the bit error rate (BER), FEC coding is used to reduce the required signal to noise ratio (SNR) for a fixed BER.

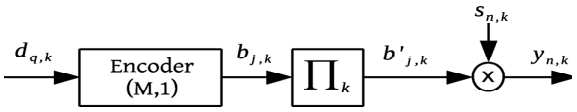

Fig.4 PS-CDMA transmitter diagram with repetition coding and interleaving of partitions.

At the transmitter encoded bits dg,k of user k, k ϵ {1,...,K}, q ϵ {1,..., L} (d) could be the result of high-rate LDPC encoding as this detector performs very well in conjunction with high rate codes are encoded by a repetition code (M, 1) as part of the DSSS modulation operation. The resulting coded bits bj.k, j ϵ {1, .., Nm} , Nm = LM , are interleaved by a user-distinct interleaver ∏k to obtain b1j,k.

IV.RECEIVER:

In the particular case where the signals from different users are uncorrelated, the conventional detector (or single-user detector) is optimum. However, in practise the signals from different users will be correlated which means that the conventional detector will be suboptimum.

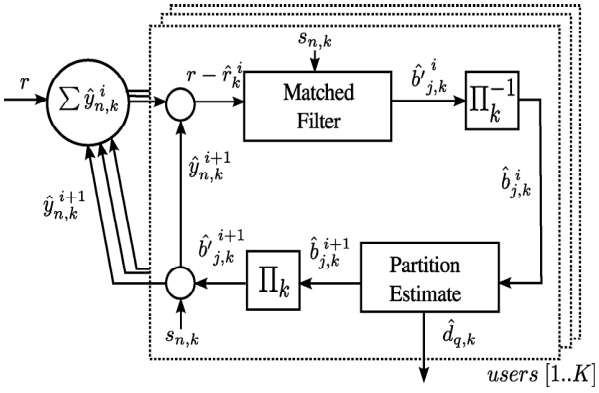

Fig. 5 Block diagram of the demodulation operation of the PS-CDMA receiver

Single-User Detector: The conventional detector or RAKE detector for the received signal given is a bank of α + 1 correlators (called fingers) for each user, as shown in Figure 5 where zc-1 is a delay of one chip.

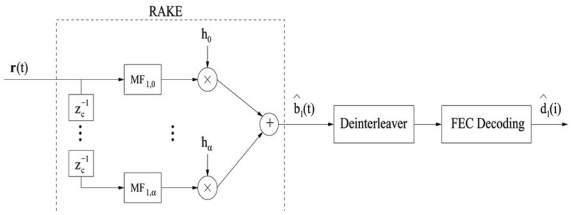

Fig. 6 The conventional DS-CDMA detector for user with FEC decoding

The outputs of the fingers provide with α + 1 replicas of the same transmitted signal at the receiver but with a delay of one chip between each other. These replicas are then combined to yield a single soft estimate of the transmitted data symbols. Since each finger detects one user without regard to the existence of the other users whose interference is assumed to be Gaussian, the optimal combining weights are the path coefficients of the channel. This is equivalent to an α + 1 branch diversity system with maximum ratio combining (MRC). Therefore, the output of the RAKE detector for the uth user is mathematically represented as

$$\hat{b}_u(t) = \sum_{a=0}^{\alpha} h_a \mathbf{c}_u^T(t)\mathbf{r}(t - aT_c)$$

Where r (t - aTc) is a delay version of the received signal r(t) (with Tc as the chip period). Considering that each transmitted signal arrives at the receiver over a single path (no multipath i.e α = 0 and with a channel coefficient amplitude h0 = 1, the conventional detector for the uth user is reduced to implement a single matched filter detector which gives as an output where the correlations with all the others users (ρu,k ≠ 0) give rise to the MAI term and the correlation with the thermal noise yields the noise term zu (t)..

V. PROPOSED ITERATIVE DEMODULATOR FOR PS-CDMA:

All users' chip estimates are aggregated and subtracted from the original received aggregate signal. If the estimates are perfect, the only values left are the contribution of noise to that chip. However, the interference cancellation has removed the user's own information, so that is added back in, which each user does within its respective

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receiver to attain a user specific version of the interference-reduced received signal. The system then iterates until MAI has been cancelled sufficiently to attain acceptable BER.

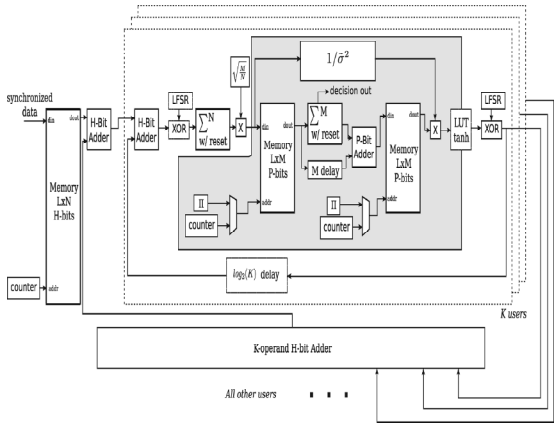

Fig 7: Architecture of the proposed iterative demodulator for PS-CDMA.

The elements within the dashed box make the individual data receiver, while the contents within the shaded area make the partition processing datapath. The datapaths each have a bit width or precision of P-bits or H-bits. All circuits within the shaded area use P-bits, otherwise circuits have a precision of H-bits. Hard decisions for BER calculation are generated with the partition processing datapath. The transmitted signal is stored in memory, using entries each with H-bits. This memory is shared among all receivers as the data is streamed to all K receivers simultaneously.

Matched Filter:

Chip arrival between all users is assumed to be synchronous, so the matched filter consists of an gate, an accumulator (with reset), and a scaler. The scaler multiplies the partitions by the sign-magnitude form by tying the output of the linear feedback shift register (LFSR) with the most significant bit (MSB) of the data.

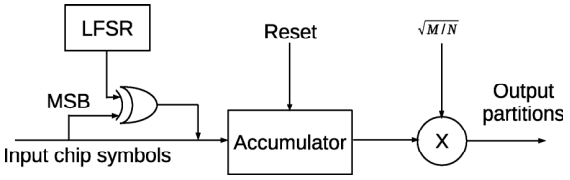

Fig. 8 Matched filter block diagram

The LFSR is a 51 stage delay line, with stages 1 and 4 tapped. The value of each stage is programmed to a unique sequence for each user. The length and taps were chosen to supply a suitable pseudo-random number generator. In the matched filter a transition between two processing domains occurs, the chip processing domain and the partition processing domain. The chip processing domain requires a greater precision in data representation of H-bits, while the partition processing domain requires a less precise representation of P-bits. This occurs due to the soft processing that occurs in the tan h-limit, whereas the cancellation requires a precision that can handle fractions of transmitted amplitudes. After the matched filter the data takes two parallel paths. The first path forms estimates of the data and calculates hard decisions. The second path is used to form an estimate of the variance in the signal.

Turbo Codes:

This error correcting code is able to transmit information across the channel with arbitrary low bit error rate (BER). This code is a parallel concatenation of two component convolutional codes separated by a random inter-leaver that combines concepts such as iterative decoding and soft input soft output (SISO) decoding. The original turbo encoder scheme consists of a combination of two convolutional codes in a parallel concatenation. This turbo encoder consists of two RSC codes in a parallel concatenation. Both encoders (RSC 1 and RSC 2) receive the same binary data bits in a continuous or block fashion but arranged in a different sequence due to the presence of a random inter-leaver.

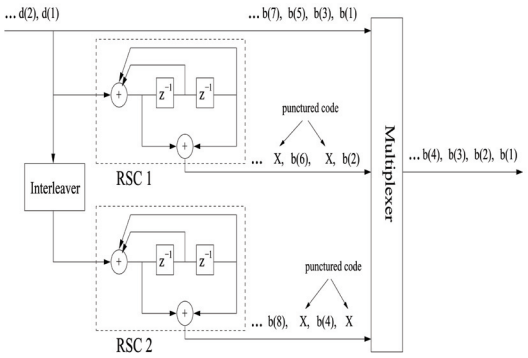

Fig.9 Turbo encoder structure for a rate 1/2

Interleaver: It has a depth of L * M elements, and instead of storing the indices, they are calculated in order to reduce usage of memory resources. The design can operate in parallel, but we chose a serial implementation shown in Fig. 9.

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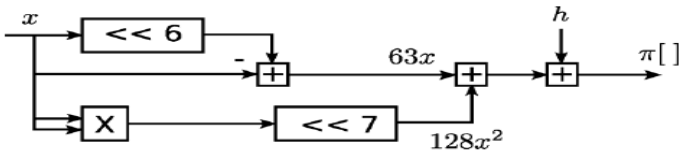

Fig.10 On-the-fly interleaver

The permutation polynomial being calculated is :

$$(63x + 128x^2 + h)\mathrm{mod}(\mathrm{L} * \mathrm{M})$$

It is generated by a counter and only one multiplier is needed. The value is introduced to create unique interleavers. The interleavers implemented in the FPGA rely on available block random access memory (BRAM). The sequential design introduces latency since the entire frame of partitions must be written in to memory before being read out.

Interference Cancellation Schemes:

A second way to perform MUD is using an interference cancellation scheme. This category of detectors can be classified mainly into three sub-categories: Parallel Interference Cancellation (PIC), Successive Interference Cancellation (SIC) and Hybrid Interference Cancellation (HIC). The basic principle of these schemes is to estimate at the receiver the MAI generated by each user in order to subtract it.

V.HARDWARE & RESULTS:

The FPGA test bed is comprised of a personal computer communicating to a FPGA through Ethernet and a DSP daughterboard. The synthesis results are based on outputs from Synopsys(D-2010) and Encounter (EDI 9.1). On two different Lyrtech development boards (C67X and QC6416) the Virtex FPGA (XC2V8000 and XC4VLX160) is completely devoted to the implementation of the PS-CDMA detector, while the Texas Instruments digital signal processor (DSP) (TMSC32C7 and TMS320C6416) serves as a convenient gateway to the input and output pins of the FPGA through an Ethernet connection to the PC. The K transmitters and AWGN channel are implemented in software in the PC and their resulting cumulative transmission is sent over the Ethernet connection to the DSP and subsequently to the FPGA. The testbed and all simulation results are based on baseband processing. The implementation results for the FPGA testbed and ASIC synthesis are summarized in this section.

Logical equivalence between C++ simulations, VHDL simulations and the FPGA implementation was confirmed using Model Sim and a custom program that interfaces with a test circuit to calculate errors seen in the detector. The implementation was found to have acceptable performance using and on their respective datapaths. The implementation results are based on only 50 frames and a finite block length of L = 512, which accounts for the minor degradation of the performance with respect to the case of infinite block size. The decoders were allowed to iterate for many iterations (100) in order to determine best BER performance possible.

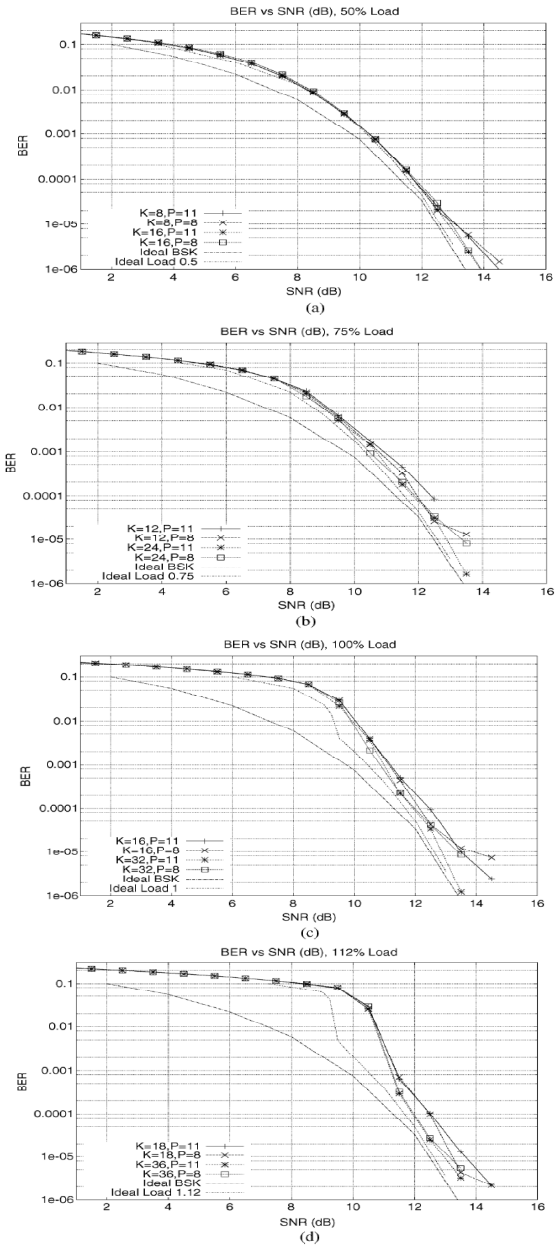

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Fig.11 Various PS-CDMA systems with different loads with the systems use M = 4 partitions, L = 512 symbols. BER for two different precisions are for the partition processing H = 11 and P = 8 or 11 over 10 frames. (a) PS-CDMA with 50% load; (b) PS-CDMA with 75% load; (c) PS-CDMA with 100% load; (d) PS-CDMA with 112% load.

VI.SUMMARY:

This paper presented the implementation of a joint detection iterative interference cancellation architecture. The base unit of the architecture is comprised of a few simple components, which allows large system implementations, while still giving good performance. The control module, variance module and the cancellation modules were identified as logic blocks that could be reduced in their logic requirement, while the serial nature of the interleavers was identified as a bottleneck for the throughput and the major contributor to implementation area.

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