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Design of Area efficient Conditional CMOS 8-bit Magnitude Comparator

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Abstract:
We present a Comparator with less Transistor count and low power by having less Active number of Transistors. Designed circuit is based on conditional methodology which does not require any Boolean equations. Conditions only will be checked whether the Output to become True(False). Limited Fan-in and Fan-out is also achieved irrespective of the Word size. Total number of transistor count for N-bit is (N-1)*12+(N-1)*10+6+10+4. The main theme is to provide new low area solution for transistor level designers. Static CMOS logic style is being considered for Designing the Circuit which has the Prime Disadvantage of occupying more Area corresponding to number of Transistors at the Circuit level. The conditional approach presented will be helpful in Optimizing the VLSI Design Constraint of Area which leads to optimization of other Design constraints. Circuit was designed by using S-EDIT tool for Schematic entry and T-SPICE for Simulation of TANNER EDA tool.

IndexTerms:
Oddbit, Evenbit ,Comparator, CMOS.

I.INTRODUCTION:
Low density parity check (Ldpc) was designed by gallager in 1962[1]. Implementation of ldpc decoder consumes more power as well as area but with high speed, comparator is important module in decoder and it is also used in digital system. C-H HUANG developed priority encoder based on logic and module which has high performance , low power and more area[2]. S-W CHENG employed conditional sum adder to design efficient comparator with high speed ,low area and more power consumption[3].

J-Y KIM and H-J YOO proposed a design without arithmetic operation which is even more efficient with area but used dynamic logic which can lead to malfunctioning of the circuit[4]. Add-Compare-Select block will be performing three different operations like Addition, Comparison and Multiplexing, here asynchronous logic is being employed without under the control of the clock[5]. Static Cmos will be having by default good Logic '1' and Logic '0' Levels, so mostly Static Cmos based Digital IC are the choice of Digital Designers when compared to Dynamic logic[6].If we are more concerned with performance for our Design then any Sum of Products or Product of Sums will normally give the high Speed because total number of levels will be less but not low Area and low power [7]. Any expression can be directly translated into equivalent transistor level Cmos Circuit by following De-morgan's law but to do so we need to have a expression[8]. Geetanjali Sharma comparator is based on gate level circuit designing which is not the lowest level of design abstraction[9].Saleh Abdel Hafeez proposed high speed comparator at expense of Area but used transmission gates logic which does not have any power rails and leads to a non-uniform structure when designing layout[10]. Comparator was designed by implementing our own conditional approach such that functionality of the circuit should be obtained but keeping in mind the design constraints like AREA as well as POWER as these are our concern[1][2][3]. To design Comparator choice of logic is not dynamic logic[4], synchronous logic is being employed[5] and logic style used is STATIC CMOS[6]. Design is not based on any Boolean equations converted into a gate level circuit[7], any expression converted into a transistor level circuit[8] still this is not the lowest level of design abstraction.

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Design is not based on pure digital logic gates[9] and no transmission gates used in our design[10].STATIC CMOS has uniform structure in pull-up and pull-down network, so layout designers can design layout efficiently. To achieve less transistor count we can chose logic styles like PTL which by default takes less number of transistors but it also has limitations of Transmission gate. VLSI has a trade-off among the design constraints like Area, Power and Speed so any two constraints in general will be kept in mind and making sure that low priority constraint is not that neglected.

II.MAGNITUDE COMPARATOR:

Comparator is going to compare 8 bits of A(A7 to A0) and 8 bits of B(B7 to B0) and decides whether ALTB(A<B) or AGTB(A>B) or AEB(A=B). Conventional Digital CMOS cells are not utilized in the Design .we need to know what are all the conditions for ALTB(A<B) to become true, if (A7<B7) then ALTB(A<B) should be true and 6T circuit which has one not gate and one two input nand gate has been designed and nand gate has one output. Now let us see the second condition that is if (A6<B6) and if (A7=B7) then ALTB(A<B) should be true, so we have designed XOR block with inputs as A7,B7 with one output and nand gate output is given to Even10T block which also has another inputs as A6 and B6 and nand gate output and this block has only one output and it has two conditions in it And now conditions required for A=B are the condition is (A7=B7) for first bit equality that is already being designed with XOR now for second bit equality condition is(A6=B6) so second bit equality and first bit equality condition, Even 12T block is being designed with inputs as A6,B6 and XOR output and it has one output.. so till now (A<B) and (A=B) up to 2 bits have been designed Now let us see the third condition for ALTB that is if (A5<B5) and if (A7=B7) and (A6=B6) but 2-bit equality output is readily available, so Even 12T block output as one of the input , A5 and B5 are the inputs 10T Odd block is designed with one output. And another input is 10T Even block output which has 2 conditions in it. So to design the fourth condition for ALTB that is if (A4<B4) and if (A7=B7), (A6=B6) and (A5=B5) but for this third equality condition added to the 2-bit equality condition gets the output for 3-bit equality and for this 12T Odd block being designed with inputs as A5,B5 , 2-bit equality output. We will get 12T Odd block with one output and now 10T Even block with inputs as A4,B4 , 12T Odd output and 10T Odd as one of the input we will get 10T Even block which has four conditions in it.

Now we go for (AEB) that is if (A5=B5) and (A4=B4) , anyhow for till 3-bit equality condition 12T Odd is readily available and now for fourth bit equality condition 12T Even block can be utilized with inputs as A4,B4 and 12T Odd output which has three conditions in it. Now let us see the fifth condition for ALTB that is if (A3<B3) and if (A7=B7), (A6=B6), (A5=B5) and (A4=B4) but 4-bit equality output is readily available, so Even 12T Even block output as one of the input , A3 and B3 are the inputs and 10T even block as one of the input 10T Odd block is being utilized . So to design the sixth condition for ALTB that is if (A2<B2) and if (A7=B7), (A6=B6), (A5=B5) ,(A4=B4) and (A3=B3) but four bit output is only available so for fifth bit equality 12T Odd block is utilized with inputs as A3,B3 and 12T Even out for this fifth equality condition added to the 4-bit equality condition gets the output for 5-bit equality and for this 12T Odd block being designed with inputs put which has 4-bit equality condition in it. Now 10T Even block is utilized with inputs as A2,B2, 5-bit equality output and 5 conditions for (A<B). Now we go for (AEB) that is if (A3=B3) and (A2=B2) , anyhow for till 5-bit equality condition 12T Odd is readily available and now for sixth bit equality condition 12T

Even block can be utilized with inputs as A2,B2 and 12T Odd output which has five conditions in it.Now let us see the seventh condition for ALTB that is if (A1<B1) and if (A7=B7), (A6=B6), (A5=B5), (A4=B4), (A3=B3) and (A2=B2) but 6-bit equality output is readily available, so Even 12T block output as one of the input , A1 and B1 are the inputs and 10T even block as one of the input 10T Odd block is being utilized . So to design the eighth condition for ALTB that is if (A0<B0) and if (A7=B7), (A6=B6), (A5=B5) ,(A4=B4) ,(A3=B3),(A2=B2) and (A1=B1) but six bit output is only available so for seventh bit equality 12T Odd block is utilized with inputs as A1,B1 and 12T Even out for this seventh equality condition added to the 6-bit equality condition gets the output for 7-bit equality Now 10T Even block is utilized with inputs as A0,B0, 7-bit equality output and 7 conditions for (A<B). Now we go for (AEB) that is if (A1=B1) and (A0=B0) , anyhow for till 7-bit equality condition 12T Odd is readily available and now for eighth bit equality condition 12T Even block can be utilized with inputs as A0,B0 and 12T Odd output which has seven conditions in it. Now we have 8-bit output for ALB(A<B) as well as AEB(A=B) and now we can use NOR gate to achieve AGB(A>B). There are 5cells in this comparator named Even10T ,Even12T, Odd10T , Odd12T and XOR .

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Fig1 is an XOR Circuit which is required to know the Equality Status at MSB stage, this Status is required at MSB-1 Stage of ALB(A<B) and it requires 10 number of Transistors. Fig2 is an Even10T Circuit which is needed to get the Output of ALB(A<B) at every EVEN bit position of the Primary inputs and it needs 10 number of Transistors. Fig3 is an Even12T Circuit which is needed to get the output of AEB(A=B) at every Even bit position of the Primary inputs and it takes 12 number of Transistors. Fig4 is an Odd10T Circuit which is needed to get the ALB(A<B) at every Odd bit position of the Primary inputs except at the MSB stage and it requires 10 number of Transistors. Fig5 is an Odd12T Circuit which is needed to achieve the AEB(A=B) at every Odd bit position of the Primary inputs except at the MSB stage and it needs 12 number of Transistors. Fig6 is Block Diagram of 8-bit Comparator which has one not gate, one nand gate, one XOR gate, three 10T Odd Circuits, three 12T Odd Circuits, four 10T Even Circuits, four 12T Even Circuits and one nor gate to achieve the AGB(A>B) Output. Our design is extendable to N-bit, from MSB-2 to any bit of LSB same blocks can be utilized with appropriate inputs it is like all the Odd primary inputs given to Odd10T and Odd12T and all the Even primary inputs given to Even10T and Even12T.Total number of transistor count for N-bit is (N-1)*12+(N-1)*10+6+10+4.

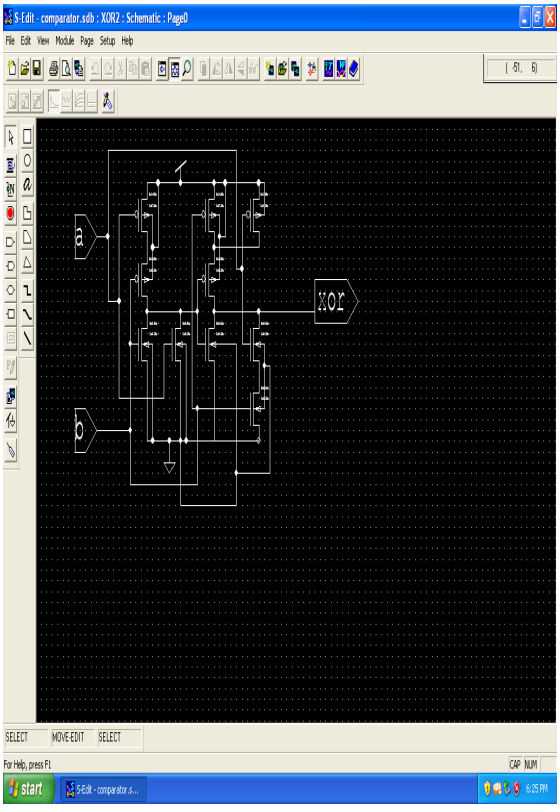

Fig. 1 XOR

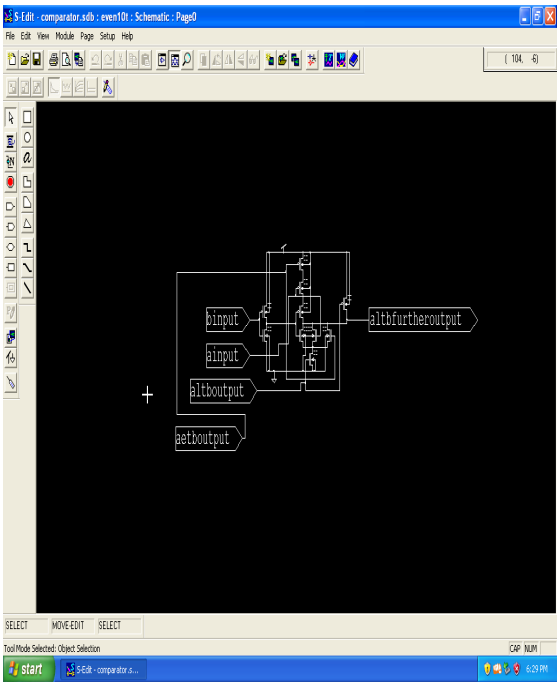

Fig. 2 Even10T Circuit

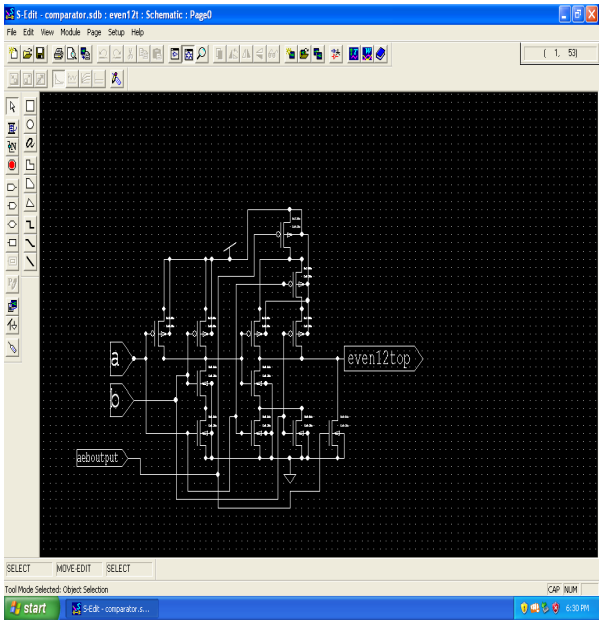

Fig. 3 Even12T Circuit

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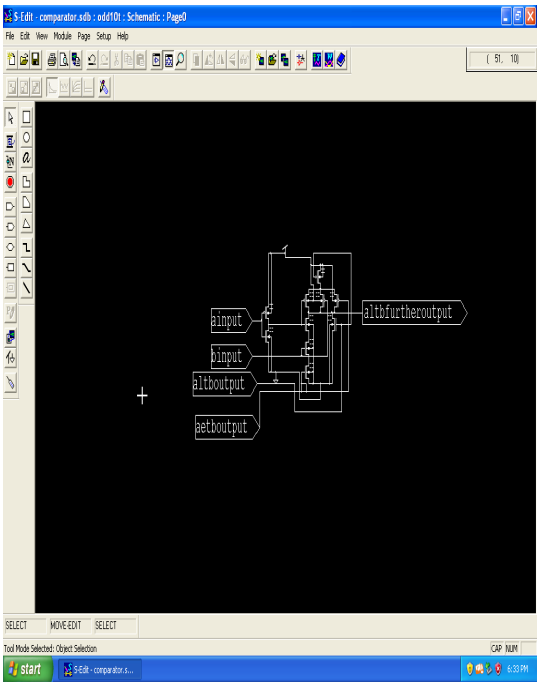

Fig. 4 Odd10T Circuit

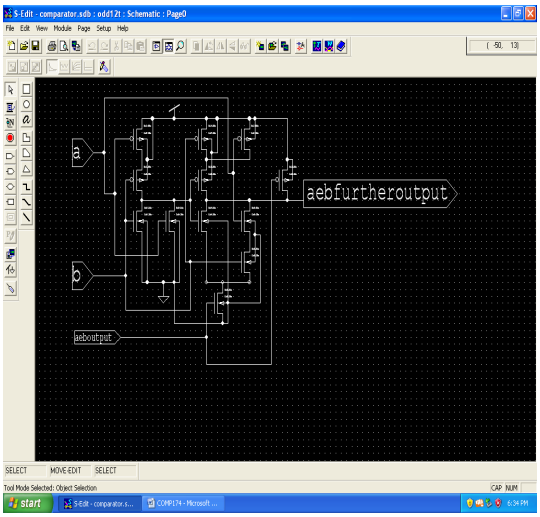

Fig. 5 Odd12T Circuit

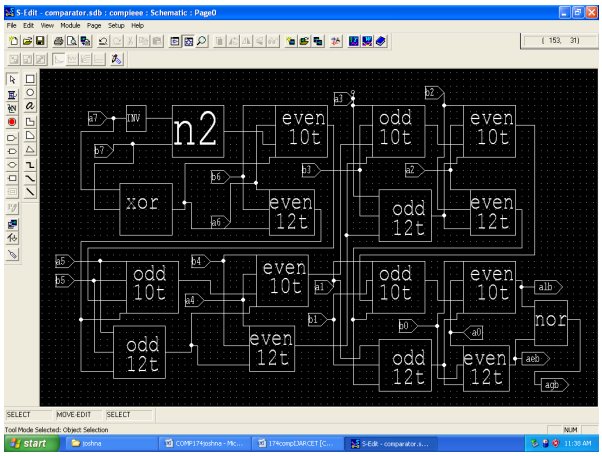

Fig. 6 Schematic of 174 transistor Comparator cell

III.STATIC CMOS:

STATIC CMOS has the advantage of having very less Static power dissipation and it has power rails so desired output will be obtained from it, Layout designers can design more possible efficient stick diagrams such that it will leads to the optimized VLSI design constraints like Area, Speed and Power. In Placement &Routing phase, only if placement is efficient then only effective routing is possible and it will affect the Metal Layers requirement. Full swing is one more advantage and either output will be pulled up to VDD or pulled down to GND. STATIC CMOS needs more number of transistors because for every P-MOS there will be corresponding N-MOS. Even though more number of P-MOS transistors or N-MOS transistors placed in series are going to increase the delay we can enhance speed by transistor sizing or by introducing buffer in which we need to sacrifice Area.

IV.PERFORMANCE ANALYSIS:

8-bit magnitude comparator has been designed by using STATIC CMOS logic style. Table1 shows AREA comparision of S.W Cheng, Saleh Abdel Hafeez and the proposed COMPARATOR. The comparator which we designed using STATIC CMOS logic style has less number of transistor count. 1570 transistors were reduced when compared to Saleh Abdel Hafeez for 64-bit, almost in a equal proportion transistor count reduction will be there for N-bit and 150 transistors were reduced in comparison with S.W.Cheng, count was less due to their logic can only identify '<' and ' >=' conditions which in contrast '<', '>' and '=' can be identified in others mentioned in Table.

TABLE1: COMPARISON OF AREA IN THREE DESIGNS

64-bit	Design in Reference3	Design in reference10	Design in this paper
(number of transistors)	1556	2976	1406

Fig7 depicts the number of transistors in comparator mentioned in [10] and the proposed one . First bar shows total transistor count in [10] and second bar shows transistor count, for the proposed one.

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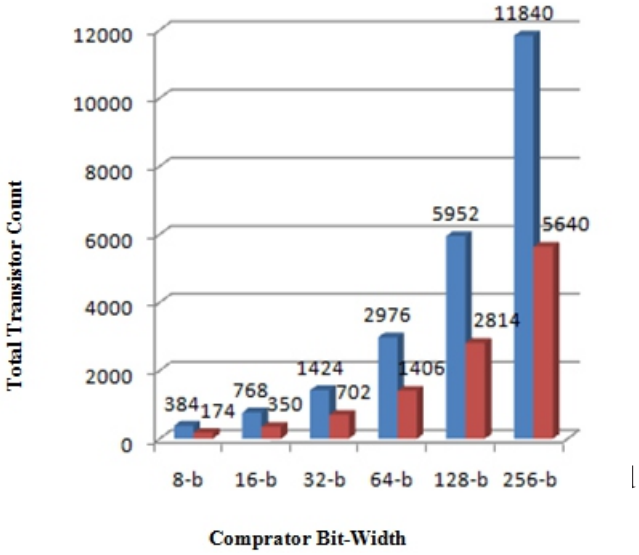
With respect to every word size transistor count reduction was more than 50% and the active transistor count in our proposed design is exactly 50% of our total transistor count for every word size. Since we have used Static CMOS Design style in which any one of either P-MOS or it's corresponding N-MOS will be on and vice-versa. This will be beneficial with respect to the Dynamic Power consumption of the circuit and this is one of the power consumption of CMOS along with Static power consumption and Short circuit power consumption.



V.CONCLUSION:

Area is one of the important design constraint as it is proportional to the cost of the design. Since our design has less number of transistors total number of active transistors will be less and it is like only 50% of total transistors will be active, so only 703 transistors will be active for 64-bit. In Saleh Abdel Hafeez comparator only 32% of the total transistors are active but 944 are the active transistors for 64-bit. In equal proportion active transistor count will be there for our proposed design as well as in Saleh Abdel Hafeez design for N-bit. we are able to design the comparator by using less number of transistors even though Static CMOS needs more number of transistors It shows an 64-bit comparator of the proposed technique only needs 1406 transistors, the technique which we presented can be easily extendable up to N-bit and some Design Techniques to be implemented to ensure that Delay is better.

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