

## An Interaction between High Step-Up Dc To Dc Converter and Fuel Cells in Power System



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**ABSTRACT:**

This paper explores a novel Pulse width Modulation (PWM) plan for two-stage interleaved support converter with voltage multiplier for energy component power framework by joining Alternating Phase shift(APS) control and conventional interleaving PWM control. The APS control is utilized to decrease the voltage weight on switches in light load while the conventional interleaving control is utilized to keep better execution in overwhelming burden. The limit condition for swapping amongst APS and customary interleaving PWM control is inferred. In light of the previously mentioned examination, a full power range control consolidating APS and conventional between leaving control is proposed. Misfortune breakdown investigation is additionally given to investigate the productivity of the converter. At long last, it is confirmed by test comes about.

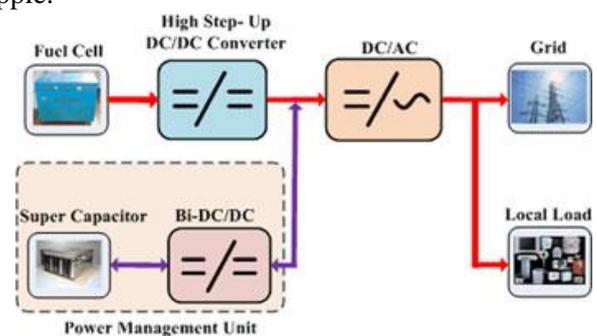
**Index Terms:**

Boost converter, fuel cell, interleaved, loss break-down, and voltage multiplier.

**I. INTRODUCTION:**

With expanding worry about vitality and environment, it is important to investigate the renewable vitality including wind power, sun oriented, energy component, and so on. Energy unit is one of promising decisions because of its focal points of zero discharge, low commotion, higher force thickness, and being effortlessly modularized for compact force sources, electric vehicles, conveyed era frameworks, and so on [1].

The matrix associated power framework in view of energy component is appeared in Fig. 1. For a regular 10-kW proton trade layer power module, the yield voltage is from 65 to 107 V. In any case, the info voltage of the three stage dc/air conditioning converter should be around 700 V; the voltage increase of the dc/dc converter between energy unit and the dc/air conditioning converter will be from 6 to 11 V. A high stride up dc/dc converter is required for the framework as appeared in Fig. 1. The dc/dc converter will produce a high recurrence info current swell, which will diminish the life time of the energy unit stack [2]–[4]. Furthermore, the hydrogen vitality usage diminishes with expanding the present swell of the energy component stack yield [5]. Along these lines, the dc/dc converter for the framework as shown in Fig. 1 should have high step-up ratio with minimum input current ripple.

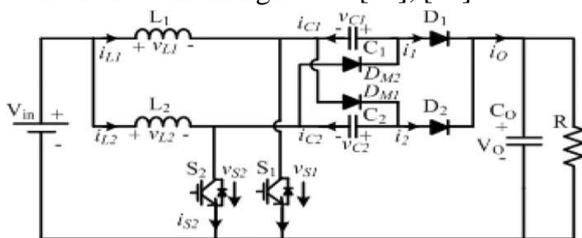


**Fig.1.Grid-connected power system based on Fuel cell**

High stride up proportion can be accomplished by joining established support converter with exchanged inductors [6], coupled inductors [7]–[9],

High-recurrence transformer [10], or exchanged capacitor [11]–[14], [19]. They can get high stride up proportion with high effectiveness, low-voltage push, and low electromagnetic obstruction. Keeping in mind the end goal to decrease yield energy component stack yield mongrel rent swell or the dc/dc converter information current swell, either a detached channel [15] or dynamic channel [5] can be utilized, be that as it may, this will expand the many-sided quality of the framework. Truth be told, interleaving the dc/dc converter can diminish the info current swell of the dc/dc converter [16]. An interleaved support converter with volt-age multiplier was proposed in [13], [14]. Its voltage addition was expanded up to  $(M + 1)$  times ( $M$  is the quantity of the voltage multiplier) of the established help converter with the same obligation cycle  $D$  and lower voltage stress. Furthermore, it has lower information current swells and yield voltage swells in contrast with the traditional help converter. The interleaving help converter with voltage multipliers is appeared in Fig. 2.

The converter shown in Fig. 2 can achieve low-voltage stress in the power devices, which increases the conversion efficiency. However, this is only true in overwhelming burden when the voltage anxiety of the force gadgets may increment when it works in irregular conduction mode (DCM) [17], which happens when energy component just supplies a light nearby load as appeared in Fig. 1. For this situation, higher voltage power gadgets should be utilized, and hence its expense and power misfortune will be expanded. These creators proposed a new heartbeat width balance (PWM) control technique, named as substituting stage shift (APS), to defeat the issue when the converter works in light load [17], [18].

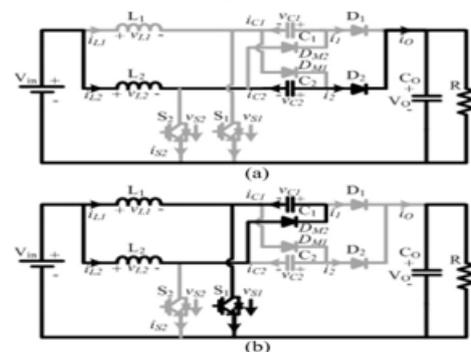


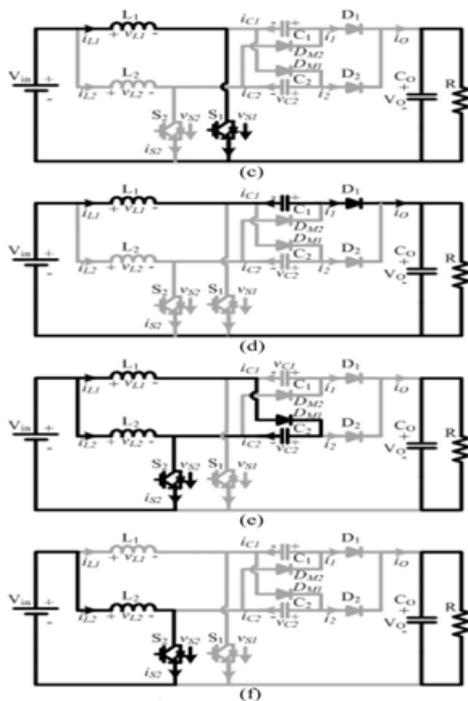
**Fig. 2. Structure of two-phase interleaved boost converter with voltage multiplier [13], [14].**

A new pulse width modulation (PWM) control method, named as alternating phase shift (APS), to overcome the problem when the converter operates in light load [17], [18]. This paper examines a novel PWM plan for two-stage interleaved support converter with voltage multiplier for energy component power framework by consolidating APS and conventional interleaving PWM control. The APS control is utilized to lessen the voltage weight on switches in light load while the conventional interleaving control is utilized to keep better execution in substantial burden. The limit condition for swapping amongst APS and customary interleaving PWM control is inferred. Taking into account the previously mentioned examination, a full power range control joining APS and customary interleaving control is proposed. Misfortune breakdown examination is likewise given to investigate the proficiency of the converter. At long last, it is confirmed by exploratory results

**II. BOUNDARY CONDITION ANALYSIS WITH TRADITIONAL INTERLEAVING CONTROL FOR LOW POWER OPERATION**

It is accepted that all parts in the converter are perfect, both capacitor  $C1$  and  $C2$  are sufficiently huge, and obligation cycle is under 0.5. The operation of an exchanging cycle of the converter can be separated into six phases at limit condition which the voltage weight on switch will be bigger than half of the yield voltage with customary interleaving control, as shown in Fig. 3. Typical theoretical waveforms at boundary condition are shown in Fig. 4.





**Fig. 3. Stages at boundary condition. (a) First stage ( $t_0, t_1$ ), (b) second stage( $t_1, t_2$ ), (c) third stage ( $t_2, t_3$ ), (d) fourth stage ( $t_3, t_4$ ), (e) fifth stage ( $t_4, t_5$ ), (f) sixth stage ( $t_5, t_6$ )**

**1) First Stage ( $t_0, t_1$ ):** At the moment of  $t_0$ , both switch  $S_1$  and  $S_2$  are off, the energy stored in the inductor  $L_2$  and capacitor  $C_2$  in previous stage are transferred to the out-put capacitor  $C_o$  through  $D_2$  as shown in Fig. 3(a). The voltage stress on switch  $S_1$  is the input voltage  $V_{in}$ , and the voltage stress on switch  $S_2$  is  $(V_o - V_{C2})$ , where  $V_o$  is the output voltage and  $V_{C2}$  is the voltage of capacitor  $C_2$ .

**2) Second Stage ( $t_1, t_2$ ):** Right now off1, the switch  $S_1$  is turned ON, the inductor  $L_1$  begins to store vitality from zero as appeared in Fig. 3(b). Meanwhile, if  $(V_{C1} + V_{C2}) < V_o$ , where  $V_{C1}$  is the capacitor  $C_1$  voltage, the diode  $D_2$  will be killed and the diode  $D_{M2}$  will be turned ON; along these lines, the vitality in the inductor  $L_2$  will be exchanged to the capacitor  $C_1$ . In the event that there is sufficient vitality in the inductor  $L_2$ ,  $V_{C1}$  will be charged to the accompanying state:  $V_{C1} + V_{C2} \geq V_o$ . At that point, the diode  $D_2$  will be turned ON once more, which is appeared in Fig. 5. In the

event that there is insufficient vitality to charge  $V_{C1}$  to  $(V_o - V_{C2})$ , then it will go to the Third Stage as appeared in Fig. 3(c). On the off chance that the vitality in the inductor  $L_2$  is simply released to zero and  $V_{C1} + V_{C2} = V_o$  toward the end of the stage, then we say that the circuit works in the limit condition state. Amid the stage, the voltage weight on switch  $S_2$  is  $V_{C1}$ .

**3) Third Stage ( $t_2, t_3$ ):** At the moment of  $t_2$ , the current in the inductor  $L_2$  just falls to zero, all the diodes are in off state and the inductor  $L_1$  is in charging state until the switch  $S_1$  is turned OFF at the moment of  $t_3$ . The voltage stress on switch  $S_2$  is  $V_{in}$ . At the end of this stage, the current in the inductor  $L_1$  comes to the peak value  $I_{L1P}$ , and

$$I_{L1P} = \frac{V_{in} D_m T_S}{L} \quad (1)$$

Where  $V_{in}$  is the input voltage,  $L$  is the inductance of  $L_1$  and  $L_2$ ,  $D_m$  is the duty cycle at boundary condition, and  $T_S$  is the switching period.

**4) Fourth Stage ( $t_3, t_4$ ):** Right now of  $t_3$ , switch  $S_1$  and  $S_2$  are in off state, the vitality in the inductor  $L_1$  and the capacitor  $C_1$  will be exchanged to the yield capacitor  $C_o$  through the diode  $D_1$ , which is like First Stage. In this stage, the voltage weight on switch  $S_1$  is  $(V_o - V_{C1})$ , and the voltage weight on switch  $S_2$  is  $V_{in}$ . Toward the end of this stage, the current in the inductor  $L_1$  declines to be  $I_{L1M}$

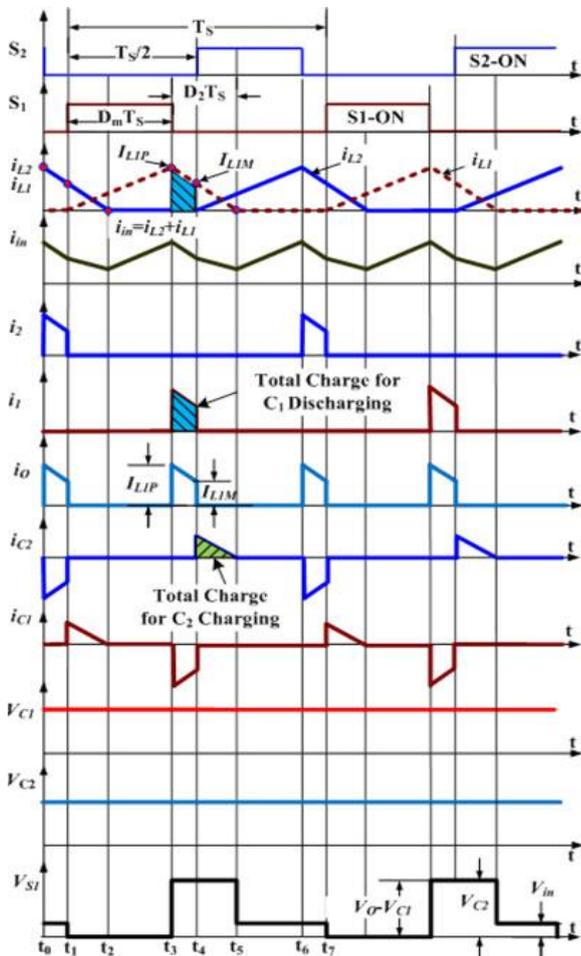
$$I_{L1M} = I_{L1P} - \frac{V_o - V_{C1} - V_{in}}{L} (0.5 - D_m) T_S. \quad (2)$$

**5) Fifth Stage ( $t_4, t_5$ ):** Right now of  $t_4$ , the switch  $S_2$  is turned ON and the inductor  $L_2$  begins to store vitality. This stage is like the Second Stage. In this stage, the voltage weight on switch  $S_1$  is  $V_{C2}$ . Toward the end of this stage, the current in the inductor  $L_1$  declines to zero from  $I_{L1M}$ . What's more, hence

$$I_{L1M} - \frac{V_{C2} - V_{in}}{L} (D_2 - 0.5 + D_m) T_S = 0 \quad (3)$$

Where  $D_2$  is the duty cycle as shown in Fig. 4.

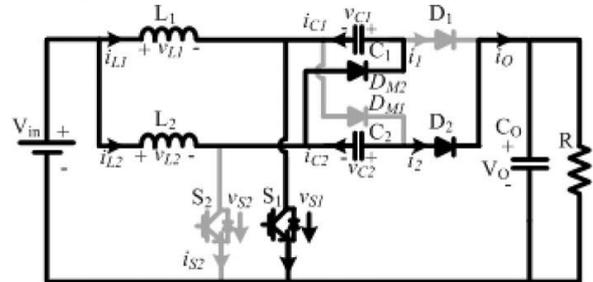
**6) Sixth Stage ( $t_5, t_6$ ):** At the moment of  $t_5$ , the current in the inductor  $L_1$  decreases to zero. All the diodes are in off state and the inductor  $L_2$  is in charging state until the stage comes to the end at the moment  $t_6$ . A new switching period will begin with the next *First Stage*.



**Fig. 4. Main theoretical waveforms at boundary condition.**

From the aforementioned analysis, the voltage sum of capacitor  $C_1$  and  $C_2$  will be  $V_0$  at boundary condition. If it is less than  $V_0$ , the voltage stress on switch  $S_1$  and  $S_2$  will be larger than  $V_0/2$ , because the voltage stress

on switch  $S_1$  is  $(V_0 - V_{C1})$  during the *Fourth Stage* and the voltage stress on switch  $S_2$  is  $(V_0 - V_{C2})$  during the *First Stage*.



**Fig. 5. One stage above boundary condition**

The average value of the output current  $i_o$  is equal to the dc component of the load current  $V_0/R$ , then

$$\begin{aligned} \frac{V_0}{R} &= \frac{1}{T_S} \int_0^{T_S} i_o dt = \frac{1}{T_S} \int_0^{T_S} (i_1 + i_2) dt \\ &= \frac{1}{T_S} \int_0^{T_S} i_1 dt + \frac{1}{T_S} \int_0^{T_S} i_2 dt. \end{aligned}$$

Considering the same parameters of the circuit in two phases as shown in Fig. 2, therefore

$$\frac{1}{T_S} \int_0^{T_S} i_1 dt = \frac{1}{T_S} \int_0^{T_S} i_2 dt. \quad (5)$$

By combining (4) and (5), it is derived

$$\begin{aligned} \frac{V_0}{R} &= \frac{2}{T_S} \int_0^{T_S} i_1 dt = \frac{2}{T_S} \int_{t_3}^{t_4} i_1 dt \\ &= \frac{2}{T_S} \cdot \left[ \frac{1}{2} (I_{L1P} + I_{L1M}) (0.5 - D_m) T_S \right] \\ &= (I_{L1P} + I_{L1M}) (0.5 - D_m) \end{aligned} \quad (6)$$

At the boundary condition, the diode  $D_2$  ( $D_1$ ) approaches the conduction state during the *Second Stage* (*Fifth Stage*), which is shown in Fig. 5. The following equation can be obtained

$$V_{C1} + V_{C2} = V_0. \quad (7)$$

Considering both capacitors  $C_1$  and  $C_2$  are large enough, average voltage of the capacitor will keep equal. Otherwise, the converter will not operate at boundary condition, therefore

$$V_{C1} = V_{C2} = (1/2) V_0. \quad (8)$$

By substituting (1) and (8) into (2), the current  $I_{L1M}$  can be derived

$$I_{L1M} = \frac{V_{in} - V_O/2 + V_O \cdot D_m}{2L} T_S \quad (9)$$

As shown in Fig. 4, the total discharge of capacitor  $C_1$  between  $t_3$  and  $t_4$  is

$$Q_{C1} = \int_{t_3}^{t_4} i_{L1} dt = \frac{1}{2} (I_{L1P} + I_{L1M}) (0.5 - D_m) T_S \quad (10)$$

The total charge of capacitor  $C_2$  between  $t_4$  and  $t_5$  is

$$Q_{C2} = \int_{t_4}^{t_5} i_{L1} dt = \frac{1}{2} I_{L1M} (D_2 - 0.5 + D_m) T_S \quad (11)$$

According to the previous analysis, the total discharge of  $C_1$  is equal to the total charge of capacitor  $C_2$  at boundary condition. Therefore, there will be

By combining (10), (11), and (12), the following can be derived

$$D_2 = (0.5 - D_m) \left( \frac{I_{L1P}}{I_{L1M}} + 2 \right) \quad (13)$$

By combining (3) and (6) and then substituting (1), (9), and (13) into them, the boundary condition can be derived as

$$\begin{cases} K = K_{crit} = \frac{n - z}{2n(n - \sqrt{2})^2} & (a) \\ D_m = \frac{n - 2}{2(n - \sqrt{2})} & (b) \end{cases} \quad (14)$$

Where  $n$  is the voltage addition of the converter ( $n = V_O/V_{in}$ ), and  $K$  is the parameters of the circuit and  $K = 2L/(R \times TS)$ . The limit requirement with conventional interleaving control chose by (14) is appeared in Fig. 6. The limitation incorporates two sections: obligation cycle  $D$  and the circuit parameters  $K = 2L/(R \times TS)$ . As the exchanging time frame  $TS$  and the information inductor  $L$  are planned at ostensible operation in consistent conduction mode (CCM), the limitation is controlled by obligation cycle  $D$  and the heap  $R$ . The motivation behind why there are two sections in the limit requirement is that the obligation cycle  $D$  fluctuates with the heap when the

converter works in DCM. For a given application, the voltage increase of the dc/dc converter is resolved. And after that, the base obligation cycle that can keep up low-voltage stress in fundamental force gadgets with conventional interleaving control will be given by (14)- (b) and as appeared in Fig. 6(a). At the same least obligation cycle, the converter works at limit condition when the circuit parameters  $K = 2L/(R \times TS)$  satisfy (14)-(a) and as shown in Fig. 6(b). At the point when the converter works over the limit condition, the circuit parameters are in Zone An of Fig. 6(b), i.e.,  $K > K_{crit}$ , the converter could accomplish split voltage weight on switches with conventional interleaving control with the obligation cycle over the strong red line as appeared in Fig. 6(a). While diminishing the heap to the strong red line at limit condition in Fig. 6(b), i.e.,  $K = K_{crit}$ , the obligation cycle of the converter will be

$$Q_{C1} = Q_{C2} \quad (12)$$

diminished to the strong red line in Fig. 6(a). While diminishing the heap further in Zone B in Fig. 6(b), i.e.,  $K < K_{crit}$ , the obligation cycle will be diminished further to be littler than the base obligation cycle that keeps up low-voltage weight on switches with conventional interleaving control. At that point, the APS control ought to be utilized to accomplish split voltage weight on switches in Zone B [17], [18]. In our 1-kW model plan, the information voltage of the converter is 86–107 V, and the yield voltage of the converter is 700 V. The voltage addition will differ from  $n_1 = 6.54$  to  $n_2 = 8.14$ , and afterward the circuit parameters at limit conditions  $K_{crit}$  will shift from  $K_{crit1} = 0.013$  to  $K_{crit2} = 0.0083$  as appeared in Fig. 6(b), the obligation cycle will shift from  $D_{m1} = 0.443$  to  $D_{m2} = 0.456$  with a specific end goal to keep up the steady yield voltage. At the point when the circuit parameters  $K = 2L/(R \times TS)$  are underneath the strong red line from point a to point b at various voltage pick up as appeared in Fig. 6(b), the obligation cycle will be diminished further to be not exactly the strong red line from  $D_{m1} = 0.443$  to  $D_{m2} = 0.456$  as appeared in Fig. 6(a), and after that the voltage weight on switches will be expanded at this heap.

Keeping in mind the end goal to accomplish the split voltage weight on switches at this heap, APS control is required.

### III. CONTROL SCHEME OF ALL POWER RANGE WITH APS AND TRADITIONAL INTERLEAVING CONTROL

As indicated by the guideline of APS [17], APS control is proposed to take care of the light load issue with obligation cycle under 0.5 as appeared in Fig. 7(a). With the heap expanding, the obligation cycle will be expanded too. At the point when the obligation cycle is in-wrinkled to 0.5, the APS control will be adjusted to be customary interleaving control with split exchanging recurrence as appeared in Fig. 7(b). As indicated by past examination as appeared in Fig. 6, the base obligation cycle to accomplish low-voltage weight on switches with customary interleaving control is under 0.5. Along these lines, it is conceivable to join both APS control and customary interleaving control to control the converter for full power range operation.

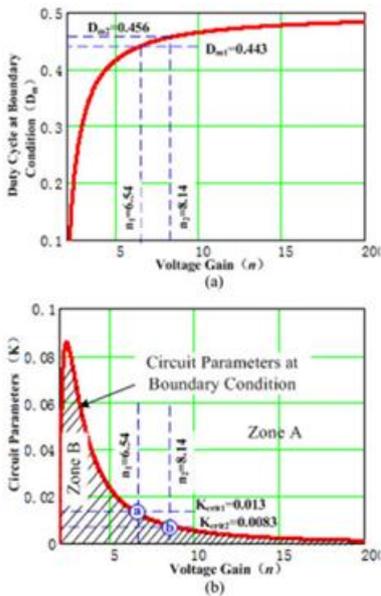


Fig. 6. Boundary constraint varies with voltage gain. (a) Duty cycle at boundary condition varies with voltage gain, (b) circuit parameters at boundary condition varies with voltage gain.

Considering the variety of the information voltage from 86 to 107 V for 1-kW power device operation and the yield voltage of the converter 700 V, the base obligation cycle of conventional interleaving control fluctuates from  $D_{m1} = 0.443$  to  $D_{m2} = 0.456$ . The control plan is appeared in Fig. 8. The obligation cycle is separated into three zones:  $D < D_{m1}$ ,  $D > D_{m2}$ , and  $D_{m1} \leq D \leq D_{m2}$ . In the primary region, i.e.,  $D < D_{m1}$ , APS control will be utilized in light of the fact that customary interleaving control can't be powerful to maintain low-voltage weight on switches. In the second region, i.e.,  $D > D_{m2}$ , conventional interleaving control will be utilized. In the third range, i.e.,  $D_{m1} \leq D \leq D_{m2}$ , either APS control or conventional interleaving control might be utilized.

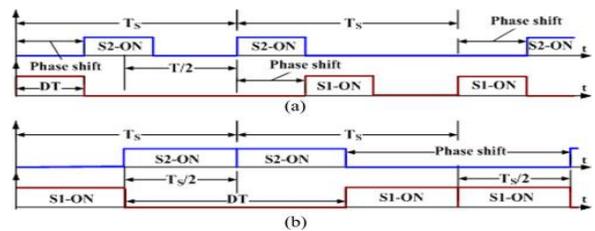


Fig. 7. PWM waveform of APS with  $D < 0.5$  and  $D = 0.5$ . (a)  $D < 0.5$ , (b)  $D = 0.5$ .

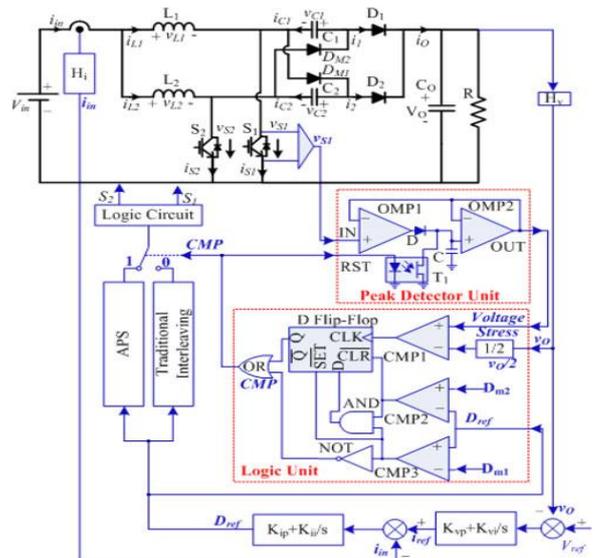


Fig. 8. Block diagram of the converter with the control scheme of all power range.

In the first area ( $D < D_{m1}$ ) with APS control and the second area ( $D > D_{m2}$ ) with traditional interleaving control, the capacitor voltage is half of the output voltage. Therefore, the switches voltage stress is clamped to half of the output volt-age [17], [18]. The swapping between the APS control and customary interleaving control in the zone  $D_{m1} \leq D \leq D_{m2}$  is accomplished by recognizing the voltage anxiety of the switch S1 as appeared in Fig. 8. At the point when the voltage anxiety of the switch S1 is higher than half of the yield voltage, the control is changed from interleaving control to APS control. In the event that the conventional interleaving control is at first utilized as a part of the second zone ( $D_{m1} \leq D \leq D_{m2}$ ) and once the switch S1 voltage anxiety is bigger than half of the yield voltage, the rationale unit yield CMP in Fig. 8 will be changed to  $CMP = 1$  and APS control will be empowered. The previously mentioned capacity for swapping between the APS and conventional interleaving control is accomplished by the Logic Unit as appeared in Fig. 8, and the operational rule of the Logic Unit is appeared in Table I.

In the event that APS control mode is utilized (i.e.,  $CMP = 1$ ), the pick coupler transistor T1 is turned ON, the voltage of capacitor C in the pinnacle indicator unit is resettled and the pinnacle finder unit is disabled. In the event that the customary interleaving control mode is utilized (i.e.,  $CMP = 0$ ), the pick coupler transistor T1 will be killed, and the crest locator unit is empowered and used to recognize the voltage anxiety of switch S1. Keeping in mind the end goal to accomplish better element execution operation, double circle control is embraced as appeared in Fig. 8, in which the inward current circle is to control the info inductor current while the external voltage circle is to control the yield voltage.  $K_{ip}$  and  $K_{ii}$  are the PI controller parameters of the inward current loop, while  $K_{vp}$  and  $K_{vi}$  are the PI controller parameters of the external voltage circle.

**TABLE I: OPERATIONAL PRINCIPLE OF THE LOGIC UNIT IN FIG. 8**

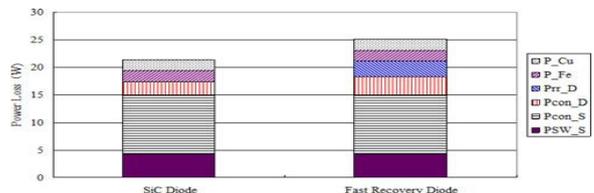
$v_{S1} > 0.5v_o$	$D_{ref} > D_{m1}$	$D_{ref} < D_{m2}$	Control Method
X	1	0	Traditional interleaving control
X	0	1	APS control
0	1	1	Keep the previous control mode
1	1	1	Swap from traditional interleaving control to APS control and stay in APS control until $D_{ref} > D_{m2}$

In our 1-kW prototype design, the circuit parameters are as follows,  $V_{in} = 100$  V,  $V_o = 700$  V,  $C_1 = C_2 = 40 \mu F$ ,  $C_o = 195 \mu F$ ,  $L_1 = L_2 = 1158 \mu H$ ,  $T_s = 100 \mu s$ ,  $H_v = 20.56$ ,  $H_i = 698.298$ , where  $H_v$  is the output voltage feedback coefficient and  $H_i$  is the input current feedback coefficient. The bandwidth of the inner current loop is 1 kHz with PI parameters as follows:  $K_{ip} = 0.061$ ,  $K_{ii} = 63.67$ .

**TABLE II: MAIN CHOICES OF POWER DEVICES**

Symbol	Voltage Stress	Product Type
$S_1, S_2$	350V	IKW20N60H3
$D_1, D_2$	350V	DSEP15-06A IDW16G65C5
$D_{M1}, D_{M2}$	700V	DSEP15-12CR IDH15S120

The bandwidth of the outer voltage loop is 100 Hz with PI parameters as follows:  $K_{vp} = 32.103$ ,  $K_{vi} = 2017$ .



**Fig. 9. Loss distribution of the converter with IGBT (IKW20N60H3) in CCM ( $r = 0.37$ ) at 1 kW. (SiC Diode: IDH15S120 and IDW16G65C5, Fast Recovery Diode: DSEP15-12CR and DSEP15-06A).**

**IV. LOSS BREAKDOWN ANALYSIS:**

As the expense of energy unit is still high, it is essential to expand the proficiency of the force converter for power device based force framework keeping in mind the end goal to diminish its operation cost and increment the use of fills. In this manner, misfortune breakdown examination is required. The ostensible force of the converter is 1 kW for misfortune separate investigation and model setup, and the information voltage is 100 V while the yield

voltage is 700 V with exchanging recurrence  $f_s=10$  kHz. The force gadgets utilized are appeared as a part of Table II. The converter could work in CCM at ostensible burden with info current swell proportion  $r = 0.37$  and the inductor  $L_1$  and  $L_2$  is 1158  $\mu$ H. The inductor is worked with the formless center. As appeared in Fig. 9, the primary parts of the misfortune are the conduction misfortune ( $P_{con S}$ ) and exchanging misfortune ( $PSW_S$ ) of the IGBT. With the quick recuperation diodes (DSEP15-12CR and DSEP15-06A) and IGBT (IKW20N60H3), the effectiveness of the converter at ostensible burden can be 97.49%. As there is no converse recuperation misfortune ( $P_{rrD}$ ) in silicon carbide (SiC) diode, the productivity can be expanded to be 97.86% with SiC diode (IDH15S120 and IDW16C65C5) and IGBT (IKW20N60H3). The converter could likewise work in limit conduction mode (BCM) at ostensible burden with info current swell proportion ( $r = 0.6$ ) and the inductor  $L_1$  and  $L_2$  is 714.3  $\mu$ H. The inductor is worked with the nebulous center.

As appeared in Fig. 10, the fundamental parts of the misfortune additionally incorporate the conduction misfortune ( $P_{con S}$ ) of the IGBT. Contrasted and CCM as appeared in Fig. 9, there is no quick recuperation misfortune even with quick recuperation diodes in BCM. Be that as it may, the inductor misfortune including the center misfortune ( $P_{Fe}$ ) and the wire misfortune ( $P_{Cu}$ ) is expanded in BCM as the present swell is expanded from 0.37 to 0.6. In BCM, the effectiveness of the converter can be 97.09% with SiC diode and 97.06% with quick recuperation diode. Comparing Fig. 9 and Fig. 10, the efficiency of the converter with IGBT and fast recovery diode in CCM is a bit higher than that in BCM. In CCM, the efficiency of the converter with fast recovery diode is only 0.37% less than that with SiC diode. Therefore, we use IGBT and fast recovery diode in CCM for experiments.

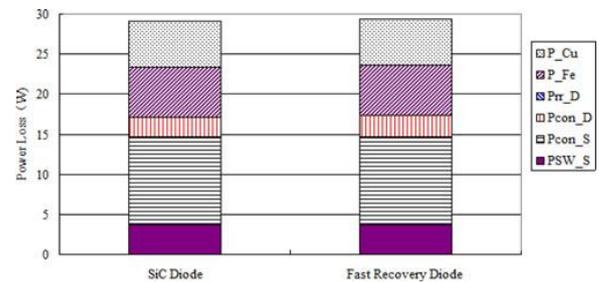


Fig. 10. Loss distribution of the converter with IGBT(IKW20N60H3) in BCM ( $r = 0.6$ ) at 1 kW. (SiC Diode: IDH15S120 and IDW16G65C5, Fast Recovery Diode: DSEP15-12CR and DSEP15-06A).



Fig. 11. Prototype of the 1-kW Converter with fuel cell and load.

## V. EXPERIMENTAL RESULTS

### A. Static Experiments

In order to verify the previous analysis, prototype is built as shown in Fig. 11. The circuit parameters are as follows,  $V_{in} = 100$  V,  $V_o = 700$  V,  $C_1 = C_2 = 40 \mu$ F,  $C_o = 195 \mu$ F,  $L_1 = L_2 = 1158 \mu$ H,  $T_s = 100 \mu$ s. The load at boundary condition is  $R_{BC} = 2023 \Omega$  and  $K_{crit} = 0.011$  at boundary condition according to (14), the duty cycle  $D_m$  at boundary condition is 0.448. The experimental results at boundary condition are shown in Fig. 12, which are in accordance with the theoretical waveform in Fig. 4. The experimental results are given to verify the previous analysis. With  $R = 478 \Omega$ , the output power is a bit greater than 1 kW, and  $K = 0.048 > K_{crit} = 0.011$ , the converter is designed to operate in Zone A of Fig. 6(b), and the traditional interleaving control can maintain the voltage stress on switches with half of the output voltage (i.e., 350 V) as shown in Fig. 13. With  $R = 1658 \Omega$ , i.e.,  $K = 0.014 > K_{crit} = 0.011$ , the converter will continue operating in Zone A of Fig. 6(b), and the voltage stress on switches is still 350 V,

which is about the half of the output voltage as shown in Fig. 14

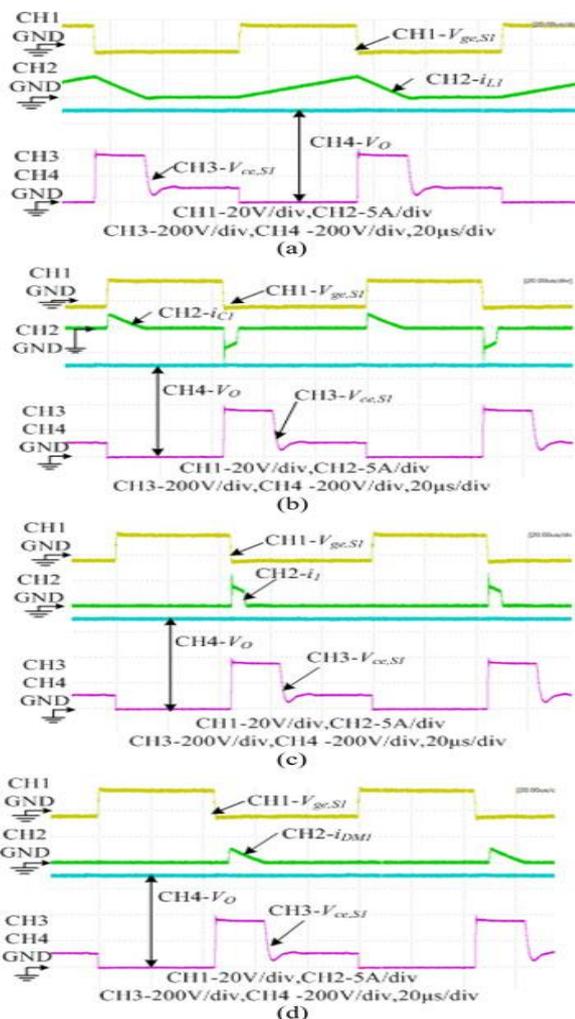


Fig. 12. Experimental results at boundary condition with traditional interleaving control ( $L = 1158 \mu\text{H}$ ,  $R = 2023 \Omega$ , and  $D = 0.448$ ). (a) CH1- $S_1$  Driver Voltage, CH2- $L_1$  Current, CH3- $S_1$  Voltage Stress, CH4-Output Voltage, (b) CH1- $S_1$  Driver Voltage, CH2- $C_1$  Current, CH3- $S_1$  Voltage Stress, CH4-Output Voltage, (c) CH1- $S_1$  Driver Voltage, CH2- $D_1$  Current, CH3- $S_1$  Voltage Stress, CH4-Output Voltage, (d) CH1- $S_1$  Driver Voltage, CH2- $D M_1$  Current, CH3- $S_1$  Voltage Stress, CH4-Output Voltage.

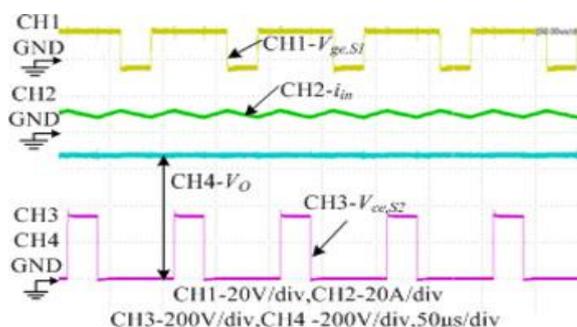


Fig. 13. Traditional interleaving control at nominal load ( $L = 1158 \mu\text{H}$  and  $R = 478\Omega$ ).

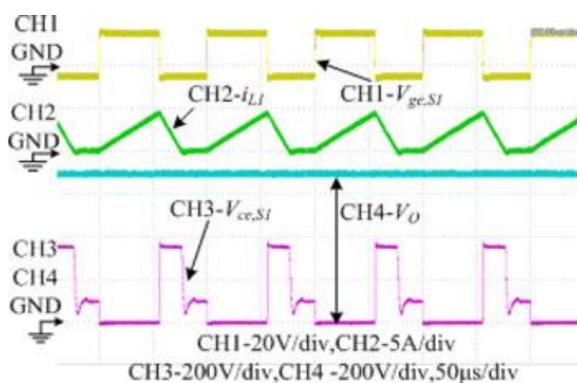


Fig. 14. Traditional interleaving control in Zone A ( $L = 1158 \mu\text{H}$  and  $R = 1658\Omega$ ).

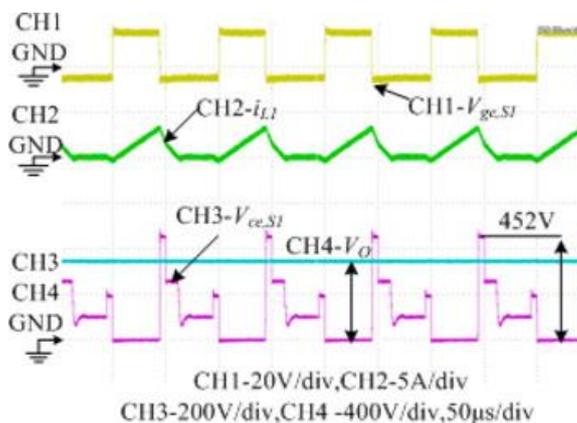


Fig. 15. Traditional interleaving control in Zone B ( $L = 1158 \mu\text{H}$  and  $R = 3460\Omega$ ).

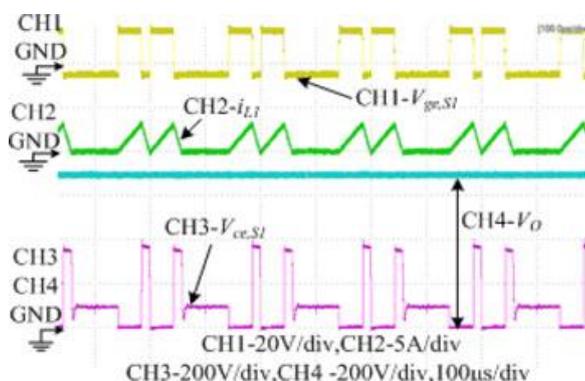


Fig. 16. APS control in Zone B ( $L = 1158 \mu\text{H}$  and  $R = 3460 \Omega$ ).

However, when decreasing the load to be  $3460 \Omega$ , i.e.,  $K = 0.0067 < K_{\text{crit}} = 0.011$ , the converter will operate in Zone B of Fig. 6(b). Here for comparison, two control methods are used and the results are shown in Fig. 15 and Fig. 16, respectively. In Fig. 15, traditional interleaving control is used, and we can see the voltage stress on the switch is  $452 \text{ V}$  which is higher than half of the output voltage. In Fig. 16, APS control is used, and we can see the voltage stress on the switch is  $350 \text{ V}$  which is about half of the output voltage. Therefore, it is effective to use APS control when the converter operates in Zone B. With the control scheme as shown in Fig. 8, more experiments are conducted to measure the voltage stress on power switches in all power range of the load. As shown in Fig. 17, the voltage stress follows the variation of the output voltage, and almost keeps half of the output voltage in all power range. The reason why the output voltage is not stable comes from the voltage ripple of  $20 \text{ V}$  in the output voltage.

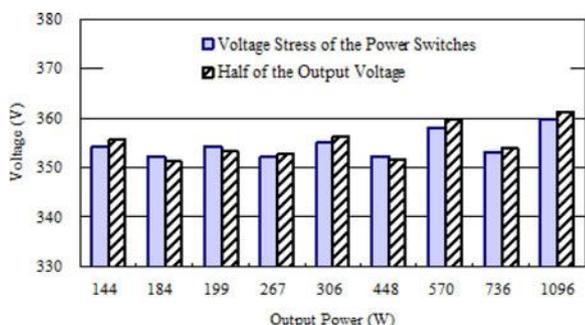


Fig. 17. Voltage stress on power switches in all power range of the load.

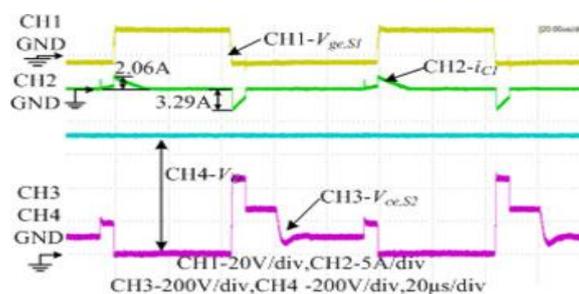


Fig. 18. Experimental results of current peak of capacitor  $C_1$  with traditional interleaving control under  $R = 3460 \Omega$

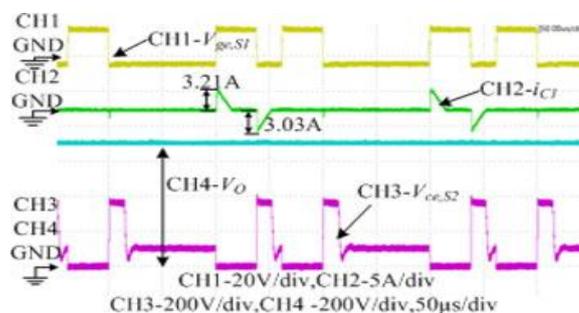


Fig. 19. Experimental results of current peak of capacitor  $C_1$  with APS control under  $R = 3460 \Omega$ .

As In any case, while diminishing the heap to be  $3460 \Omega$ , i.e.,  $K = 0.0067 < K_{\text{crit}} = 0.011$ , the converter will work in Zone B of Fig. 6(b). Here for examination, two control techniques are utilized and the outcomes are appeared in Fig. 15 and Fig. 16, individually. In Fig. 15, customary interleaving control is utilized, and we can see the voltage weight on the switch is  $452 \text{ V}$  which is higher than half of the yield voltage. In Fig. 16, APS control is utilized, and we can see the voltage weight on the switch is  $350 \text{ V}$  which is about portion of the yield voltage. Thusly, it is viable to utilize APS control when the converter works in Zone B. With the control plan as appeared in Fig. 8, more trials are directed to quantify the voltage weight on force switches in all force scope of the heap. As appeared in Fig. 17, the voltage stress takes after the variety of the yield voltage, and just about keeps half of the yield voltage in all force range.

The motivation behind why the yield voltage is not steady originates from the voltage swell of 20 V in the yield voltage.

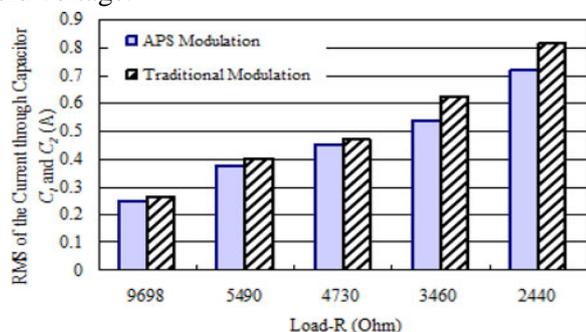


Fig. 20. Comparison on RMS of the current through capacitor (C<sub>1</sub> and C<sub>2</sub>) with different control method below boundary condition ( $R > 2023 \Omega$ ).

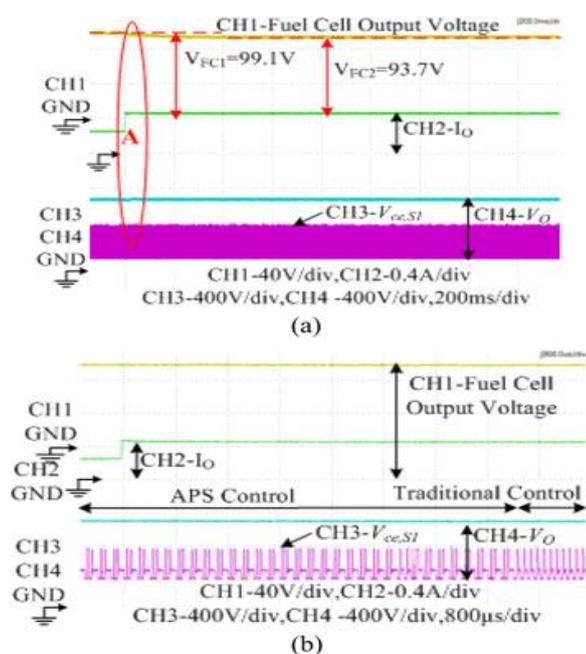


Fig. 21. Waveforms when load varies from 3478  $\Omega$  to 1658  $\Omega$  with fuel cell as input. (a) Waveforms when the load varies from 3478  $\Omega$  to 1658  $\Omega$ . (b) zoomed waveforms in Area A.

The C<sub>1</sub> and C<sub>2</sub> are designed with film capacitor with the part number is SHB-500-40-4 from EACO Capacitor, Inc., and its maximum RMS current is 19 A, which is much greater than the aforementioned current ripple.

### B. Dynamic Experiments

In order to test the dynamic performance of the converter with fuel cell as input, the converter is connected to the output of the PEMFC shown in Fig. 11. When the load varies from 3478  $\Omega$  to 1658  $\Omega$  as shown in Fig. 21, the output voltage of the fuel cell will varies from 99.1 to 93.7 V, the control scheme will swap from APS control to conventional interleaving control, the voltage anxiety of force switches keeps half of the yield voltage amid the time of burden variety, and the yield voltage of the converter keeps 700 V in stable operation under the two burden. At the point when the heap changes from 1658  $\Omega$  to 3478  $\Omega$  as appeared in Fig. 22, the yield voltage of the energy unit will differs from 93.7 to 99.1 V appropriately, the control plan will swap from customary interleaving control to APS control, and the voltage anxiety of force switches keeps half of the yield voltage also. Subsequently, the control plan proposed in this paper could accomplish split voltage weight on switches when swapping between conventional interleaving control and APS control.

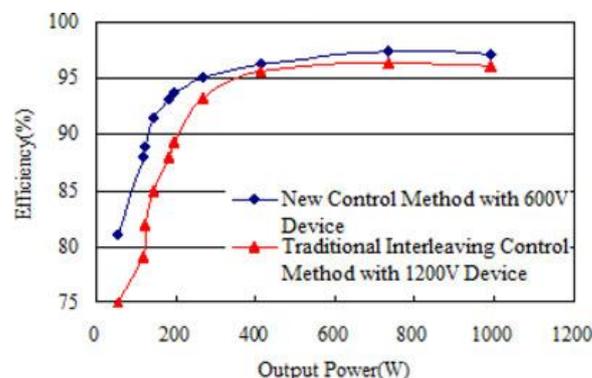
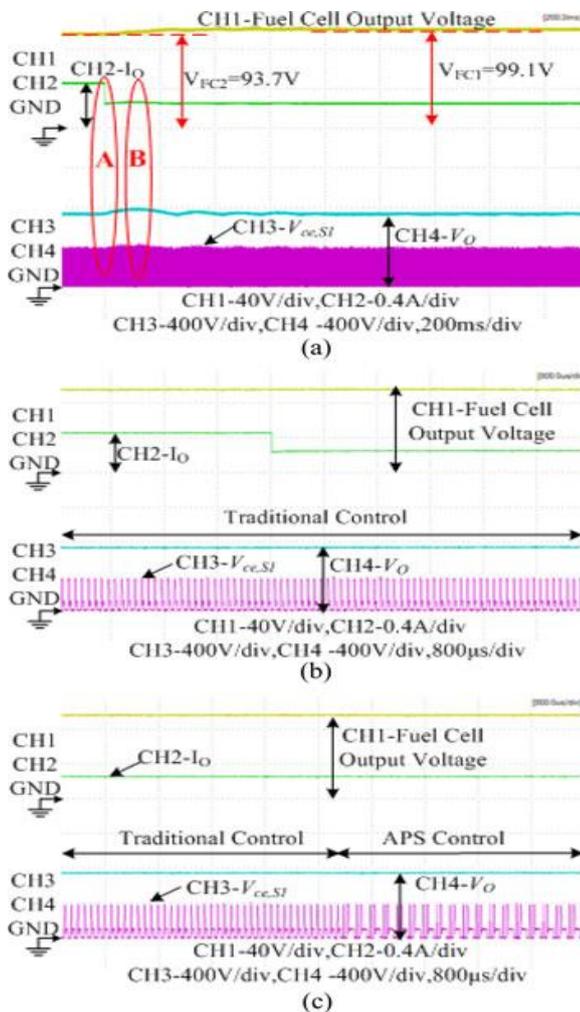


Fig. 23. Efficiency comparison of the converter with two control method. (Power device with new control method: DSEP15-12CR, DSEP15-06A and IKW20N60H3. Power device with traditional interleaving control method: DSEP15-12CR and IKW25N120H3).



**Fig. 22. Waveforms when load varies from 1658 Ω to 3478 Ω. Waveforms when load varies from 1658 Ω to 3478 Ω with fuel cell as input. (a) Waveforms when load varies from 1658 Ω to 3478 Ω, (b). (a) Waveforms when load varies from 1658 Ω to 3478 Ω with fuel cell as input, (b) Zoomed waveforms in Area A, (c) Zoomed waveforms in Area B.**

## VI. CONCLUSION:

The limit condition is inferred after stage investigation in this paper. The limit condition arranges the working states into two zones, i.e., Zone An and Zone B. The conventional interleaving control is utilized as a part of Zone A while APS control is utilized as a part of Zone B. Furthermore, the swapping capacity is accomplished by a rationale unit. With the proposed control conspire, the converter can accomplish low-voltage weight on

switches in all force scope of the heap, which is checked by test comes about.

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