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Interleaved Phase-Shift Full-Bridge Converter with Transformer Winding Series-Parallel Autoregulated (SPAR) Current Doubler Rectifier

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ABSTRACT:

The analysis and design guidelines for a two-phase in-terleaved phase-shift full-bridge converter with transformer winding series–parallel autoregulated current doubler rectifier are presented in this paper. The secondary windings of two transformers work in parallel when the equivalent duty cycle is smaller than 0.25 but in series when the duty cycle is larger than 0.25 owing to the series–parallel autoregulated rectifier. With the proposed rectify-ing structure, the voltage stress of the rectifier is reduced. Also, the interleaving operation reduces the output current ripple. A 1-kW prototype with 200–400-V input and 50-V/20-A output is built up to verify the theoretical analysis.

Index Terms:

Interleaved phase-shift full-bridge (PSFB) con-verter, rectifiers, series–parallel autoregulated.

I. INTRODUCTION:

The interleaved topologies are attractive in high-power application that calls for high power density and low-profile package. The interleaving technique alleviates the current rate of the semiconductor devices, and the shifting between two phases decreases the input and the output current ripples, which reduces the size of the input and output filters [1]–[4]. It also simplifies the thermal management by physically distributing the magnetic components and semiconductor devices in the whole system.

The phase-shift full-bridge (PSFB) converter is popular in medium- and high-power dc/dc applications. It has desirable features such as ZVS switching operation, high efficiency, and simple topology [5], [6]. Soft switching is achieved by utilizing the energy in the leakage inductance of the transformer and/or external current sources to charge and discharge the intrinsic ca-pacitances of the MOSFETs. High conversion efficiency, high power density, and low electromagnetic interference are easy

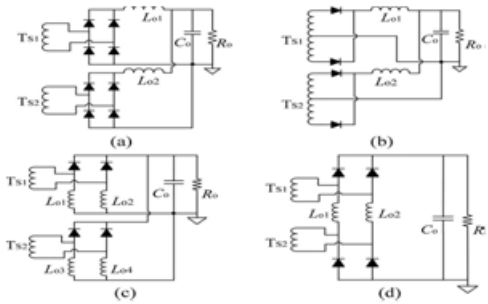

Fig. 1.Schematics of the secondary rectifiers in the two-phase PSFB converterapplication. (a) Full-bridge rectifier. (b) Center-tapped rectifier. (c) CDR.(d) SPAR CDR [26].

To be obtained by phase-shift control strategy and simple topol-ogy [5]–[8], [16]. The PSFB converter with better soft switch-ing performance [5]–[10], wider working range [11]–[14], and higher efficiency [15]–[18] attracts lots of attention in recent years.For the two-phase interleaved PSFB converter [19]–[23], there are several topologies available for the secondary recti-fier structures.

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The conventional rectifier structures such as full-bridge rectifier, center-tapped rectifier, and current doubler rectifier (CDR) are widely applied in various applications [24], [25]. Fig. 1 presents the schematics for existing rectifiers for the two-phase interleaved PSFB converter. Only the secondary windings of the transformers T_{s1} and T_{s2} are presented. Fig. 1(a) shows the full-bridge rectifier structure, which is desirable in high output voltage applications. Fig. 1(b) shows the center-tapped rectifier structure. There is only one device in the current-flowing path. However, the voltage stresses of the diodes are high. What is more is that the center-tapped winding structure is complex, which leads to low utilization of the transformer core. This rectifier is attractive in medium- and low-output-voltage appli-cation. The CDR in Fig. 1(c) is generally used in high-current low-voltage applications in which the current in the transformer winding is half of the load current and the structure of windings is simple. But two inductors are needed for each phase, and the interleaved rectifiers require too many inductors.

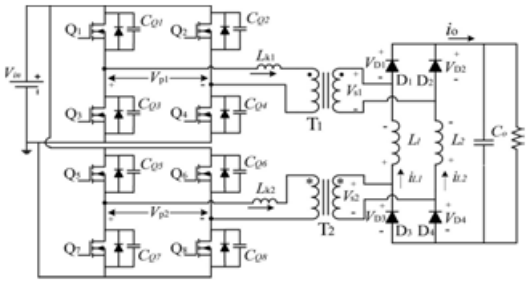

Fig. 2. Schematic of the interleaved PSFB converter with SPAR-CDR.

In order to reduce the voltage stresses of the rectifier devices and the secondary-side wingding count, a CDR with transformer winding series–parallel auto regulated (SPAR-CDR) based on the two-phase interleaved PSFB converter was proposed in [26] shown in Fig. 1(d). The proposed rectifier has the following ad-vantages compared to the conventional rectifiers: 1) the voltage stress of diodes can be reduced to around 50% compared with the center-tapped rectifier and the conventional CDR. Hence, low-voltage synchronous rectifier (SR) can be utilized to reduce the conduction loss and improve the efficiency; 2) the number of rectifier components and inductors are minimized; and 3) the secondary wingding count is reduced and the utilizing coefficient of the transformer core is improved. The schematic of the two-phase interleaved PSFB with SPARCDR is shown in Fig. 2. The operating principle has been introduced briefly in [26]. This paper emphasizes on the detailed analysis and design considerations. More experimental results are provided to verify the theoretical analysis and the design guidelines in this paper.

II. OPERATING PRINCIPLES

A. Brief Introduction of the Interleaved PSFB With SPAR-CDR

Two full bridges are adopted in the primary side. Phase 1 consists of the switches Q1–Q4 , transformer T1 , and diodes D1and D2 . Phase 2 consists of the switches Q5–Q8 , transformerT2 , and diodes D3 and D4 . Two phases are connected by the output inductances $L1$ and $L2$ and controlled in an interleaved manner. The detailed waveforms are presented in Figs. 3 and 4,where Φ is defined as the phase-shift angle between two phases and the duty cycle D is defined as the pulse width of midpoint voltage of each phase during one switching cycle. According to the relationship between primary duty cycle (D)and the phase-shift angle Φ ($\Phi = \pi/2$), the operation process in one switching cycle of the converter is divided into two cases. When the input voltage is low, the duty cycle D is larger than normalized phase-shift angle α ($\alpha = \Phi/2\pi$, case 1). When the input voltage is high, the converter enters into case 2, namely$<\alpha$. In order to understand the performance of the interleaved PSFB converter with SPAR-CDR, some assumptions are made to simplify the analysis:

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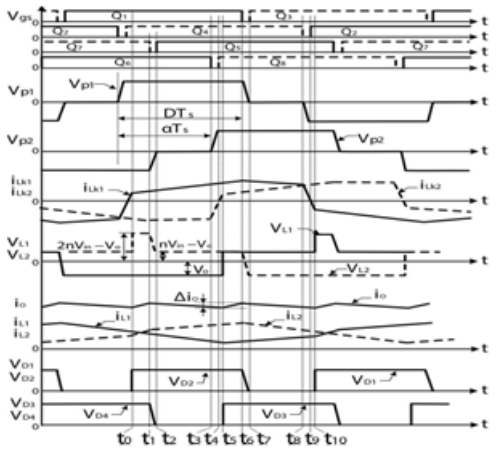

Fig. 3.Operating waveforms of the proposed converter in case 1.

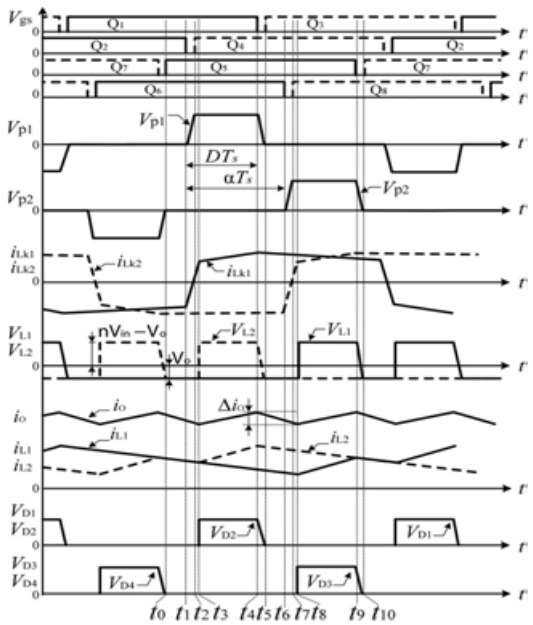

Fig. 4. Operating waveforms of the proposed converter in case 2

1) transformers are almost identical, which means $n_1 = n_2 = n$ (N_p:N_s=1:n), $L_{m1} = L_{m2}$, $L_{k1} = L_{k2}$;
2) switches consist of the junction capacitances (C_Q) and body diodes; other parasitic components and voltage drop caused by the turn-on resistance are ignored, the diodes of the secondary side are ideal;
3) the output filter capacitance is large enough such that the output voltage is constant during one switching cycle.

B. Operating Principle of the Interleaved PSFB Converter in One Switching Cycle

The operating modes of half switching cycle are presented according to different duty cycle cases.

Case 1 (input voltage is low and D > α): In this case, theinput voltage is low and the duty cycle D is larger than α. The operation during half switching cycle can be divided into ten modes; the key waveforms and the equivalent circuit of each mode are given in Figs. 3 and 5, respectively.

Mode 0 [t_0 –t_1]: At the beginning of this mode, Q_1, Q_4, Q_6,and Q_7 are ON, and energy is transferred to the load through transformers T_1 and T_2 . Since the secondary voltage of T_1 is positive while T_2 is negative, D_1 and D_3 are conducting, which makes T_1 , T_2 , and L_2 in series and L_1 connects to V_o directly. Therefore, primary-side currents $i_{L\,k1}$ and $i_{L\,k2}$ are both ni_{L2} , which are reflected from secondary-side inductance L_2 . During this period, L_1 is discharged by the voltage V_o and L_2 is charged by the voltage $2nV_{in}-V_o$. The voltages across the diodes D_2 and D_4 are both nV_{in} . This mode ends when Q_7 turns OFF.

Mode 1 [t_1 –t_2]: At t_1, switch Q_7turns OFF and $Q_1$and $Q_4$are ON. Parasitic capacitances $C_{Q\,7}$ and $C_{Q\,5}$ are discharged and charged, respectively, by the reflected inductance of L_2 . Because the inductance L_2 is large enough and the switching transition is rapid, the inductance can be seen as a current source during this switching transition. Hence, the primary current $i_{L\,k2}$ can be treated as a constant current source in this interval and it charges the parasitic capacitances of the MOSFETs. When the drain to source of Q_7 ($V_{CQ\,7}$) reaches V_{in} at t_2 , this mode ends.

Mode 2 [t_2 –t_3]: When the voltage $V_{CQ\,5}$decreases to zeroat t_2 , body diode $D_{Q\,5}$ turns ON and takes over the current $i_{L\,k2}$. The switch Q_5turns ON after $t_2$and achieves ZVS-on. Inthis interval, Q_5 and Q_6 are both conducting and current $i_{L\,k2}$ is circulating in primary

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side. The current $i_{L\,k1}$ still equals to in this interval.
The transformer winding is short circuited, and the diodes D_3 and D_4 are both conducting. The voltage across D_2 is nV_{in} . The current of L_2 increases with the slope $(nV_{in}-V_o)/L_2$, while the current in L_1 decreases with the slope

Mode 3 [t_3 –t_4]: Q_6turns OFF at t_3. The circulating primarycurrent begins to charge $C_{Q\,6}$ and discharges $C_{Q\,8}$, respectively. When $V_{CQ\,8}$ reaches zero at t_4 , the ZVS-on condition for Q_8 can be achieved, that is the soft switching of the lagging leg of PSFB. The currents in D_3 and D_4 begin commutating at t_3 . The secondary side of the transformer T_2 is short circuited. The simplified equivalent circuit of this mode is shown in Fig. 5(d). It can be simplified into a resonant circuit between L_{k2} and equivalent parasitic capacitances. When $V_{CQ\,8}$ reaches zero at

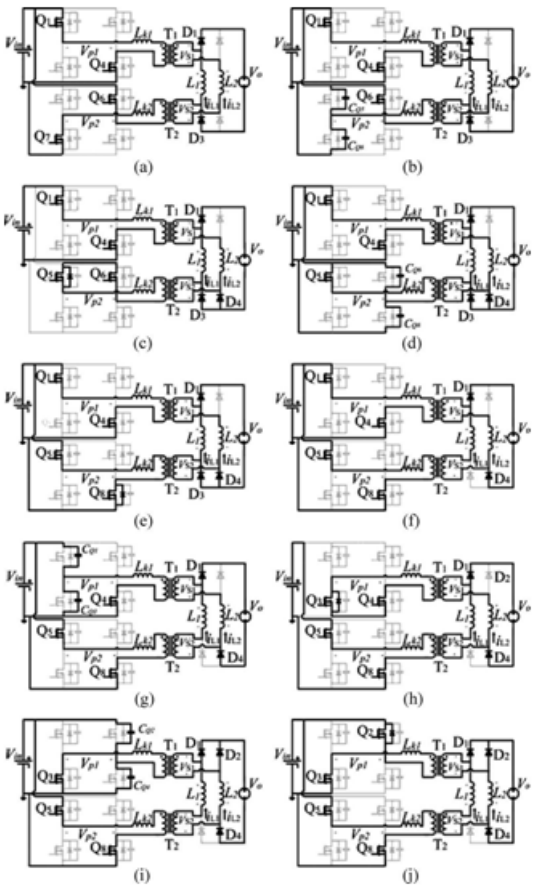

Fig. 5.Equivalent circuits for different modes in case 1. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5. (g) Mode 6. (h) Mode 7 (i) Mode 8. (j) Mode 9.

Mode 4 [t_4 –t_5]: Because switch $Q_8$is turned ON at t_4, theinput voltage is across the leakage inductance L_{k2} because secondary-side diodes D_3 and D_4 are still in current com-mutation. The primary current $i_{L\ k2}$ increases under the slope V_{in} /L_{k2}. When the current commutation between $D_3$and D_4completes, primary current $i_{L\,k2}$ reaches ni_{L1} at t_5 and this mode ends.

Mode 5[t_5 –t_6]: After t_5, Q_1, Q_4, Q_5, and $Q_8$are ON. Theinput power is transferred to the load through T_1 and T_2 . Both the secondary-side voltages of the transformers, *V*s1 and *V*s2 , are positive, so diodes D1 and D4 conduct. Primary current *iLk*1 equals *niL*2 , and *iLk*2 equals to *niL*1.The currents of output inductances *iL*1 and *iL*2 are increasing with the same slope of (*nV*in− *Vo*)/*L*1 . The voltages across the diodes D2 and D3 arebothnVin . The equivalent circuit is shown in Fig. 5(f). This mode ends when Q1 turns OFF.

Mode 6[t6 –t7]: Q1 turns OFF at *t*6 . The output inductances*L*1 and *L*2 are large, so they are seen as current sources during this switching interval. The parasitic capacitances *C*Q1 and *C*Q3 are charged and discharged by the primary current source *iLk*1 , respectively. The equivalent circuit of this mode is shown in Fig. 5(g) and it is similar to mode 1.This mode ends when *V*p1 decrease to zero.

Mode 7 [t7 –t8]: After *V*p1 reaches zero, *VC*Q3 decreases to zero too. Then, Q3 turns ON at ZVS condition, and primary voltage of T1 is clamped to zero. Therefore, the winding of the transformer T1 is short circuited and primary current *iLk*1 is circulating at primary side. Also, secondary-side diodes D1 and D4 are both conducting. Primary current *iLk*2 is clamped to *niL*2 . During this interval, the current of *L*2 is decreasing with the slope of *Vo*/*L*2 . Diode D2 remains OFF. The equivalent circuit of this mode is in Fig. 5(h). This mode ends when Q4 turns OFF.

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Mode 8 [t8 –t9]: At *t*8, Q4 is turned OFF. The circulating primary current begins to charge *C*Q4 and discharges *C*Q2, respectively. When *VC*Q2 reaches zero at *t*9 , the ZVS-on condition for lagging leg switch Q2 can be achieved. The current commutation between D1 and D2 begins at *t*8 , which leads to short circuit at secondary side of T1 . The simplified equivalent circuit of this mode is similar to that in Fig. 5(i). It can be simplified into a resonant circuit between *Lk*1 and equivalent parasitic capacitances. It is similar to mode 3. When *VC*Q2 reaches zero at *t*9 , this mode ends.

Mode 9 [t9 –t10]: After *VC*Q2 decreases to zero, Q2 turns ON.And, the input voltage *V*in is across leakage inductance *L*k1because the currents in D1 and D2 are still commutating. Theprimary current *iLk*1 increases under the slope *V*in/*Lk*1.Whenthe current commutation betweenD1 andD2 completes, primary current *iLk*1 reaches *niL*2 at *t*10. Then, this mode ends.Since the two interleaved channels operate symmetrically, theoperations of next half period started from *t*9 are the same asprevious modes except that the roles of the two channels areexchanged. After that, one cycle is completed. According to the volt-second balance of inductor *L*1 in one switching cycle, the steady-state gain of the proposed rectifier can be derived in (2) and (3). It is assumed that the duty cycles *D* of two phases are identical.

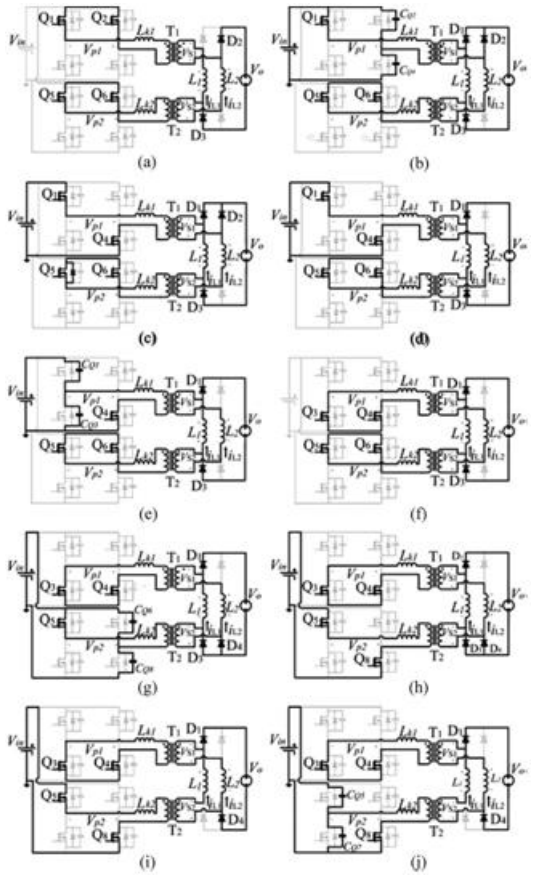

Fig. 6.Equivalent circuits for different modes in case 2. (a) Mode 0. (b)Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5. (g) Mode 6. (h) Mode 7.(i) Mode 8. (j) Mode 9.

Mode 0 [t0 –t1]: Q1, Q2, Q5 , and Q6 are ON during this mode; both *iLk*1 and *iLk*2 are circulating in the primary side. *V*s1 and *V*s2 are clamped to zero, so diodes D2 and D3 conduct. Primary current *iLk*1 equals *niL*1 , and *iLk*2 equals *niL*2 .

*Mode 1 [t1 –t2]:*Q2 turns OFF at *t*1 , and the circulating current charges *C*Q2 and discharges *C*Q4. The current in D1 and D2 begins to commutate, and the equivalent circuit is presented as Fig. 6(b). The charge procedure is similar to mode 3 in case 1, so it is not repeated again. The current commutating between D1 and D2 starts at *t*1 .

Mode 2 [t2 –t3]: The current commutating between D1 and D2 continues during this interval, so the

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primary current $iLk1$increases under Vin , when $iLk1$ reaches $niL2$ at $t3$, this modeends.

Mode 3 [t3 –t4]: The current commutating completes at $t3$; after that, phase 1 is transferring energy to the load while phase 2 is circulating in the primary side. Secondary diodes D1 and D3 are conducting. During this interval, $iL1$ is decreasing under

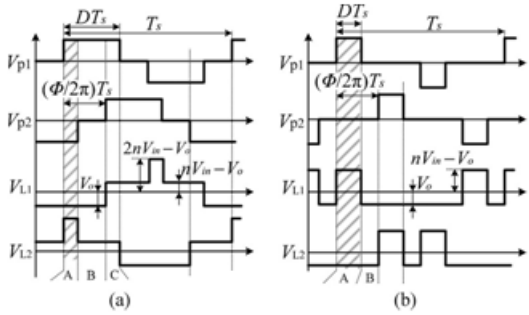

Fig. 7. Simplified key waveforms of SPAR-CDR. (a) D> α, Case 1. (b)D<α, Case 2.

The slope of V_o/L_1 and i_{L2} is increasing under the slope of $(nV_{in}-V_o)/L_2$. The equivalent circuit of this mode is present in Fig. 6(d). When Q_1 turns OFF at t_4 , this mode ends.

Mode 4[t_4 –t_5]: Q_1turns OFF at t_4, and$i_{L\,k1}$charges $C_{Q\,1}$and discharges $C_{Q\,3}$; the primary current $i_{L\,k1}$ can be treated as a constant current source in this interval, and it charges the par-asitic capacitances of the MOSFETs. When the drain to source of Q_3 ($V_{CQ\,3}$) reaches zero at t_5 , this mode ends.

Mode 5 [t_5 –t_6]–mode 9 [t_9 –t_{10}]: These modes are similar tomodes 0–4 because of the symmetry of circuit. Phase 1 circulates in the primary side, and phases 2 transfers energy to the load. The equivalent circuit refers to Fig. 6(f)–(j).

The next half switching period is symmetric with above de-scriptions. According to the volt-second balance in one switching cycle of inductor $L1$, the steady-state transfer gain of the rectifier can be derived in (4) and (5) as follows:

C.Operating Principle of Transformer WindingSeriesParallel Autoregulation

According to the analysis presented above, the major dif-ference between two operating cases is the equivalent working structure of the secondary rectifier. Fig. 7 shows the simplified key waveforms of two cases from Figs. 3 and 4 by neglecting the switching transition modes and primary devices. When the duty cycle D is larger than the normalized phase-shift angleα (case 1), the half switching cycle can be divided into four intervals with three equivalent stages: I, II, and III. When the duty cycle D is less than α (case 2), the half switching cycle can be divided into four intervals with two equivalent stages (II and IV). Fig. 8 shows the simplified secondary-side equivalent circuits of four stages, where the secondary windings are replaced with voltage sources V_{s1} and V_{s2} , respectively. In stage I, V_{s1} and V_{s2} are in series shown in stage I of Fig. 8. The voltage across the inductor L_2 is $(2nV_{in}-V_o)$, presented in Fig. 7(a). In stage II, V_{s1} and V_{s2} work alternatively in half switching cycle, leading to different equivalent circuits in Fig. 8. Hence, one of the voltages across the output inductors is $(nV_{in}-V_o)$ and the other is V_o. In stage III, the voltage sources $V_{s1}$and $V_{s2}$are in parallel as shown in Fig. 8. And, the voltages across L_1

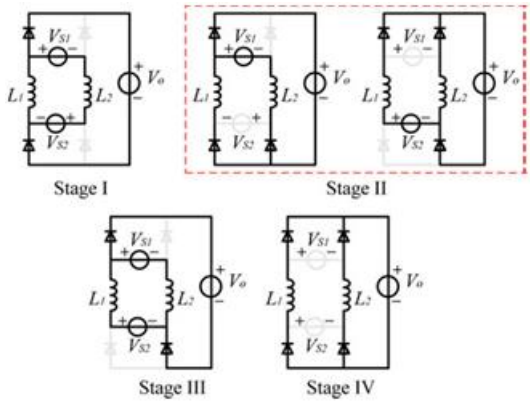

Fig. 8.Simplified secondary-side equivalent operating stages.

AndL2 are both $(nV_{in}-V_o)$ in this stage. When the duty cycle D is less than α (case 2), there is a different stage IV comparedto stages in case 1.

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In this stage, the voltage sources V_{s1} and V_{s2}do not work, and all secondary diodes are in freewheelingcondition. Therefore, the voltages across the inductors L_1 and $L_2$are bothV$_o$. When the duty cycle D decreases and getting close to the normalized phase-shift angle α in case 1 (D> α), the time of stages I and III diminished gradually. When D equals α, there is only stage II left and the directions of V_{L1} and V_{L2} alter every half switching cycle. In case 2, D is smaller than the normalized phase-shift angle α. When D increases and gets closer to α, the time of stage IV gets shorter. When D equals α, there is only stage II left, which is the same as the situation in case 1. The circuit operations in two cases when D equals α are identical, so the transition between two cases is smooth. With the SPAR-CDR rectifier structure, the interleaved PSFB converter can work with transformer winding series–parallel regulation according to duty cycle condition. In case 1 (D> α), there are a series connection interval and a parallel operating interval of transformer windings in half switching cycle.

III.DESIGN CONSIDERATIONS FOR THE PROPOSED CONVERTER

A. Steady-State Gain and Turns Ratio

Based on (2)–(5), the conversion gain of the proposed con-verter in both cases can be expressed in (6), where the duty cycle loss is ignored. It is noted that the phase-shiftangleα does not influence the conversion gain. It means that when the duty cycle is close to α, though the perturbation of duty cycle will change the operating modes of the rectifier, there is no step of steady-state gain between two operation cases The turns ratio of the transformers is designed in such away that the expected output voltage should be guaranteed, even under the minimum input voltage. Ignoring the turn on resistance of the MOSFETs and voltage drop of the rectifier

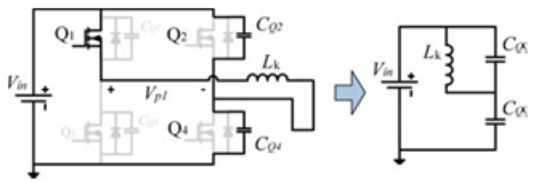

Fig. 9.Equivalent circuit for ZVS procedures of lagging legs.

B. ZVS Condition

Calculating the leakage inductor (Lk) is based on the amount of energy required for ZVS. This energy needs to deplete the energy from the parasitic capacitance before the corresponding MOSFET in the lagging leg is turned ON. Take phase 1 as an example [refer to Fig. 5(i) and Fig. 6(b)], the current commutation clamps the transformer voltage to zero and only the primary current is charging and discharging the capacitors CQ2 andCQ4,so the ZVS condition for the lagging leg devices depends on theenergy stored in the leakage inductance. Assume that the dead time is long enough for the charge procedure. The equivalent circuit of this procedure is plotted in Fig. 9. Define λ as the load percentage boundaries of the ZVS working area for lagging leg. It means that ZVS is realized from λ · load to full load, and ZVS is lost from no load to λ · load. Take λ = 0.4 as an example, ZVS of lagging leg is achieved when output current is larger than 0.4 · Iomax and it is lost when output current is smaller than 0.4 · Iomax, where Iomax is the output current at full load. Under the condition that the converter achieves ZVS at 100% load down to λ load, the leakage inductance can be calculated as

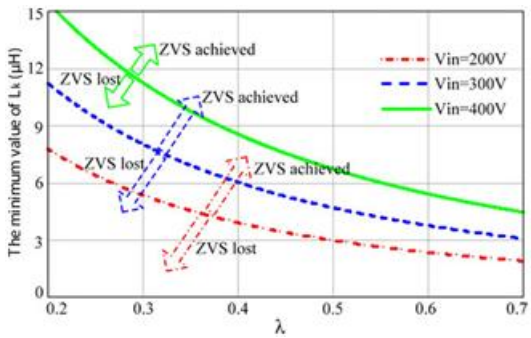

Fig. 10.Leakage inductance value in function of load range.

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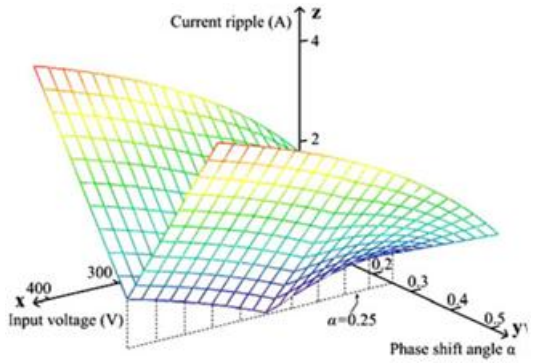

Fig. 11. Relationship of current ripple, input voltage, and the normalized phase-shift angle.

Fig. 10 presents the selection of a leakage inductor. The vertical axis is the value of Lk , and the horizontal axis is the value of λ. The region above the line means that the charge energy is large enough to achieve ZVS. The region below it means that ZVS is lost. When the input voltage range is wide, the highest input voltage should be considered to select the leakage inductance. The higher the input voltage, the larger the leakage inductance is needed. Nevertheless, larger leakage inductance leads to a longer current commutation period of the secondary diode, which means larger duty cycle loss. It decreases the efficiency in return. So a compromise should be made when selecting the leakage inductance.

C. Output Current Ripple

The normalized phase-shift angle α does not influence the conversion gain, but determines the current ripple of the output inductor. The output current ripple Δio with different α and D is expressed as (11) shown bottom of the next page The relationship of the ripple magnitude, the normalized phase-shift angle, and input voltage is presented by the 3-D graph in Fig. 11. The picture indicates that when normalized phase-shift angle α is 0.25, the current ripple is minimized.

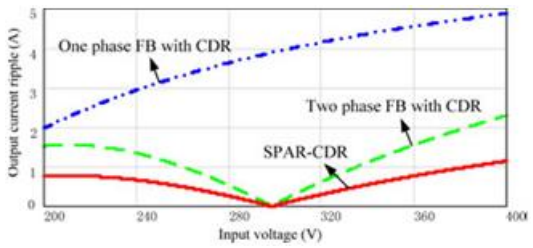

Fig. 12. Current ripple of different rectifiers with the same filter inductance.

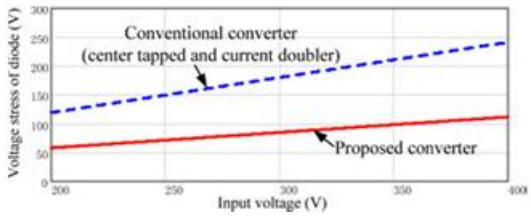

Fig. 13.Voltage stress of the secondary-side diodes.

Fig. 12 shows the current ripple comparison of conventional PSFB converters with CDRs and the SPAR-CDR structure as a function of the input voltage. They have the same pri-mary structure, control strategy, and the output-filter inductance (L_o = 60 μH). The output current ripple of the proposed recti-fier is much smaller than that of one-phase conventional CDR. The interleaved two-phase CDR decreases the current ripple because of the interleaving controlling scheme, but the current ripple is also twice as the

D. Diode Stress

The voltage stresses of the rectifier diodes in the proposed converter are given as

$$V_{Diode} = nV_{in\,max} = V_o/(2\cdot D_{min}). \quad (13)$$

Fig. 13 depicts the voltage stress of the proposed converter, the conventional PSFB converter with center-tapped rectifier, and the one with CDR. The voltage stress of the SPAR-CDR

TABLE 1:PARAMETERS OF THE PROTOTYPE

	Proposed	Center tapped
V_{in}	200–400 V	
V_o, I_o	50 V/20 A	
Frequency	100 kHz	
Primary MOSFETs	STP21NM60N	STP21NM60N
Secondary diodes/SRs	V20150S/ IPB108N15N3G	STTH20R04W/ ———
Transformer	Core: PQ32/30 Turns ratio: 30:9 L_m :2 mH; L_k :1.6 μH	Core: PQ32/30 Turns ratio: 30:9:9 L_m :2 mH; L_k :1.6 μH
External leakage	7 μH	7 μH
Output inductor	60 μH	60 μH

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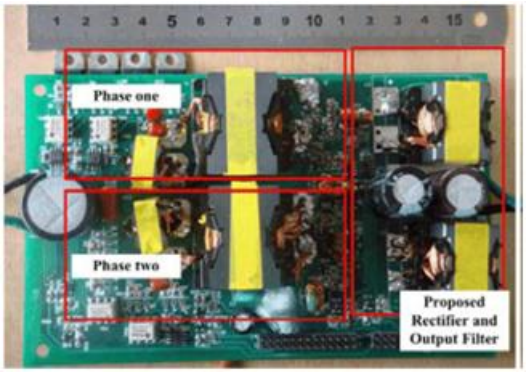

Fig. 14. Photograph of the experimental prototype.

structure is reduced to around 50%, which means that better diode with lower breakdown voltage and forward conduction voltage can be adopted. In order to increase the efficiency, SR can be applied to the proposed rectifier as well. The voltage stress for the SPAR-CDR is around 100 V, so a 150-V MOSFET with very low conduction resistance is preferred. Although there are less conducting devices in the center-tap rectifier, the voltage stress for center-tapped rectifier is around 250 V; 300–400-V breakdown voltage devices should be selected. In such a voltage level, the MOSFETs are not popular and their performances are not optimized, leading to high conduction loss and series reverse recovery loss.

IV. EXPERIMENTAL RESULTS:

A 200–400-V input, 50-V/20-A output PSFB converter with the SPAR-CDR structure was designed to validate the

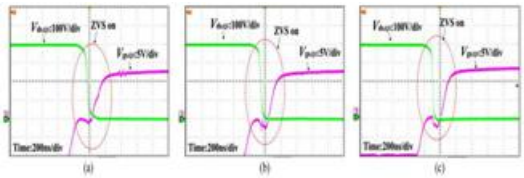

Fig. 15.ZVS performance of leading leg under different load conditions. (a) When I o = 2 A. (b) When I o = 10 A. (c) When I o = 20 A.

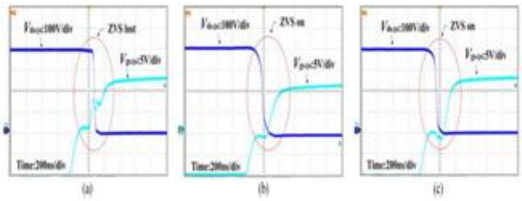

Fig. 16.ZVS performance of lagging leg under different load conditions. (a) When I o = 2 A. (b) When I o = 10 A. (c) When I o = 20 A.

Theoretical analysis and demonstrate the circuit performance. A DSP controller (TMS320F28335) is employed for the feed-back control and gate signals generation. The gate signals are passed to the primary side through isolated driving transform-ers. A prototype with conventional center-tapped rectifier is also built-up for comparison. The key parameters of the prototypes of the proposed and conventional converters are presented in Table I. These parameters are designed according to the analysis in Section III. Fig. 14 shows the photograph of the experimental prototype. The experimental waveforms of the proposed converter with diode rectifier (see Fig. 2) are given in figs.15–20. Fig. 15 shows the drive signal V_{gs} and the drain–source voltage V_{ds} of switch Q_3 in the leading leg under different load conditions. It indicates that ZVS of the leading legs is achieved under different load conditions.

It is easier to realize ZVS-on for the leading legs than that of the lagging leg, as the junction capacitors of the switches in the leading leg are charged by the reflected current of the output inductor and the energy stored in the output inductor is quite large. Fig. 16 gives the waveforms of the drive signal $V_{gs}$and the drain–source voltage$V_{ds}$of switch Q_4in the laggingleg. At light load, ZVS is not fully realized [see Fig. 16(a)] and there is a miller platform in the driving signal. This is because the energy in the leakage inductance is not enough to charge the junction capacitance. At half and full load [see Fig. 16(b) and(c)], ZVS-on is fully achieved, which accords with the theory calculation.The experimental waveforms of the secondary-side elements are shown in Figs. 17 and 18. Fig. 17 presents the voltage wave-forms across the diodes under different duty cycle conditions. Since the values of the voltage stress across the diodes are nV_{in}, it varies with different input voltage.

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Fig. 18 presents thesecondary-side transformer voltages V_{S1} ,V_{S2} and the voltage across inductors V_{L1} , V_{L2} . It shows that all the waveforms are agreed well with the theoretical analysis in the previous section.

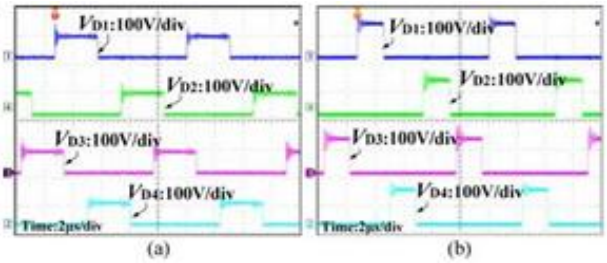

Fig. 17.Measured voltages across the diodes at different input voltage.(a) Case 1, D> α. (b) Case 2, D< α.

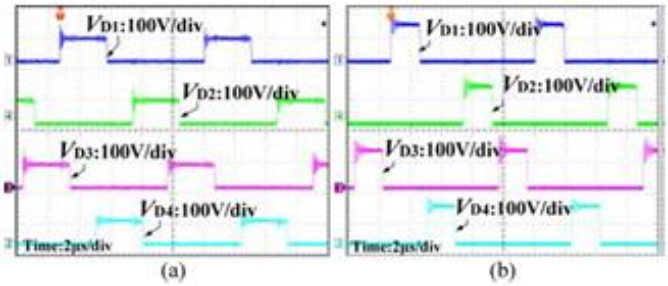

Fig. 18. Measured voltages across secondary windings and output voltage of rectifier at different input voltages. (a) Case 1, D> α. (b) Case 2, D< α.

(see Figs. 3 and 4). Fig. 18(a) shows measured when D> α, the convexes in V_{L1} and V_{L2} indicate that when input voltage is low, the two channels work in series during these intervals, and the value is $2nV_{in}-V_o$. Fig. 18(b) shows measured when D <α and two channels work in turns. Fig. 19 presents the primary waveforms including the mid-point voltage of two bridges (V_{p1} ,V_{p2}) and the primary current (i_{p1} , i_{p2}) under two working cases, which accords with the the-ory analysis in Figs. 3 and 4. Fig. 20 measures the current in the output inductors and the total output current under differ-ent operating cases when I_o is 10 A. Because of the current

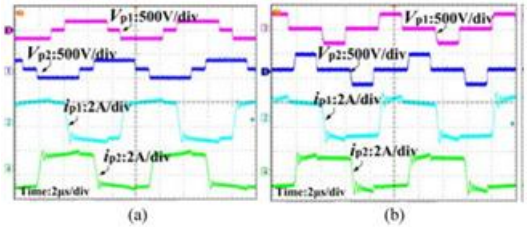

Fig. 19.Measured voltages across primary windings and primary currents at different input voltages.(a) Case 1, D> α. (b) Case 2, D< α.

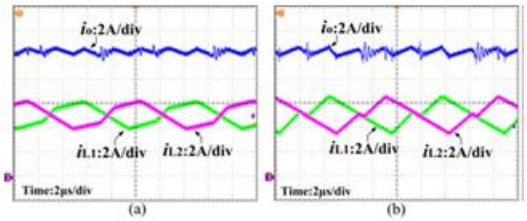

Fig. 20.Current waveforms of the output inductors and the total output current ripple.(a) Case 1, D>α. (b) Case 2, D< α.

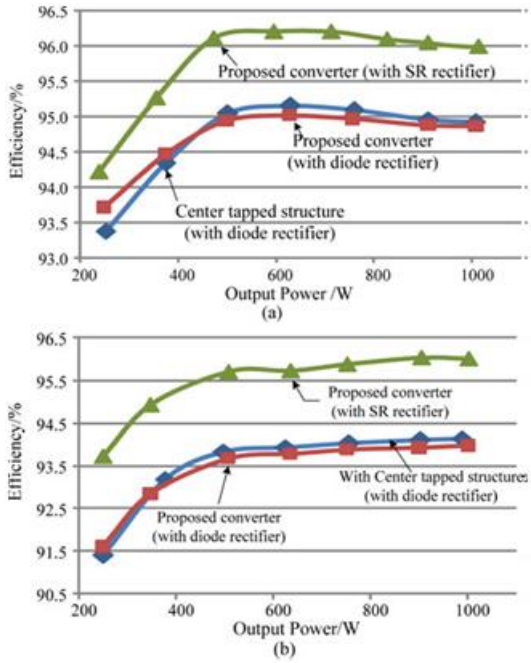

Fig. 21. Measured efficiencies of prototypes under varying load conditions and working cases. (a) Case 1, when V_{in} = 200 V (D> α). (b) Case 2, whenV_{in}= 400V (D < α).

Cancellation effect of the interleaving operation, the total output current ripple reduced a lot.

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The measured efficiencies at various load conditions and different input voltages of the prototypes are shown in Fig. 21. When using the diode rectifier, the proposed converter shares almost the same efficiency with the conventional center-tapped converter. Though the proposed rectifier (with Schottky diode, 150 V) has larger conduction loss, the Scotty diode has verylittle reverse recovery loss. The center-tapped rectifier (with fast recovery diode, 400 V) has lower conduction loss, but the re-verse recovery loss of the fast recovery diode is much larger than the Scotty ones, so the general efficiencies are almost equal. However, since the proposed structure reduces the volt-age stresses of the rectifier diodes, it becomes more valuable to apply the SR in the secondary side. When adopting the SR rectifier, the efficiency is improved to about 0.7–1.8%.

V. CONCLUSION:

A novel two-phase interleaved PSFB converter with hybrid CDR is presented in this paper. The secondary-side windings of the transformers can be autoregulated between series and paral-lel structures under different duty cycle conditions. The voltage stresses of the rectifiers are reduced and low-voltage MOSFETs can be used as SR to improve the efficiency. Furthermore, the current cancellation of interleaving control scheme reduces the current ripple of the output filter and decreases the filter size. Experimental results verified the theoretical analysis, and the efficiency of the proposed converter can be improved to about 0.7–1.8% compared to the conventional PSFB with the center-tapped converter.

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