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An Efficient Design of Adder/Subtractor using P2RG Reversible Gate

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ABSTRACT

Present day VLSI circuit outline is represented by low power utilization prerequisites of ICs. Reversible rationale has gotten incredible significance due to no data bit misfortune amid calculation which brings about low influence dispersal. Additionally, there is a need to change over the reversible circuits into shortcoming tolerant reversible circuits to recognize the event of mistakes. Equality safeguarding property can be utilized for this. Another 5*5 equality protecting reversible door is proposed in this paper, named as P2RG. The most huge part of this work is that it can work both as a full viper and a full subtractor by utilizing one P2RG and Fredkin entryway as it were. Proposed outline is better as far as entryway number, junk yields, consistent data sources and region than the current likenesses. Along these lines, this paper gives the underlying edge to outline more mind boggling frameworks which will have the capacity to execute more confused operations utilizing equality protecting reversible rationale.

Index Terms—Reversible logic; Parity Preserving; P2RG; Adder/Subtractor

I. Introduction

In today's specialized world, warm contemplations, re-risk issues and effectiveness have ended up significant concerns. These days, examination is being done to plan a framework with superior, speed and low power scattering or in a perfect world no warmth era. As force utilization is a noteworthy limitation in planning of VLSI circuits so we have to change to that registering world where no data misfortune exists on the grounds that as indicated by Landauers rule, on all of calculation, routine advanced frameworks disperse KTln2 measure of vitality, where K is Boltzmanns consistent and T is the temperature at which the calculation is performed [1]. Bennett demonstrated that this vitality dissemination would not happen in the event that the same number of data bits are produced, i.e. no data misfortune exists [2].Present irreversible advancements disperse a considerable measure of warmth as far as bit misfortune which diminishes life of the circuit. Every single consistent operation in today's traditional PCs are irreversible. It implies extraction of contribution from the separate yield is impractical. Then again, reversible calculation has a striking component of one of a kind balanced mapping amongst data sources and yields which lessens the real issue of force dispersal with no data misfortune.

A Reversible logic is characterized by:
1.Equal number of inputs and outputs.
2.There exists one to one mapping between the respective inputs and outputs.
3.Loops and fan out are not allowed.

In traditional PCs, just NOT door performs reversible operation since it has an equivalent number of data sources and yields with their one of a kind coordinated mapping. Some reversible doors have as of now been proposed in writing like the controlled-not (CNOT) (proposed by Feynman) [3], Toffoli and Fredkin entryways [4], IG Gate [5] and MIG entryway [6]. Reversible entryways have different application in the planning of adders, subtractors, multipliers [7], [8] and so on, same like established PCs. The fundamental center of this paper is to outline a circuit that can fill in as viper and also subtratctor all the while with least quantities of waste yields, steady information sources

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and zone.Remaining part of the paper is devised as follows: Explanation of Design constraints of reversible circuits and some important definitions are given in section II. Reversible gates present in literature are given in section III. Proposed gate is shown in section IV. Application of the proposed design is shown in section V. Results with comparison table is shown in section VI and finally conclusion and future work are made in section VII.

II. DESIGN CONSTRAINTS AND DEFINITIONS

Minimizing the quantity of Ancillary (consistent) Inputs: An additional, assistant piece or altered qubit state that is added to the essential contributions to request to accomplish the particular usefulness yet they should be minimized for minimizing helper stockpiling.

Minimizing the quantity of Garbage Outputs: Outputs that are not utilized further, required just to make the capacity reversible (which results to minimize region and force).

Minimizing the Gate Count: Number of entryways that are utilized to understand the framework is door tally [9].

Adaptation to internal failure: Any physical gadget while performing established or quantum calculation is subjected to mistake either because of commotion in the earth or blame in the gadget. It can be identified by flaw tolerant registering. In spite of the fact that reversibility can recoup bit misfortune, yet it can't recognize bit mistakes in the circuit [10]. Late advanced circuit planning is currently concentrating on the flaw tolerant reversible circuits.

Equality Preservation: It can be utilized for the adaptation to non-critical failure calculation. Shortcomings in the circuit can be distinguished by contrasting the equality of information sources and yields. The possibility of the equality protecting property in the configuration reversible rationale circuits was given by Parhami [11]. It is realized that reversible entryways have an equivalent number of information sources and yields. Along these lines, for equality conservation, this is adequate to demonstrate that equality of data sources and yields ought to be equivalent. For instance, in an equality safeguarding, 4*4 reversible door must fulfill the condition which is given underneath:

$$A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$$

Where A, B, C and D are gate inputs and P, Q, R and S are gate outputs.

III. LITERATURE SURVEY

In Fig.1, some existing fault- tolerant reversible gates are shown:

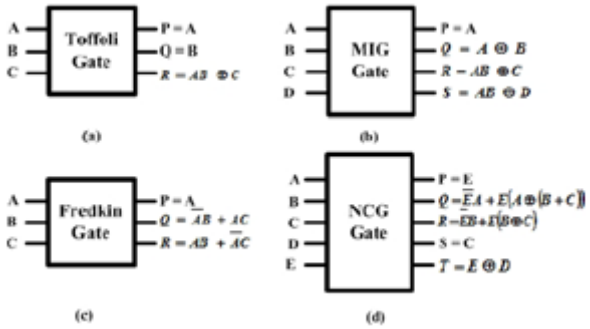

Fig. 1: (A) Toffoli Gate (B) MIG Gate (C) Fredkin Gate (D) NCG Gate

IV.PROPOSED DESIGN

A new 5*5 parity preserving reversible gate, P2RG is introduced in Fig.2 (a).

- This gate is one through which means one of its inputs is also an output.
- It is shown in Fig.2 (b) that Proposed gate is universal since it is able to perform NOR operation. When input B= 1 and D= 0 then output Q performs NOR operation i.e. (A+C)' . As it is known that NAND and NOR gates are universal gates so it can be concluded that it can be exploited to realize any arbitrary Boolean function.

Truth table of this gate is shown in Table 1, where A, B, C, D and E are the inputs and P, Q, R, S and T are the outputs. It can be seen from the table that all the input and output vectors are uniquely related. The

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parity preserving property is promptly verified from the table by comparing the parity of the input to the parity of the output that is (A⊕B⊕C⊕D⊕E) and (P⊕Q⊕R⊕S⊕T). Example: from the truth table of P2RG i.e Table 1, for the inputs 00010 respective outputs are 01011. According to the equation 1:

$$0 \oplus 0 \oplus 0 \oplus 1 \oplus 0 = 1 = 0 \oplus 1 \oplus 0 \oplus 1 \oplus 1$$

Like the above example, parity preserving property can be easily verified for the remaining inputs with their outputs also.

V.APPLICATION OF P2RG

In this machine subordinate time, we anticipate that PCs will do some sort of number juggling operation like expansion, subtraction. In this area primary commitment of the paper is displayed. It demonstrates how the thought functions. Thought behind the planning of P2RG entryway is to develop a combinational circuit that can fill in as full viper and in addition full subtractor on a solitary unit. We require just a control door to control the method of operation for the expansion/subtraction.

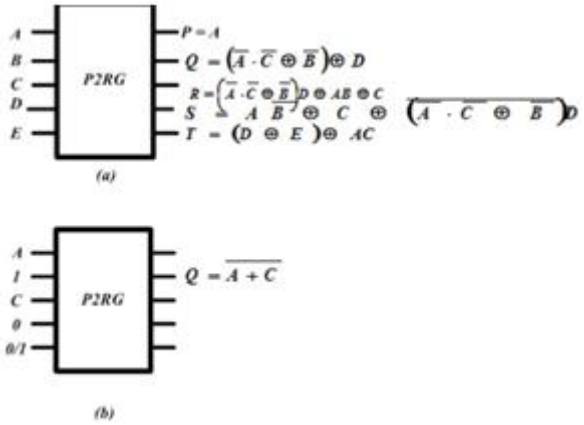

Fig. 2: (a) 5*5 parity preserving reversible gate (P2RG) (b) P2RG as universal gate.

A. Parity Preserving Half Adder/Subtractor

The equality protecting half snake/subtractor is acknowledged utilizing one P2RG entryway and one Fredkin door as appeared in Fig.3. Half viper and subtractor are the essential building square to outline full snake and subtractor. We require two data sources i.e. An and B to plan a half viper/subtractor. No past convey or acquire is required in this. Along these lines, this configuration has two information sources An and B and a control line Ctrl which will control method of operation, i.e. at the point when Ctrl is at rationale 0, the circuit will go about as half snake and when ctrl is at rationale 1, the circuit will go about as half subtractor. It will give three steady sources of info and four junk bits g1 to g4. Boolean expressions to understand the usefulness of half snake and half subtractor are given underneath:

$$Sum/Difference = A \oplus B$$

$$Carry = AB$$

$$Borrow = \bar{A} B$$

B. Parity Preserving Full Adder/Subtractor

Many adder designs using reversible gates by several authors have been studied. The proposed design will work as adder as well as subtractor on a single unit. The parity preserving full adder/subtractor is realized using one P2RG gate and one Fredkin gate. In Fig.4, the circuit has three inputs A, B, C in and a control line Ctrl which will control mode of operation. If Ctrl= 0, it will work as a full adder else it would function as a full subtractor. It has 2 constant inputs, C is set to 0 and E can be set to either 0 or 1. The basic Boolean expressions for sum/difference, carry and borrow are given below for full adder and subtractor:

TABLE I: Truth Table of P2RG Gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	1	1
0	0	0	1	1	0	1	0	1	0
0	0	1	0	0	0	1	1	1	0
0	0	1	0	1	0	1	1	1	1
0	0	1	1	0	0	0	0	1	1
0	0	1	1	1	0	0	0	1	0
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	0	0	1	0	1
0	1	0	1	1	0	0	1	0	0
0	1	1	0	0	0	0	1	1	0
0	1	1	0	1	0	0	1	1	1
0	1	1	1	0	0	1	1	0	1
0	1	1	1	1	0	1	1	0	0
1	0	0	0	0	1	1	0	1	0
1	0	0	0	1	1	1	0	1	1
1	0	0	1	0	1	0	1	1	1
1	0	0	1	1	1	0	1	1	0
1	0	1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1	0	0
1	0	1	1	0	1	0	0	0	0
1	0	1	1	1	1	0	0	0	1
1	1	0	0	0	1	0	1	0	0
1	1	0	0	1	1	0	1	0	1
1	1	0	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	1	0
1	1	1	0	0	1	0	0	1	1
1	1	1	0	1	1	0	0	1	0
1	1	1	1	0	1	1	0	0	0
1	1	1	1	1	1	1	0	0	1

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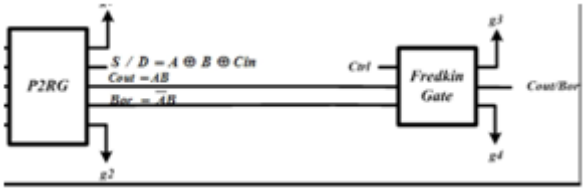

Fig. 3: Parity Preserving Half Adder/Subtractor using P2RG gate

$$(Sum/Difference = (A \oplus B \oplus Cin))$$

$$(Carry = ((A \oplus B).Cin) \oplus AB))$$

$$(Borrow = ((A).B) \oplus (((A \oplus B)).Cin))$$

Proposed circuit is optimized in terms of number of constant inputs and garbage outputs. Fig.4 shows the implementation of parity preserving full adder/subtractor in which g1, g2,g3 and g4 are garbage outputs.

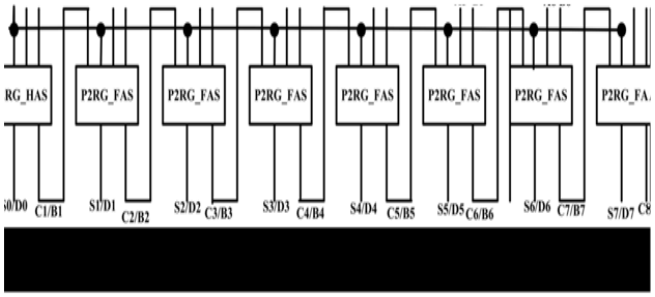

Fig. 5: Parity preserving 8-Bit Adder/Subtractor using P2RG gate

C. Parity Preserving 8-bit Parallel Adder/Subtractor

A n-bit parallel viper/subtractor will require a chain of (n-1) full adders/subtractor and one half snake/subtractor. Thusly 8-bit equality saving parallel snake/subtractor is planned by utilizing one equality pre-serving half viper/subtractor (P2RG HAS) and seven equality saving full viper/subtractor (P2RG FAS). It has two 8-bit numbers which are A0 to A7 and B0 to B7 as sources of info and a control line ctrl which will control the method of operation. At the point when ctrl line is set at rationale 0, the circuit will perform 8-bit expansion operation and when ctrl line is set at rationale 1, the circuit will perform 8-bit subtraction. The Carry/Borrow got after expansion/subtraction is spoken to by C1/B1 to C7/B7.Output convey/acquire of every piece, i.e. C1/B1 to C7/B7 will be the third contribution for the following piece. The yields, Sum/Difference and Carry/Borrow are appeared in the Fig.5 as S0/D0 to S7/D7 and C8/B8 individually. Fig.5 demonstrates the equality saving 8-bit parallel viper/subtractor.

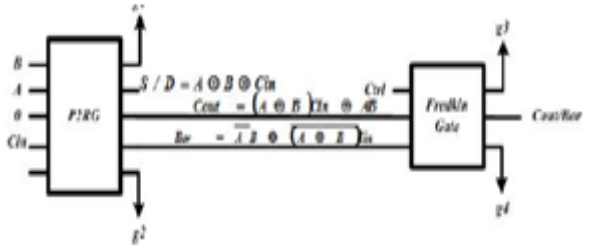

Fig. 4: Parity Preserving Full Adder/Subtractor using P2RG gate

VI. RESULTS

In past areas, a methodology for planning equality saving reversible full viper/subtractor has been talked about. At that point a methodology for equality safeguarding 8-bit parallel reversible full viper/subtractor has been talked about.

In this area, assessment of the proposed circuits with the assistance of the relative results is exhibited. Table II speaks to that the execution of proposed equality safeguarding reversible full viper circuit is better com-pared to existing partners. This configuration has been enhanced as far as steady information sources, waste yields and range. For zone estimation, CMOS acknowledgment is done in Microwind by utilizing 90nm innovation hub. Table III demonstrates that execution of equality saving 8-bit parallel snake/subtractor is superior to anything existing plans.

TABLE II: Comparative Experimental Results of Various Parity Preserving Full Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Area(μm)^2
F2G[12]	9	9	11	923.1
MIG[6]	5	5	7	671.0
Proposed Gate	2	2	4	454.5

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TABLE III: Comparative Experimental Results Of Various Parity Preserving 8-Bit Full Adder/Subtractor

	Gate Count	Constant Input	Garbage Output	Area(μm)^2
F2G[12]	67	67	82	9860.5
MIG[6]	37	37	52	7923.1
Proposed Gate	16	17	32	5289.1

VII. CONCLUSION AND FUTURE WORK

In this paper, a novel equality protecting reversible door, P2RG and its applications were proposed. The proposed circuit was contrasted and the current outlines as far as consistent information sources, trash yields, and territory. The consistent information sources and junk yields are streamlined. Region is enhanced by half for full snake/subtractor and 46.36% for 8-bit full viper/subtractor contrasted with the F2G entryway while 32.26% of territory is enhanced for full snake/subtractor and 33.24% of zone is enhanced for 8-bit full snake/subtractor contrasted with the MIG door. The configuration is better among all its current Counterparts as far as consistent data sources, waste yields and territory. Power computed of the full viper/subtractor is 0.214mil-liwatt while power ascertained of the same circuit utilizing irreversible door is 33.59milliwatt. So 33.376milliwatt measure of force is spared here. Similarly, we can see here the force dissemination in reversible circuits is verging on irrelevant contrasted with irreversible circuits in light of no bit misfortune. The reversible circuits proposed and composed in this work can frame the premise of equality protecting reversible ALU of a primitive quantum CPU.

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